# EXHIBIT 1

# D7 Pages 1-25

Appendix D7
Defendants and Counterclaimants' Invalidity Contentions
*Advanced Micro Devices, Inc., et al., v. Samsung Electronics Co., Ltd., et al., Case No. 3:08-CV-0986-SI*

**U.S. patent No. 5,559,990 Invalidity Chart: JP-62-1182-A ("the '1182 Reference")**

All asserted claims are anticipated by the '1182 Reference and/or are rendered obvious by it, either alone or in combination with other prior art described below and/or listed in Section I of Defendants' and Counterclaimants' Preliminary Invalidity Contentions and/or through modifications described below. Nothing in this invalidity chart should be construed as signifying or suggesting Defendants and Counterclaimants' adoption of or acquiescence in any claim scope and/or claim construction positions taken by Plaintiffs and Counterdefendants in this litigation.

| CLAIM | RESPONSE |
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| 1. A memory comprising: | Although a preamble is normally not limiting, should this preamble be limiting, this element is met in JP-62-1182-A ("the '1182 Reference"). Specifically, the '1182 Reference is titled "Semiconductor Memory Device." |
| a plurality of rows of memory locations; | This element is met in the '1182 Reference. Specifically, the '1182 Reference states that:<br><br>"For example, the memory array M-ARY 1 and the memory array M-ARY 2 have been allocated so that the column addresses will be 0-1023 and the row addresses will be 0-511, and in the event that they have been designated such that the storage capacity will be approximately 1 M bit in total, if the row address ax', which serves as the above-mentioned initial value, indicates the address 3 that has been allocated to the memory array M-ARY 1 that is on the left side, the above-mentioned expansion serial access mode will be in a selection state at the same time because of the word selection timing signals Φ x 1, Φ x 2 that are generated by the word line that corresponds to that and the word line that corresponds to the address 4 of the memory array M-ARY 2 on the right side. ['1182 Reference, Page 4, second column; *see also* Fig. 1; *see also* Claim 1] |

| CLAIM | RESPONSE |
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| a plurality of first registers, each first register for receiving a row address; | This element is met in the '1182 Reference alone or in combination with any of U.S. Patent No. 4,849,937 ("the '937 Reference") or U.S. Patent No. 5,367,495 ("the '495 Reference") or U.S. Patent No. 4,759,021 ("the '021 Reference"). Specifically, the '1182 Reference states that:<br><br>"Specifically, address signals that have been provided from an external terminal in accordance with operation mode signals that have been designated from specified external control signals are incorporated as the initial values; there is an address counter circuit that performs a stepping operation based on the pulse that has been provided from the external terminal; the address signals that have been formed by the above-mentioned address counter circuit in accordance with the above-mentioned operation mode signals are relayed to an address decoder via a multiplexer; and in accordance with the address signals formed by the above-mentioned address counter circuit, column selection operations for the other memory array where the word line is already in a state of selection is performed upon completion of the final selection of addresses for one of the memory arrays during column selection for the memory array that has been partitions into two." ['1182 Reference, Page 2, first and second column; *see also* Fig. 1; *see also* Claim 1]<br><br>To the extent AMD reads this limitation on the Samsung devices, this '1182 Reference meets this limitation.<br><br>The '937 Reference states:<br><br>"The address counter 81 receives the signals $Ø_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e., twice that of the basic |

| CLAIM | RESPONSE |
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| | clock pulses $Ø_S$). Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. In a similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e., twice that of the basic clock pulses $Ø_S$). Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42]<br><br>The '495 Reference states:<br><br>"The register 70a, 70b, 70c or 70d selected by the block decoder 50 holds 8-bit address codes ARC0-ARC7 supplied in synchronism with the row selection signal RAS. Since the holding of the address codes ARC0-ARC7 will be maintained even after access is shifted to another cell array block, these registers 70a-70d store respectively the address codes ARC0-ARC7 of the last access in the cell array blocks 10a-10d and supply them to the selectors 80a-80d which also receive the address codes ARC0-ARC7 supplied in synchronism with the row selection signal RAS and introduce them to the row decoders 20a-20d." ['495 Reference, Col. 4:25-37]<br><br>The '021 Reference states:<br><br>"Since the low-speed large-capacity memories 11, 12, 13, 14 performing the 4-way interleave operation are shifted in access timing usually by one cycle from each other, the memories 11-14 are provided respectively with registers 23-26 each for holding an address." ['021 Reference, Col. 4:5-9] |

| CLAIM | RESPONSE |
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| | Further, the '1182 Reference could be combined with any of U.S. Patent No. 5,274,596 ("the '596 Reference") or U.S. Patent No. 4,811,297 ("the '297 Reference") or U.S. Patent No. 5,367,495 ("the '495 Reference") to meet this limitation. |
| a plurality of row decoders, each row decoder for activating a portion of a row identified by signals from one of said first registers; | This element is met in the '1182 Reference. Specifically, the '1182 Reference states that:<br><br>"The row address decoders R-DCR1 and R-DCR2 decipher the above-mentioned address signals x0-xm and form the selection signals of the word line, are synchronized to the word line selection timing signals Φx1 and Φx2, and perform the selection operation of a one word line of the memory arrays M-ARY 1 and M-ARY 2 and dummy word line. ['1182 Reference, Page 3, first column]<br><br>Further, the '1182 Reference could be combined with any of the '596 Reference or the '297 Reference or the '495 Reference to meet this limitation. |
| one or more sense amplifiers for amplifying contents of said memory locations in the row portions; and | This element is met in the '1182 Reference. Specifically, the '1182 Reference states that:<br><br>"During writing and reading, the sense amplifiers SA1, SA2 will be in an operative state selectively because of the dynamic signals Φ pa1, Φ pa2, references will be a slight reading voltage from the memory cell that has been linked to one data line by the operation of the selection of a word line and standard voltage from the dummy cell that has been connected to the other data line by the operation of selection of a dummy word line, and the complementary data lines will be amplified to a high level." ['1182 Reference, Page 3, first column] |

| CLAIM | RESPONSE |
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| an output for providing output signals from said sense amplifiers, | This element is met in the '1182 Reference. Specifically, the '1182 Reference states:<br><br>"In response to that, if there is a reading operation where only the main amplifier operation timings signals Φma1 are at a high level, the main amplifier MA 1 will be in the operative state, and the write-enable signals [we bar] will be at a high level, and the memory information from the memory cell that has been selected as mentioned above will be transmitted to the external terminal D through the data output circuit of the data input-output circuit I/O." ['1182 Reference, Page 5, second column] |
| wherein at least two locations L1 and L2 in different rows having different row addresses in said memory can be read out to said output in burst mode such that the memory receives an address of one of said locations and provides in response contents of a plurality of memory locations, including the locations L1 and L2, in the sequence of consecutive addresses, so that while one of said row decoders is activating a row portion comprising said location L1 and contents of said location L1 are being transferred from one or more of said sense amplifiers to said output, another one of said row decoders is activating a row portion comprising said location L2 and contents of said location L2 are being transferred from said location L2 to one or more of said sense amplifiers. | This element is met in the '1182 Reference alone or in combination with the '494 Reference or the '196 Reference.<br><br>Specifically, the '1182 Reference states that:<br><br>"During writing and reading, the sense amplifiers SA1, SA2 will be in an operative state selectively because of the dynamic signals Φ pa1, Φ pa2, references will be a slight reading voltage from the memory cell that has been linked to one data line by the operation of the selection of a word line and standard voltage from the dummy cell that has been connected to the other data line by the operation of selection of a dummy word line, and the complementary data lines will be amplified to a high level." ['1182 Reference, Page 2, second column to Page 3, first column]<br><br>"Moreover, the next word line in the other memory array will be switched during the switching of the column in the first memory array, and, as a result, all of the bits can be read continuously." ['1182 Reference, Page 6, |

| CLAIM | RESPONSE |
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| | first column]<br><br>"There is an effect that is obtained whereby high-speed access that corresponds to all bits can be carried out by alternate switching of the word line selection operation and the operation of the sense amplifier to access another memory array next during column switching in response to the other memory array, which is one of the two memory array." ['1182 Reference, Page 6, first and second columns]<br><br>"Two types of access operation can be carried out selectively, namely, access by 1-bit units and expansion serial access mode (it includes in effect a conventional column static mode and a nipple [sic] mode)." ['1182 Reference, Page 6, second column]<br><br>The '494 Reference states:<br><br>"The selection of memory locations forming each cyclic pattern of addressing is controlled by the control unit 13. The row counter 45 and column counter 44 are connected so that unless instructed by the control 13 to do otherwise they count through successive addresses along each row and then row by row." ['494 Reference, Col. 8:22-27]<br><br>"Consequently after reaching address 0 the column and row counters cycle sequentially along each row for the two memory blocks in turn (starting at column zero of row 0 in array 0) using all memory locations in each row and then moving to the next row and repeating the operation." ['494 Reference, Col. 11:26-31]<br><br>"addressing sequentially more than one memory location in said first memory block and effecting a data transfer for each memory location |

| CLAIM | RESPONSE |
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| | addressed, and at the same time effecting an equate operation on bit lines in said second memory block; and after addressing memory locations in said first memory block, switching said addressing and equate operation so as to address sequentially more than one memory location in said second memory block and effecting a data transfer for each memory location addressed and at the same time equating bit lines in said first memory block." ['494 Reference, Col. 13:36-48]<br><br>The '196 Reference states:<br><br>"In accordance with the present inventions, while a particular row is being accessed in one array, the corresponding bit lines in the other array are being precharged. Thus, as data is sequentially accessed along the one row and as the end of that row is reached, an immediate access can then occur to any row within the second array since the bit lines in that array will already have been initialied." ['196 Reference, Col. 2:60-67]<br><br>"In general, while one array is being accessed, the other array is being precharged (i.e., elevating the logic state of bit lines and settling transient signals) in preparation for the next access form such other array. Therefore, precharging times for one array overlap the time for performing read or write operation in the other array, and therefore do not limit operating speed." ['196 Reference, Col. 3:41-47] |
| 2. The memory of claim 1, said memory having a random mode in which the memory receives an address and provides in response the contents of a unique memory location, | It was well-known in the art to retain a random mode while adding the functionality of a sequential read operation. The following are illustrative:<br><br>EP 9 326 885 ("the '885 Reference") states: |

| CLAIM | RESPONSE |
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| | "The circuit provides both random and sequential access functions and allows the memory to be used as a shift register of variable length." ['885 Reference, Page 1]<br><br>U.S. Patent No. 5,263,003 ("the '003 Reference") states:<br><br>"In a first mode, the memory circuit responds to an initial request for access and an address signal by reading data from a storage location in one of the memory banks. Subsequent requests for access to continguous storage locations do no require an address signal, instead a control mechanism responds by generating an address to read data alternately from storage locations in the first and second memory banks. In a second mode, the memory circuit responds to every request for access to the memory circuit by enabling access to the first or second memory bank as indicated by an address which accompanied the request." ['003 Reference, Abstract] |
| wherein, both in burst mode and in random mode, while the contents of said location L1 are being transferred from one or more of said sense amplifiers to said output, the contents of said location L2 are being transferred from said location L2 to one or more of said sense amplifiers. | It would be obvious to a person of skill in the art that transferring the contents of a location L1 from one of the sense amplifiers to the output while the contents of a location L2 are transferred from the location L2 to one or more sense amplifiers could be used in either a burst mode or a random mode. *See* claim 1 above.<br><br>Further, to the extent AMD reads this limitation on the Samsung devices, this limitation is met by numerous prior art references having both a random access mode and a burst mode. |
| 3. The memory of claim 1 wherein when the locations | This element is met in the '1182 Reference alone or in combination with |

| CLAIM | RESPONSE |
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| L1 and L2 are read out in burst mode and when the contents of said location L1 are being transferred from one or more of said sense amplifiers to said output and the contents of said location L2 are being transferred from said location L2 to one or more of said sense amplifiers, the sense amplifiers from which the contents of said location L1 are being transferred are enabled and the sense amplifiers to which the contents of said location L2 are being transferred are disabled, but these latter sense amplifiers become enabled subsequently for amplifying the contents of said location L2. | any of EP 0 087 754 ("the '754 Reference") or U.S. Patent No. 4,937,788 ("the '788 Reference") or the U.S. Patent No. 4,849,937 ("the '937 Reference") or the '003 Reference or U.S. Patent No. 5,251,178 ("the '178 Reference").<br><br>The '754 Reference states:<br><br>"In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire memory means are greatly reduced." ['754 Reference, Page 4:16-20]<br><br>"As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-3 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58]<br><br>The '788 Reference states:<br><br>"According to this arrangement, only one plane is selected in accordance with the content of the upper-order two bits of the row address. The selected plane is activated and exhibits the memory operation but the rest of the planes which are under the non-selection state are inoperative. Therefore, the decoders and the sense amplifiers are inoperative in these inoperative planes and the memory is not refreshed. Therefore, power is consumed in only the selected plane and unnecessary power consumption |

| CLAIM | RESPONSE |
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| | in the other plane can be saved. Thurs, the requirement for low power consumption can be satisfied." ['788 Reference, Col. 5:57-68]<br><br>The '937 Reference states:<br><br>"The sense amplifier 86 is controlled by the signals SEEV to smplify the read data thereby to supply the same to the data latch 87, which in turn temporarily stores the outputs from the sense amplifiers 86. When the signals SEEV are at low levels, the data latch 87 is electically cut off from the sense amplifier 86. Data from the data latch 87 are transferred to the output latch 89 when the signals OEEV are at high levels. In a similar manner, the sense amplifier 96 is controlled by the signals SEOD to amplify the read data thereby to supply the same to the data latch 97, which in turn temporarily stores the outputs from the sense amplifier 96. When the signals SEOD are at low levels, the data latch 97 is electrically cut off from the sense amplifier 96." ['937 Reference, Col. 4:52-66.<br><br>The '003 Reference states:<br><br>"The flash memory control 99 also selectively enables one of tow sets of bi-directional data buffers 90 and 91 which respectively couple th bank data buses 82 and 83 to the processor section data bus 63. The bank data buses 81 and 83 can be coupled to the instruction bus 61 by the flash memory control 88 selectively enabling buffers 92 and 93, respectively." [003 Reference, Col. 9:21-27]<br><br>The '178 Reference states:<br><br>"Referring now to FIG. 2, the circuit of FIG 1 has been modified to utilize |

| CLAIM | RESPONSE |
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| | the fact that, when RA10=1, only one half of the ARRAY BANKs 20 are being utilized and that, when RA10=0, the other half of the ARRAY BANKs 20 are being utilized. In particular, the RA 10 address is used to cause only the half of the ARRAY BANKs 20 that are being utilized to draw power from the DRAM energy source during read/write operations, while at the same time permitting the periodic performance of the refresh cycle in the usual manner on all ARRAY BANKs." ['178 Reference, Col. 3:32-42] |
| 4. The memory of claim 1 wherein: | |
| said memory comprises k pluralities S-1, . . . , S-k of locations wherein k is a number of said pluralities and is greater than or equal to two;<br><br>for each plurality S-i, said sense amplifiers can receive simultaneously the contents of number m of locations from said plurality S-i, wherein m is a positive integer; and | This limitation is met by the '1182 Reference. Specifically, the '1182 Reference states:<br><br>"Although this embodiment is not especially restricted, the memory array is split into two on the left and the right such as M-ARY 1 and M-ARY 2 in its configuration. In the memory arrays M-ARY 1 and M-ARY 2, a column-type (data line) signal line consists of a pair of complementary data lines that have been placed parallel, and the two pairs of complementary data lines will constitute a set; in the diagram they are configured by a double intersecting method arranged to face the horizontal direction. . . . The above column decoder C-DCR deciphers the address signals like those set out below, is synchronized to the data line selection timing signals Φ y, and forms selection signals that are provided to the above-mentioned column switching circuits C-SW1, C-SW2." ['1182 Reference, Page 2, Column 2; *see also* Fig. 2 and Claim 1] |
| time tARA does not exceed m * (k-1) * (tOE), wherein: | A person of skill in the art would know that this timing relationship would be used when designing the memory disclosed in claim 1. |

| CLAIM | RESPONSE |
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| tARA is measured from the time that an address of a location is made available to said memory to the time when one or more of said sense amplifiers develop an output signal indicative of the contents of said location; and<br><br>tOE is the time to transfer an output of any one of said sense amplifiers to said output of said memory. | |
| 5. The memory of claim 1 | |
| wherein, in burst mode, a time in which each location of said plurality except said one of said locations is read out to said output after a previous location has been read out to said output is shorter than a time in which said one of said locations is read out to said output after said address of said one of said locations has been received by said memory. | This limitation is met by the '1182 Reference alone or in combination with any of the '885 Reference or U.S. Patent No. 4,918,587 ("the '587 Reference") or the '003 Reference or JP-02-282994-A ("the '994 Reference") or U.S. Patent No. 4,799,199 ("the '199 Reference"). Specifically, Figure 3 of the '1182 Reference illustrates this timing.<br><br>The '885 Reference states:<br><br>"Circuitry for serial read memory access utilizing a random starting address. Fast read access is provided without upsetting the original data pattern stored in the memory core if the sequential read is terminated in midstream." ['885 Reference, Page 1]<br><br>The '994 Reference states:<br><br>"For that reason, even if the address moves serially to the next row and changes, the data itself will be read at high speed $t_0$. As is evident from the explanation above, as long as serial access continues, the internal data can continue to be read at high speed." ['994 Reference, Page 4, Column |

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| | 1]<br><br>"In the specifications, the address access time $t_1$ is estimated at 150 ns, and $t_0$ is estimated at the level of 30 ns for simple determination at the number of steps of the gates. In a hypothesis of the worst-case scenario for the current jump command +1 instruction, the jump command would be 3 bytes for the operand +2 data, 1 instruction would be 1 byte. Therefore, the average access time is {150 ns x 1 + 30 ns x 3}/4 = 60 ns. In contrast, the access time is 150 ns when the invention is not used." ['994 Reference, Page 4, Column 2]<br><br>The '587 Reference states:<br><br>"The reduction in the memory access cycle time from a convention memory access operation, generally represented by the first prefetch with a three clock cycle span between event t1 and t2, is clearly evident when the times are compared to those of the consecutive prefetch operation extending for two clock cycles between corresponding time intervals t3 and t4. Time t2 and t4 identify the first clock interval suitable to initiate succeeding memory access operations." ['587 Reference, Col. 5:63-6:3]<br><br>The '003 Reference states:<br><br>"The consecutive program instructions are read alternately from the two memory banks 71 and 72. In the present example, the second program instruction will be read from the second bank 72 of the flash memory 55. When the second microprocessor 54 generates another read request on the control bus 62, the flash memory control 88 will respond by enabling the instruction bus buffer 93 associated with the second memory bank 72. As the first and second instructions were located at the same internal address |

| CLAIM | RESPONSE |
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| | in each of the two memory banks that instruction already will be present on the second bank data bus 83 from the previous access request. Thus, the length of time required to obtain the second instruction is considerably less than that needed for the first instruction." ['003 Reference, Col. 10:67-11:13]<br><br>"In this manner, the flash memory control 88 upon receiving a read request, alternately obtains instructions from the two memory banks 71 and 72. The process speeds the access to a series of contiguous storage locations. As long as each subsequent instruction is located at the next logical address, the bank address generator 86 controls the addressing and the second microprocessor 54 does not have to send an address with each access request." ['003 Reference, Col. 11:33-41]<br><br>The '199 Reference states:<br><br>"However, in some integreated circuit memory devices, several other storage cells are accessed simultaneously and the contents thereof are held temporarily in a buffer. Typically, the access addresses of the 'extra' storage cells differ from the original access address by only one or two bits. However, subsequent accesses to these cells can be accomplished by simply executing additional access cycles without changing the access address. In the art, such memories are referred to as 'nibble mode'. In some other integreated circuit memories, a portion of the original address can be 'assumed' for one (or more) subsequent accesses, so that only the least significant portion of the address needs to be decoded, etc. Thus, once the original access had been completed, subsequent accesses to 'related' storage cells will be significantly quicker." ['199 Reference, Col. 1:13-28] |
| 6. The memory of claim 1 wherein said memory is | This limiation is met by the '1182 Reference. Specifically, the '1182 |

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| fabricated in an integrated circuit. | Reference states:<br><br>"Shown in FIG. 1 is a block diagram of a dynamic-type RAM in which the invention has been applied. The circuit component that constitutes the circuit blocks in the diagram is not especially restricted by the manufacturing technology for a semiconductor integrated circuit that is known in the industry; however, it is formed on a semiconductor substrate such as single crystal silicon." ['1182 Reference, Page 2, second column] |
| 7. The memory of claim 1 further comprising: | |
| a plurality of second registers, each second register for receiving at least a portion of a column address; and | This limitation is met by the '1182 Reference alone or in combination with any of U.S. Patent No. 4,875,196 ("the '196 Reference") or the '937 Reference. Specifically, the '1182 Reference states:<br><br>"Address buffer R, C-ADB is not especially restricted; however, it is synchronized to the internal control signals (not shown in the diagram) that have been formed based on the chip selection signals [cs bar], and it incorporates the row (X) address signals AX and the column (Y) address signals AY that consist of multiple bits that have been provided from an external terminal." ['1182 Reference, Page 3, first column]<br><br>To the extent AMD reads this limitation on the Samsung devices, the '1182 meets this limitation.<br><br>The '196 Reference states that:<br><br>"The row and column location in the arrays 31, 33 at which data is |

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| | accessed is controlled by the counters which, in one embodiment of the invention may be binary counters, or the like, which have an extended counting range that is double the number of address locations in the array to be accessed." ['196 Reference, Col. 4:49-55; See also, FIGS. 2A, 2B]<br><br>The '937 Reference states that:<br><br>"The address counter 81 receives the signals $Ø_{EV}$ to supply even X address signals to an X decoder 82 and even Y address signals to a Y decoder 83 in the cycle of the signals $Ø_{EV}$ (i.e. twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 82 are supplied to the first memory cell array 84 while outputs from the Y decoder 83 are supplied to the transfer gate 85. Ina similar manner, the address counter 91 receives the signals $Ø_{OD}$ to supply odd address signals to an X decoder 92 and add Y address signals to a Y decoder 93 in the cycle of the signals $Ø_{OD}$ (i.e. twice that of the basic clock pulses $Ø_{S)}$. Outputs from the X decoder 92 are supplied to the second memory cell array 94 while outputs from the Y decoder 93 are supplied to the transfer gate 95." ['937 Reference, Col. 4:29-42]<br><br>Further, the '1182 Reference could be combined with any of the '596 Reference or the '297 Reference or the '495 Reference to meet this limitation. |
| a circuitry for each second register for selecting in response to signals from one of the second registers a plurality of columns to be read by the sense amplifiers. | This limitation is met by the '1182 Reference. Specifically, the '1182 Reference states:<br><br>"Column switches C-SW1, C-SW2 receive selection signals that are formed by the above-mentioned column address decoder C-DCR, and |

| CLAIM | RESPONSE |
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| | they connect the above-mentioned complementary data lines on the memory array M-ARY 1 or the memory array M-ARY 2 to the common complementary data CD1, CD2." ['1182 Reference, Page 1, second column]<br><br>Further, the '1182 Reference could be combined with any of the '596 Reference or the '297 Reference or the '495 Reference to meet this limitation. |
| 8. A memory comprising: | Although a preamble is normally not limiting, should this preamble be limiting, this element is met in the '1182 Reference. Specifically, the '1182 Reference states that:<br><br>Although a preamble is normally not limiting, should this preamble be limiting, this element is met in the '1182 Reference. Specifically, the '1182 Reference is titled "Semiconductor Memory Device." |
| a set of consecutively addressed memory locations L1, . . . Ln; | This element is met in the '1182 Reference. Specifically, the '1182 Reference states that:<br><br>"Thereafter, when high-level clock signals are supplied to the external clock signals [CL bar], the address counter circuit COUNT receives the above-mentioned clock signals Φ and performs a+1 step operation. In that instance, the column-based counter circuit (Y) forms the carrier signals ca by the above-mentioned step operation, and that itself will be at address 0. In addition, the row-based address will change to 5." ['1182 Reference, Page 5, first column]<br><br>"(3) In the expansion serial access mode, there is an effect that is obtained |

| CLAIM | RESPONSE |
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| | whereby all that needs to be done is to change the external terminal because address signals are formed by a built-in address counter circuit, and, therefore, it will be very easy for users to handle." ['1182 Reference, Page 6, second column] |
| a plurality of sense amplifier circuits for amplifying contents of said memory locations; and | This element is met in the '1182 Reference. Specfically, the '1182 Reference states:<br><br>"During writing and reading, the sense amplifiers SA1, SA2 will be in an operative state selectively because of the dynamic signasl Φ pa1, Φ pa2 …." ['1182 Reference, Page 2, second column] |
| an output for providing output signals from said plurality of sense amplifier circuits, | This element is met in the '1182 Reference. Specifically, the '1182 Reference states that:<br><br>"In response to that, if there is a reading operation where only the main amplifier operation timings signals Φma1 are at a high level, the main amplifier MA 1 will be in the operative state, and the write-enable signals [we bar] will be at a high level, and the memory information from the memory cell that has been selected as mentioned above will be transmitted to the external terminal D through the data output circuit of the data input-output circuit I/O." ['1182 Reference, Page 5, second colum] |
| wherein said memory has a burst mode operation for receiving an address and reading out to said output, in response to said address, any given number of memory locations in the sequence of consecutive addresses with wrap around so that the next location, if any, to be read | This element is met in the '1182 Reference alone or in combination with the '494 Reference, or the '885 Referece or U.S. Patent No. 4,912,631 ("the '631 Reference") or the '196 Reference. Specifically, the '1182 Reference states that: |

| CLAIM | RESPONSE |
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| out after said location Ln is said location L1, such that during said operation while the contents of any location L to be read out other than the last location to be read out are being transferred from said plurality of sense amplifier circuits to said output, the contents of another location to be read out after said location L are being provided to said plurality of sense amplifier circuits for amplification and subsequent transfer to said output, and | "When the reading has finished to the column address 1023 in response to the above-mentioned address 4, the carrier signals ca for the column-type counter circuit (Y) are produced similarly to what is explained above, and they themselves will be the address 0 and the row-based address will be changed to 6." ['1182 Reference, Page 5, second column]<br><br>"(5) There is an effect that is obtained whereby high-speed continuous reading is carried out from a random address by incorporating address signals that have been supplied from the external terminal as initial values." ['1182 Reference, Page 6, second column]<br><br>"(6) Based on (1) to (5) above, there is an effect that is obtained whereby there can be provided a semiconductor memory device that is applicable to a semiconductor memory where picture element data that is large in quantity is repeated to depict high-precision picture images using a display device, such as a CRT, and, therefore, high-speed continuous reading would be presumed to be necessary." ['1182 Reference, Page 6, second column]<br><br>*See also* Figure 3 and accompanying description on Page 4.<br><br>The '494 Reference states:<br><br>"The selection of memory locations forming each cyclic pattern of addressing is controlled by the control unit 13. The row counter 45 and column counter 44 are connected so that unless instructed by the control 13 to do otherwise they count through successive addresses along each row and then row by row." ['494 Reference, Col. 8:22-27] |

| CLAIM | RESPONSE |
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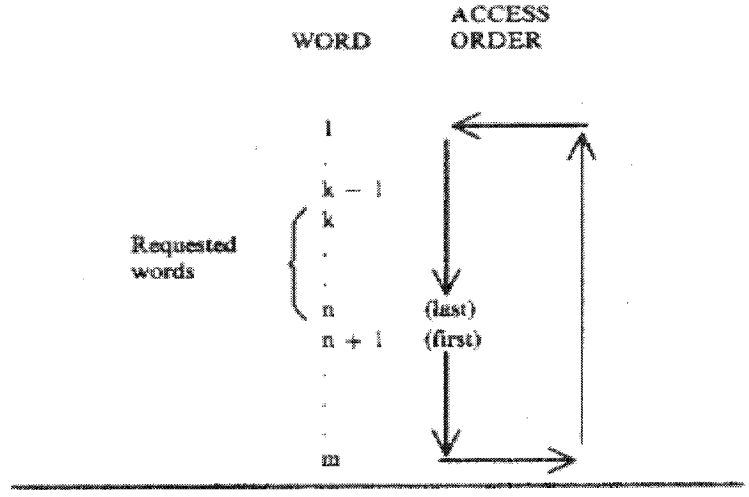
| | "Consequently after reaching address 0 the column and row counters cycle sequentially along each row for the two memory blocks in turn (starting at column zero of row 0 in array 0) using all memory locations in each row and then moving to the next row and repeating the operation." ['494 Reference, Col. 11:26-31]<br><br>"addressing sequentially more than one memory location in said first memory block and effecting a data transfer for each memory location addressed, and at the same time effecting an equate operation on bit lines in said second memory block; and after addressing memory locations in said first memory block, switching said addressing and equate operation so as to address sequentially more than one memory location in said second memory block and effecting a data transfer for each memory location addressed and at the same time equating bit lines in said first memory block." ['494 Reference, Col. 13:36-48]<br><br>The '885 Reference states:<br><br>"After the last memory address is reached, the access automatically rolls over to the first address." ['885 Reference, Col. 3:1-3]<br><br>"A method as in claim 5 wherein the sequence of incremented addresses wraps around when the address of the Nth register is reached such that all N registers in the array are read." ['885 Reference, Col. 7:45-48]<br><br>The '631 Reference states that:<br><br>"The above-described method is accomplished by utilizing two pieces of information, which are placed on the bus (23) by the GDP: the data word's offset and the number of words requested. The data word's offset |

| CLAIM | RESPONSE |
|---|---|
| | in the cache line is derived from adress bits 2 and 3 (00=word 1, 01=word 2, 10=word 3, and 11=word 4). The number of words being requested is obtained from the size bits 0 and 1 (00=1word, 01=2 words, 10=3 words, and 11=4words).<br><br>Using these two pieces of information, the following algorithm is executed:<br><br>FIRST WORD ACCESSED = PROCESSOR WORD ADDRESS + SIZE +1<br><br>The 1 is added to the size in order to yield the correct offset. For example, if the GDP requests two words at offset 01 in a four-word line, it is convereted to a wraparound request of four words to memory starting at word four [offset (01) + word count (01) + 1 = 11]." ['631 Reference, Col. 3:46-65]<br><br>See, '631 Reference, Table II: |

| CLAIM | RESPONSE |
|---|---|
| | TABLE II<br>  <br><br>See also, '631 Reference, Abstract, Table I, Fig. 3.<br><br>The '196 Reference states:<br><br>"In accordance with the present inventions, while a particular row is being accessed in one array, the corresponding bit liens in the other array are being precharged. Thus, as data is sequentially accessed along the one row and as the end of that row is reached, an immediate access can then occur to any row within the second array since the bit lines in that array will already have been initialized." '196 Reference, 2:60-67 |

| CLAIM | RESPONSE |
|---|---|
| | "In general, while one array is being accessed, the other array is being precharged (i.e., elevating the logic state of bit lines and settling transient signals) in preparation for the next access form such other array. Therefore, precharging tiems for one array overlap the time for performing read or write operation in the other array, and therefore do not limit operating speed." '196 Reference, 3:41-47 |
| wherein said memory further comprises a control circuit for selectively enabling said sense amplifier circuits so that said control circuit enables a sense amplifier circuit whose output signals are being transferred to the output of said memory but said control circuit does not enable all said sense amplifier circuits at the same time. | This limitation is met by the '1182 Reference alone or in combination with the '754 Reference or the '788 Reference or the '937 Reference or the '003 Reference or the '178 Reference. Specifically, the '1182 Reference states:<br><br>"In response to that, the operation timing signals Φ pa 1 and Φ pa 2 of the sense amplifiers SA 1 and SA 2, which are slower than the above-mentioned word line selection timing signals Φ x 1 and Φ x 2, are generated at the same time too." ['1182 Reference, Page 5, column 1]<br><br>*See also* Figure 1.<br><br>The '754 Reference states:<br><br>"In each operation cycle of the present invention, a plurality of sense amplifier circuits can be selected according to the content of a single bit of the address data, for example, and the rest of the plurality of sense amplifier circuits are kept in the non-active state. Therefore, charging/discharging currents will not flow through the data lines connected to those sense amplifier circuits which are in the non-active state, and total current consumption and current peaks in the entire |

| CLAIM | RESPONSE |
|---|---|
| | memory means are greatly reduced." ['754 Reference, Page 4:16-20]<br><br>"As mentioned above, in the dynamic memory device shown in Fig. 5, only the sense amplifier circuits 18-1 and 18-3 or the sense amplifier circuits 18-2 and 18-4 are activated, and the other row sense amplifier circuits are not activated." ['754 Reference, Page 5:56-58]<br><br>The '788 Reference states:<br><br>"According to this arrangement, only one plane is selected in accordance with the content of the upper-order two bits of the row address. The selected plane is activated and exhibits the memory operation but the rest of the planes which are under the non-selection state are inoperative. Therefore, the decoders and the sense amplifiers are inoperative in these inoperative planes and the memory is not refreshed. Therefore, power is consumed in only the selected plane and unnecessary power consumption in the other plane can be saved. Thus, the requirement for low power consumption can be satisfied." ['788 Reference, Col. 5:57-68.]<br><br>The '937 Reference states:<br><br>"The sense amplifier 86 is controlled by the signals $SE_{EV}$ to amplify the read data thereby to supply the same to the data latch 87, which in turn temporarily stores the outputs from the sense amplifiers 86. When the signals $SE_{EV}$ are at low levels, the data latch 87 is electrically cut off from the sense amplifier 86. Data from the data latch 87 are transferred to the output latch 89 when the signals $OE_{EV}$ are at high levels. In a similar manner, the sense amplifier 96 is controlled by the signals $SE_{OD}$ to amplify the read data thereby to supply the same to the data latch 97, which in turn temporarily stores the outputs from the sense amplifier 96. |

| CLAIM | RESPONSE |
|---|---|
| | When the signals $SE_{OD}$ are at low levels, the data latch 97 is electrically cut off from the sense amplifier 96." ['937 Reference, Col. 4:52-66]<br><br>The '003 Reference states:<br><br>"The flash memory control 88 also selectively enables one of two sets of bi-directional data buffers 90 and 91 which respectively couple the bank data buses 82 and 83 to the processor section data bus 63. The bank data buses 82 and 83 can be coupled to the instruction bus 61 by the flash memory control 88 selectively enabling buffers 92 and 93, respectively." ['003 Reference, Col. 9:21-27]<br><br>The '178 Reference states:<br><br>"Referring now to FIG. 2, the circuit of FIG. 1 has been modified to utilize the fact that, when RA10=1, only one half of the ARRAY BANKs 20 are being utilized and that, when RA10=0, the other half of the ARRAY BANKs 20 are being utilized. In particular, the RA 10 address is used to cause only the half of the ARRAY BANKs 20 that are being utilized to draw power from the DRAM energy source during read/write operations, while at the same time permitting the periodic performance of the refresh cycle in the usual manner on all ARRAY BANKs." ['178 Reference, Col. 3:32-42] |
| 9. The memory of claim 8 wherein, during said operation, said control circuit enables at the same time only: | |
| (1) the sense amplifier circuit whose output signals are | This limitation is met by the '1182 Reference alone or in combination |