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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

ADVANCED MICRO DEVICES, INC., et al.,

Plaintiffs,

v.

SAMSUNG ELECTRONICS CO., LTD., et al.,

Defendants.

Case No. CV-08-0986-SI

PLAINTIFFS' OPENING CLAIM CONSTRUCTION BRIEF

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INTRODUCTION

Plaintiffs Advanced Micro Devices, Inc. and ATI Technologies ULC (collectively "AMD") have accused Defendants Samsung Electronic Co., Ltd., Samsung Semiconductor, Inc., Samsung Austin Semiconductor, LLC, Samsung Electronics America, Inc., Samsung Telecommunications America, LLC, Samsung Techwin Co., Ltd., and Samsung Opto-Electronics America, Inc. (collectively "Samsung") of infringing seven AMD patents: U.S. Patent Nos. 5,559,990 ("'990"), 5,248,893 ("'893"), 4,737,830 ("'830"), 5,545,592 ("'592"), 5,623,434 ("'434"), 5,377,200 ("'200"), and 6,784,879 ("'879"). Six of those seven patents (all except '592) now are before the Court for construction of claim terms.

AMD's '990, '893, and '830 patents relate to memory. The '434 and '200 patents disclose and claim improved technology for processors. Finally, the '879 patent claims a processing unit and programming instructions for a valuable graphical user interface for controlling video in electronic devices.

AMD submits that each claim term at issue should be given the scope reflected in the claim language, unless the intrinsic record explicitly and unambiguously puts those of skill in the art on notice that a term has a more limited or more expansive scope. AMD respectfully requests that the Court construe each term according to AMD's proposed construction.

ARGUMENT

I. CLAIM CONSTRUCTION LEGAL PRINCIPLES

Claim construction is a matter of law for the Court. *Cybor Corp. v. FAS Techs., Inc.*, 138 F.3d 1448, 1456 (Fed. Cir. 1998). The inquiry begins with the words of the claims themselves. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1314 (Fed. Cir. 2005). The use of the terms in the context of the claims "can be highly instructive." *Id.* Claim differentiation raises a presumption that the construction of terms should not result in claims with identical scope. *Halliburton Energy Services, Inc. v. M-I LLC*, 514 F.3d 1244, 1251 n.3 (Fed. Cir. 2008). Terms that appear in multiple claims generally should be given the same meaning. *Phillips*, 415 F.3d at 1314.

The specification provides context for claim construction, but preferred embodiments from the specification should not be read into the claims without an express definition or

disclaimer in the intrinsic record. *Phillips*, 415 F.3d at 1316, 1323. To disclaim claim scope, the specification must use "words of manifest exclusion," *Teleflex, Inc. v. Ficosa N. Am. Corp.*, 299 F.3d 1313, 1325-26 (Fed. Cir. 2002), or "unequivocally preclude" embodiments that otherwise would be within the ordinary meaning of the claim terms. *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1346 (Fed. Cir. 2008). A definition of a claim term in the specification must clearly reflect an intent to limit the claims. *Helmsderfer v. Bobrick Washroom Equip., Inc.*, 527 F.3d 1379, 1381 (Fed. Cir. 2008).

A proposed construction that excludes all preferred embodiments from the claims generally cannot be correct. *Oatey Co. v. IPS Corp.*, 514 F.3d 1271, 1277 (Fed. Cir. 2008). The purpose or objective of the invention also may be considered. *Osram GmbH v. U.S. Int'l Trade Comm'n*, 505 F.3d 1351, 1358 (Fed. Cir. 2007). Specifically, a claim term should not be construed in a way that contradicts or defeats the purpose of the invention. *Id.*

Statements made by the applicant during prosecution may rise to the level of a disclaimer if they expressly and clearly exclude embodiments from the scope of the claims. *Voda v. Cordis Corp.*, 536 F.3d 1311, 1321 (Fed. Cir. 2008). The Court may consider prior art cited during prosecution as part of the intrinsic record to provide context for the meaning of terms in the art. *V-Formation, Inc. v. Benetton Group SpA*, 401 F.3d 1307, 1311 (Fed. Cir. 2005).

Expert testimony and dictionary definitions may assist the Court in understanding how one of ordinary skill in the art would understand the claim terms. *Phillips*, 415 F.3d at 1318. Inventor testimony, however, generally does not carry weight for claim construction. *Howmedica Osteonics Corp. v. Wright Med. Tech., Inc.*, 540 F.3d 1337, 1347 (Fed. Cir. 2008).

II. THE CHENG '990 PATENT

A. Description of the Invention

The Cheng '990 patent describes improvements to computer memory. Memory in a computer stores and provides data to a processor or other device that requests it. Declaration of Andrew Wolfe ("Wolfe Decl.") ¶18. The '990 patent describes a memory with dedicated circuitry for each of its subarrays that enhances the performance of memory by providing for (1) high-performance burst modes, and (2) selective enabling of sense amplifiers. *Id.*

Generally, memory is comprised of an array of memory locations divided into rows and columns, and circuitry such as registers, decoders, and sense amplifiers for accessing these locations. *Id*. The registers and decoders are responsible for processing the address of a data request to identify its location in the array. *Id.* The sense amplifiers "amplify" the contents of that location for output from the sense amplifier, and eventual output to the requesting device. *Id*. The array and the circuitry can be formed as a single integrated circuit or as a plurality of integrated circuits. *Id*.

Some claims of the '990 patent improve memory performance by dividing the array of memory locations into a plurality of subarrays, each with circuitry dedicated solely to it. Thus, each subarray has its own set of registers, decoders, sense amplifiers and other circuitry. Because each subarray has dedicated circuitry, each subarray can act independently but in coordination with another subarray to provide two significant performance enhancements.

First, the dedicated circuitry provides for high-performance burst modes that can output data more quickly than traditional burst modes. While some claims require a high-performance burst mode, others do not.

The dedicated circuitry also provides for selective sense amplifier enablement: while some sense amplifiers are enabled to output data, others are disabled. Because sense amplifiers consume large amounts of power, this feature of the '990 patent results in significant power savings. Again, some claims require structure for selectively enabling sense amplifier enablement while others do not.

B. "Integrated Memory" Is a Limitation That Requires the Memory To Be Formed As a Single Integrated Circuit.

"Integrated memory" (asserted claims 20, 22-23)	
AMD's Construction	**Samsung's Construction**
"A memory fabricated in a single integrated circuit."	This is part of the preamble and is not a limitation. Were a construction required, the proposed construction is: "A memory containing one or more integrated circuits."

AMD has proposed "integrated memory" for construction. The term "integrated memory," which appears in the preamble to claim 20, is a limitation of the claim that means "a memory fabricated in a single integrated circuit." Samsung argues that the phrase is not a limitation and, although Samsung agrees the term relates to integrated circuits, that it should be construed as a memory containing one or more integrated circuits. Thus, the issues for the Court are: (1) does the term "integrated memory" mean a memory fabricated in a single integrated circuit; and (2) is "integrated memory" a limitation on claim 20. The answer to each of these questions is "yes."

1. "Integrated Memory" Means a Memory Formed as a Single Integrated Circuit.

The '990 patent claims demonstrate that the patentee intended "integrated circuit" and "integrated memory" to mean a single integrated circuit. *See Phillips,* 415 F.3d at 1314 ("Differences among claims can also be a useful guide in understanding the meaning of particular claim terms."). Claim 1 of the '990 patent recites "a memory." Claim 6 recites "[t]he memory of claim 1 wherein the memory is fabricated in an integrated circuit." Claims 8 and 14 read similarly. As a result, the memory in claims 1 and 8 encompasses memory fabricated in *one or more* integrated circuits, whereas the memory in claims 6 and 14 encompasses only memory fabricated in *one* integrated circuit. Wolfe Decl. ¶26.

The "integrated memory" of claim 20 must also encompass only memory fabricated in one integrated circuit in order to give meaning to all terms in the claim. *See Merck & Co., Inc. v. Teva Pharms. USA, Inc.*, 395 F.3d 1364, 1372 (Fed. Cir. 2005) ("*Merck II*") (observing that constructions giving meaning to all terms of a claim are preferred). Because the "memory" of claim 1 can be one or more integrated circuits, the "integrated memory" of claim 20 must mean something else; otherwise the term "integrated" is superfluous. In this case, "integrated memory" means memory fabricated in a single integrated circuit.

The specification provides further support for this conclusion, stating: "some embodiments are not integrated into *one integrated circuit*." '990 at 13:7-10 (emphasis added)

(Ex. A).[1] The specification also refers to "the" integrated circuit. *Id.* at 7:16-18. Thus, when the patent limits claim scope to memories fabricated in an integrated circuit, it means "one integrated circuit." *See Freescale Semiconductor, Inc. v. Promos Techs., Inc.*, 561 F. Supp. 2d 732, 749 (E.D. Tex. 2008) (holding that "an integrated circuit" meant "a single integrated circuit" where patentee indicated that the invention was implemented in a "single integrated circuit"). Thus, the patentee here has indicated that "integrated circuit" and "integrated memory" mean "one integrated circuit." '990 at 13:7-10 (Ex. A).

The general presumption that the "indefinite article 'a' or 'an' in patent parlance carries the meaning of 'one or more'" arises from the "use of the transition 'comprising' in conjunction with the article 'a' or 'an.'" *Scanner Techs. Corp. v. ICOS Vision Sys. Corp.*, 365 F.3d 1299, 1305-06 (Fed. Cir. 2004). In the absence of the transition "comprising," one must look to the specification for some indication that the patentee "intended it to have other than its *normal singular meaning*." *N. Am. Vaccine, Inc. v. Am. Cyanamid Co.*, 7 F.3d 1571, 1575-76 (Fed. Cir. 1993) (emphasis added) (holding that "a" did not mean "one or more" in claim without transition "comprising"). No such indication exists here. The intrinsic record consistently supports the presumption that the article "a" or "an" should be given its "normal singular meaning." *Id.* Thus, to give meaning to all claim terms and to the specification's descriptions of embodiments of the invention, "integrated memory" must mean a memory fabricated in a single integrated circuit.

2. "Integrated Memory" Is a Limitation in Claim 20.

In claim 20, "integrated memory" is used intentionally and adds important structure to the claim. *Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 808-09 (Fed. Cir. 2002) (explaining that preamble that does more than merely describe structurally complete invention limits claim). As shown above, comparison of the preambles to independent claims 1 and 8 on the one hand and claim 20 on the other establishes that "integrated memory" means a memory fabricated in a single integrated circuit. Also, the addition of "integrated" signifies to one of ordinary skill that the "integrated memory" of claim 20 requires the memory to be fabricated in a

[1] Citations to "Ex. __" refer to exhibits attached to the Declaration of Aaron R. Fahrenkrog in Support of Plaintiffs' Opening Claim Construction Brief, submitted with this brief.

single integrated circuit, whereas the "memory" of claims 1 and 8 does not. Wolfe Decl. ¶27.

"Integrated memory" is not merely a descriptive name given "to the set of limitations in the body of the claim that completely set forth the invention." *IMS Tech., Inc. v. Haas Automation, Inc.*, 206 F.3d 1422, 1434 (Fed. Cir. 2000). The body of claim 20 does not completely set forth the invention: "integrated" does not appear anywhere other than the preamble, and the claim elements could be found in a combination of one or more integrated circuits. Wolfe Decl. ¶27. Thus, a single integrated circuit is not inherent to the remaining claim elements. *Id.* Instead, "integrated memory" is the structure in which the claimed limitations must be present. *Freescale*, 561 F. Supp. 2d at 749. "Integrated memory" is "a fundamental characteristic of the claimed invention that is properly construed as a limitation of the claim itself." *Poly-America, L.P. v. GSE Lining Tech., Inc.*, 383 F.3d 1303, 1310 (Fed. Cir. 2004).

The specification explains that whether the claimed memory is formed as a single integrated circuit is an important structural feature of the invention. The specification states that "some embodiments are not integrated into one integrated circuit." '990 at 13:7-10 (Ex. A); *see Catalina Mktg.*, 289 F.3d at 808 ("[W]hen reciting additional structure or steps underscored as important by the specification, the preamble may operate as a claim limitation."); *Negotiated Data Solutions, LLC v. Dell, Inc.*, __ F. Supp. 2d __, 2009 WL 186180 at *18-19 (E.D. Tex. Jan. 16, 2009) (finding "integrated circuit" provided limiting structure when used in preamble to a claim); *Freescale*, 561 F. Supp. 2d at 749 (same). Furthermore, one of the preferred embodiments in the '990 patent is specifically identified as an integrated circuit. '990 at 7:8-18 (Ex. A). *See Negotiated Data*, __ F. Supp. 2d at *18 (noting that patentee uses "integrated circuit" to "describe the preferred embodiment"). "Integrated memory" is a claim limitation.

C. AMD's Construction of "Burst Mode Operation" Is Taken Verbatim From the Patentee's Argument to Overcome Prior Art During Prosecution.

"Burst mode," "Burst mode operation," and "Burst mode read operation" (asserted claims 1-14, 20, 22-23)	
AMD's Construction	**Samsung's Construction**
For "burst mode" (claims 1, 8, 20): "A serial transfer mode in which a memory transfers the contents of a plurality of locations in response to the address of one location." For "burst mode operation" and "burst mode read operation" (claims 8, 20): "A serial transfer in which the contents of a plurality of locations are provided in response to the address of one location."	For "burst mode," "burst mode operation" and "burst mode read operation" (claims 1, 8, 20): A mode for sequentially accessing memory locations in which the memory receives the address of one memory location and provides in response the contents of a plurality of consecutive memory locations.

AMD's constructions of the phrases "burst mode," "burst mode operation," and "burst mode read operation" are correct because they are based on an argument the patentee made to the examiner in an attempt to overcome prior art. Samsung, which proposed these phrases for construction, also draws its proposed construction from the intrinsic record. Samsung's construction is incorrect, however, because it is taken from a general, less-probative statement, and is open to an interpretation that does not comport with the claims or the specification.

"Arguments and amendments made during the prosecution of a patent application and other aspects of the prosecution history . . . must be examined to determine the meaning of terms in the claims." *Southwall Techs., Inc. v. Cardinal IG Co.*, 54 F.3d 1570, 1576 (Fed. Cir. 1995). AMD's construction of "burst mode" is taken verbatim from a patentee argument in the '990 patent file history. The patent examiner initially rejected claims in the '990 patent as being anticipated by U.S. Patent No. 4,636,986. Office Action, Jan. 26, 1995, at 3 (Ex. G). The examiner stated that "burst mode . . . as claimed in the instant invention . . . is nothing more than a beginning mode address and an ending address which is equivalent to a serial transfer[2] of

[2] A serial transfer outputs several memory locations one at a time. Wolfe Decl. ¶31. In contrast, a block transfer outputs several memory locations simultaneously. *Id.*

information of which the reference teaches burst mode transfer to the extent of the claims." *Id*. (footnote added). In arguing to overcome the rejection, the patentees asserted that "burst mode . . . is not any serial transfer but *a serial transfer in which the contents of a plurality of locations are provided in response to the address of one location*." Amendment, Apr. 27, 1995, at 4 (emphasis added) (Ex. H). Because the patentee used the exact same language in arguing for patentability, AMD's construction defines what "burst mode" means in the context of the '990 patent. *See, e.g.*, *N. Am. Container, Inc. v. Plastipak Packaging, Inc.*, 415 F.3d 1335, 1344-46 (Fed. Cir. 2005) (holding that arguments made during prosecution to overcome prior art can both limit claim scope and override general rules of claim construction); Wolfe Decl. ¶32.

Samsung's construction was not presented as an argument in response to a rejection but instead was lifted from a general description contained in the introductory section to the patentee's appeal brief. Appeal Brief, Sept. 27, 1995, at 2 (Ex. I). As such, it is to be accorded little probative effect as to the meaning of the term.

Furthermore, Samsung's proposed construction is at odds with the '990 patent claims. Samsung's proposed construction calls for the memory to output a plurality of "consecutive memory locations." The phrase "consecutive memory locations" is not found in any claim. Instead, the claims refer to "consecutive addresses." To the extent that Samsung's construction suggests physically consecutive memory locations, it is unsupported by the claims and contradicted by the specification of the '990 patent. '990 at 2:16-37; claims 1, 8, 20 (Ex. A).

D. "Consecutive Addresses" Should Not Include a Limitation That Is Directly Contradicted by the Specification.

"Consecutive addresses" (asserted claims 1-14, 20, 22-23)	
AMD's Construction	**Samsung's Construction**
"Consecutive addresses" and its variations need no construction and should be given their ordinary meaning.	"Consecutive addresses" and its variations require construction.
For "consecutive addresses" (claims 1, 8, 20): "Addresses following one after the other in order." For "memory locations L1, . . . Ln" (claim 8): "Locations corresponding to addresses following one after the other in order." For "locations L1 and L2" (claim 1): "Two locations corresponding to addresses following one after the other in order."	For "consecutive addresses," "memory locations L1, . . . Ln," and "locations L1 and L2" (claims 1, 8, 20): A set of addresses following one after the other in order from L1 to Ln wherein each memory location represents a memory cell that is associated with a single address.

These terms need no construction and should be given their ordinarily understood meaning because the specification does not indicate that they are used in a unique or special way. *Hazani v. United States Int'l Trade Comm'n*, 126 F.3d 1473, 1480 (Fed. Cir. 1997). Alternatively, AMD's construction is proper because it is consistent with the intrinsic record. Indeed, Samsung, which has proposed the phrases for construction, agrees that "consecutive" means "following one after the other in order." Samsung adds a vague "wherein" clause that imposes limitations that are directly contradicted by the specification.

Samsung's added limitation that "each memory location represents a cell that is associated with a single address" contradicts the specification's statement that, "[i]n some embodiments, each memory location M-i includes several memory cells, for example, eight cells as in FIG. 5." '990 at 6:10-12 (Ex. A). In the context of this patent, a cell is only one bit of memory. Wolfe Decl. ¶36. The specification further explains that the memory described in FIGS. 8-28 incorporates 8-bit memory locations. '990 at 7:5-10 (Ex. A). Thus, Samsung's requested limitation that each memory location has only one cell cannot be correct.

Samsung's proposed construction also contains the limitation that the addresses proceed

from L1 to Ln. This limitation is wrong because claim 20 does not refer to any particular set of locations, and claim 1 refers only to the addresses L1 and L2. The limitation also is incompatible with claim 1. Changing claim 1's limited set L1 to L2, to the unlimited set L1 to Ln, improperly narrows the claim scope. Claim 1 recites limitations that apply to L1 and L2, but Samsung's construction requires those limitations to apply to the unlimited set L1 to Ln. Accordingly, the construction of "consecutive addresses" is "addresses following one after the other in order."

E. AMD's Construction of "Enable / Disable" Is Correct Because It Does Not Import Limitations on Unrecited Sense Amplifiers.

"Enabling" and "Disabling" of "Sense Amplifiers" (asserted claims 3, 8, 23)	
AMD's Construction	**Samsung's Construction**
For "sense amplifiers . . . are enabled/disabled" (claim 3): "Sense amplifiers are enabled when they are selected to develop a signal on their outputs, and are disabled when they are not selected to develop a signal on their outputs." For "control circuit for selectively enabling / "control circuit enables" (claims 8, 23): "a circuit that selects sense amplifier circuits to develop a signal on their outputs"	For "sense amplifiers . . . are enabled/disabled" / "control circuit enables" (claims 3 and 23): Developing a signal on the output of a sense amplifier only when it is transferring data from its output to the memory output, and not developing a signal on the output of a sense amplifier when data is being transferred from a memory location to the sense amplifier. For "control circuit for selectively enabling" (claim 8): Developing a signal on the output of a sense amplifier only when it is transferring data from its output to the memory output or developing a signal on the outputs of a predetermined number of sense amplifiers whose outputs are to be transferred to the memory output immediately after the currently enabled sense amplifier transfers its data to the memory output, and not developing a signal on the output of the remaining amplifiers to which data is being transferred from memory locations to the sense amplifiers.

Samsung selected these phrases for construction as a single term. Accordingly, AMD's constructions of these phrases focus on the element common to each: enabling and disabling sense amplifiers. A sense amplifier is enabled when it is selected to develop a signal on its output; it is disabled when it is not selected to develop a signal on its output. This construction

applies consistently across all claims. In contrast, Samsung proposes unacceptably vague constructions that narrow claim scope and exclude a preferred embodiment. Thus, the Court must decide whether to adopt a construction that restricts the enable/disable status of sense amplifiers that the claims intentionally do not restrict.

"The appropriate starting point . . . is always with the language of the asserted claim itself." *Comark Commc'ns, Inc. v. Harris Corp.*, 156 F.3d 1182, 1186 (Fed. Cir. 1998). The relevant portions of claims 3, 8, and 23 yield the following straightforward results:

Claim 3 Language	**Sense Amplifier (SA) Status**
"[T]he sense amplifiers from which the contents of said location L1 are being transferred are enabled . . ."	The SA for location L1 is enabled.
"[T]he sense amplifiers to which the contents of said location L2 are being transferred are disabled . . ."	The SA for location L2 is disabled.
	The claim places no restrictions on any other sense amplifiers: they could be all enabled, all disabled, or some enabled and some disabled.

Claim 8 Language	**Sense Amplifier (SA) Status**
"[S]aid control circuit enables a sense amplifier circuit whose output signals are being transferred to the output of said memory but . . ."	The control circuit enables at least the SA providing data to the memory output.
"[S]aid control circuit does not enable all said sense amplifier circuits at the same time."	The control circuit disables at least one SA not selected to provide data to the memory output.
	The claim places no restrictions on any other sense amplifiers: they could be all enabled, all disabled, or some enabled and some disabled.

Claim 23 Language	**Sense Amplifier (SA) Status**
"[T]he control circuit enables the sense amplifier circuit selected to provide data to the memory output and . . ."	The control circuit enables at least the SA selected to provide data to the memory output.
"[T]he control circuit . . . at the same time disables one or more sense amplifier circuits	The control circuit disables at least one SA not selected to provide data to the memory

not selected to provide data to the memory output."	output.
	The claim places no restrictions on any other sense amplifiers: they could be all enabled, all disabled, or some enabled and some disabled.

Although each claim uses slightly different phrasing, the results are the same: during a burst mode operation at least one sense amplifier is enabled, at least one sense amplifier is disabled, and the claims do not include limitations regarding the existence or status of any other sense amplifiers. That is consistent with the specification and a preferred embodiment detailed by the patentee. '990 at 5:49-61 (Ex. A); s*ee Merck & Co., Inc. v. Teva Pharms. USA, Inc.*, 347 F.3d 1367, 1371 (Fed. Cir. 2003) ("*Merck I*").

AMD's constructions preserve the selective enabling and disabling of sense amplifiers as described in the claims. AMD construes only what is necessary: what it means to enable and disable sense amplifiers. AMD does not construe more because the remaining claim language is clear on its face, and doing so would render portions of that language redundant. *See Merck II*, 395 F.3d at 1372 (preferring constructions that do not render claim terms superfluous). That AMD's constructions apply consistently across claims 3, 8 and 23 verifies the correctness of this approach. *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1119 (Fed. Cir. 2004).

AMD's constructions are also correct because they come from the specification. *See Phillips,* 415 F.3d at 1316 (observing that "the specification necessarily informs the proper construction of the claims"). The specification states: "[w]hen line 350.L-i is low, *the sense amplifier circuit* 350.L-i *is enabled to develop the signal on its output*." '990 at 11:24-26 (emphasis added) (Ex. A). Enablement occurs when the sense amplifier is selected: the specification explains that sense amplifiers are enabled to allow them "sufficient time to develop their output signals" before transferring data. *Id.* at 5:50-54. Because a sense amplifier can have only two states, enabled or disabled, a sense amplifier is disabled when it is not selected to develop a signal on its output. Wolfe Decl. ¶38.

Placed in claims 3, 8 and 23, AMD's constructions do not alter the effects of the claim

language shown in the tables above: during a burst mode operation at least one sense amplifier is enabled, at least one sense amplifier is disabled, and the existence of or status required for any other sense amplifiers is unrestricted.

In contrast, Samsung's constructions narrow claims 3, 8 and 23 by (1) adding limitations found nowhere in the patent, and (2) importing limitations from other claims. *See Broadcom Corp. v. Qualcomm, Inc.*, 543 F.3d 683, 689 (Fed. Cir. 2008) (observing that it is improper to limit claim to unclaimed features); *SRI, Int'l v. Matsushita Elec. Corp. of Am.*, 775 F.2d 1107, 1122 (Fed. Cir. 1985) (finding that it is error as a matter of law to import limitations from one claim into another). Samsung's constructions require certain sense amplifiers to be enabled or disabled, when the claims do not restrict the status of those sense amplifiers. Such limitations contradict the claim language and exclude an embodiment detailed in the specification. '990 at 5:45-61 (Ex. A). Samsung also imports limitations from at least one dependent claim into an independent claim. Consequently, Samsung's constructions cannot be correct.

III. THE SAKAMOTO '893 PATENT

A. Description of the Invention

1. Insulated Gate Field Effect Devices

The '893 patent relates to insulated gate field effect devices (also known as Metal Oxide Semiconductor Field Effect Devices, or "MOSFETs"). MOSFETs function as transistors in integrated circuits. Declaration of Jack Lee ("Lee Decl.") ¶8. In integrated circuits, a MOSFET can operate as a switch, being "on" when current is able to pass through it from the source to the drain, and "off" when no current should pass through. Lee Decl. ¶10. A useful analogy is to compare a MOSFET to a water spigot. The "source" is the pipe leading to the spigot, the drain is the water outlet from the spigot, and the gate is the valve that turns the water on or off. When the spigot (or gate) is turned off, no water (or current) flows through the device. *Id.*

An example of a MOSFET is shown in Figure 9 of the patent. Paragraph 9 of the Lee Declaration depicts a colored version of Figure 9 with additional labels. The key components include the source and drain, which are found in the substrate of the integrated circuit, an insulating layer formed on the substrate, and a gate formed on the insulating layer.

2. Fabrication and Structure of MOSFETs

A process called "doping" plays a key role in MOSFET fabrication. Doping refers to the process of treating parts of the integrated circuit with various chemicals, known as "impurities," to increase the number of charge carriers. Lee Decl. ¶11. N-type doping increases the number of one type of charge carrier (electrons), whereas P-type doping increases the number of a different type of charge carrier (holes). *Id.*

In the example MOSFET shown in Lee Decl. ¶9, the gate, source and drain have P-type doping, whereas the substrate beneath the gate and between the source and drain has N-type doping. The area at the border between the source/drain and the substrate becomes depleted of carriers (such as holes) that can carry current from the source to the drain. Lee Decl. ¶12. Similarly, the area at the border between the gate and the substrate also becomes depleted of carriers. *Id.* These areas without carriers are known as "depletion zones." *Id.* These zones are identified in the figure at Lee Decl. ¶9. These depletion zones prevent current from flowing from the source to the drain. Lee Decl. ¶12. The transistor is in an "off" state because there is no channel between the source and the drain through which the current can flow. *Id.* In other words, the transistor does not conduct current. *Id.*

The transistor is "on" when current can flow from the source to the drain. Lee Decl. ¶13. To accomplish this, voltage is applied to the gate and drain. *Id.* This "operating voltage" creates two electric fields. *Id.* One field (a vertical field) pulls carriers to the surface of the substrate under the insulation layer. Lee Decl. ¶¶13-14 (description and figure illustrating vertical field). These carriers can carry current, but need a second force to pull them in either direction. Lee Decl. ¶13. This force is provided by the second electric field, a horizontal field that pulls current from the source to the drain. Lee Decl. ¶¶13-15 (description and figure illustrating horizontal field). Carriers are pulled to an area near the gate and between the source and drain, known as a "channel." Lee Decl. ¶¶16, 18 (description and figure illustrating channel). The channel disappears near the drain. Lee Decl. ¶16. However, carriers (and therefore current) can make it through to the drain because the area without a channel is very small and the horizontal electric field is very strong. *Id.* The area without a channel that can conduct current when the transistor

is turned "on," even though the channel disappears, is known as a "pinch-off region," (Lee Decl. ¶16), and is identified as "Lg1." '893 at Fig. 4 (Ex. B); *see also* Lee Decl. ¶9.

3. Improvements Claimed by the '893 Patent

The '893 patent claims a MOSFET with a particular structure. Specifically, it includes a recessed, or concave, area where the insulating layer and gate dip down into the substrate. '893 at 6:1-9 (Ex. B). The recessed area is curved at least in part. *Id.* at 6:21-27. Figure 4 depicts an embodiment of the claimed transistor. A colored version with additional labeling is found at Lee Decl. ¶18. The claimed invention dramatically improves MOSFETs by making the effective channel length longer. '893 at 4:3-37 (Ex. B). Thus, MOSFETs can be made smaller without some of the negative side effects presented by shrinking the distance between the source and drain. Lee Decl. ¶17.

B. AMD Accepts Samsung's Construction of "Self-aligned to the Respective First and Second Opposed Sides of the Gate."

AMD accepts Samsung's proposed construction. Accordingly, the claim term "self-aligned to the respective first and second opposed sides of the gate" shall now mean "formed by a process in which the gate is used as a mask during source and drain implantation."

C. Samsung Accepts AMD's Construction of "The Depth of Said First and Second Impurity Regions."

Samsung accepts AMD's proposed construction. Accordingly, the claim term shall now mean "the depth of the source and drain regions." *See* Ex. P.

D. "Channel-free" Means "Without a Channel."

"Channel-free region" and "Channel-free zone" (asserted claims 1, 2, 4)	
AMD's Construction	**Samsung's Construction**
"The terms 'channel-free region' and 'channel-free zone' refer to areas where there is no channel."	"A portion of the substrate without an inversion region/zone and that conducts current."

The crux of this dispute is whether the channel-free area must conduct current. The parties also disagree whether "channel-free" areas should be described in simple terms as areas

without a channel (as AMD urges) or by introducing additional jargon regarding "inversion regions" (as Samsung urges).

AMD's construction is simple, readily understood by a jury, and reflects ordinary meaning. As a matter of plain English, "channel-free regions" and "channel-free zones" refer to areas where there is no channel.

The specification uses "channel-free" in a manner that is consistent with the common, ordinary meaning. Figure 9 identifies an area of the substrate labeled as "Lg1" as a "channel-free length." '893 at 3:24-26; Fig. 9 (Ex. B). In the text of the specification corresponding to this figure, it states that "between one end of the channel region 13 and the drain 5, there is a region of a length Lg1 *without a channel* being formed therein." *Id.* at 2:6-8 (emphasis added). Thus, the specification equates the term "channel-free" with being "without a channel."

Samsung apparently agrees that the area in question is without a channel (although it refers to the area as being without an "inversion region") but incorrectly adds the words "that conducts current" to the end of its construction. By requiring that the channel-free area conduct current, Samsung limits the scope of the claims to transistors in the turned-on state. As explained above, there is a small channel-free area in the turned-on state that conducts current (also known as a "pinch-off region"). *See* pp. 14-15, *supra*. Samsung excludes the turned-off state, where the channel-free region (the entire area beneath the gate and between the source and drain) does not conduct current, from the scope of the claims. *See* p. 14, *supra*.

Samsung's narrow construction is inconsistent with the claims. *See Phillips*, 415 F.3d at 1312 (describing primacy of claim language in claim construction). In particular, claim 4 recites a "channel-free zone" that develops when the transistor is "in the turned *off* state." '893 at 6:13-20 (Ex. B). In other words, claim 4 specifically includes the area under the gate and between the source and drain that does *not* conduct current when the transistor is turned off. Therefore, the term "channel-free" cannot be limited to an area that exists only in a transistor that is turned *on*.

Nothing in the intrinsic record undermines or disclaims the plain language of claim 4. The specification describes the pinch-off region in the "on" state of the device (that conducts current) as "channel free." S*ee* '893 at Fig. 9 (using term "Channel-Free Length"), 1:67-2:3

(explaining that Figure 9 shows status "when operating voltage is supplied") (Ex. B). There are no statements, much less an unequivocal statement, disclaiming channel-free areas that do not conduct current. Thus, nothing in the intrinsic suggests that the "channel-free" area is limited to one that conducts current in the turned-on state.

Finally, Samsung substitutes "inversion zone" for the term "channel." First, the term "inversion zone" is not used in the patent, so it introduces additional technical jargon that has no meaning to lay jurors. Second, Samsung's new term creates confusion because other parts of the asserted claims refer to the "channel." '893 at 6:13-16 ("a channel-region formed between the source and drain regions, for defining a channel that conducts current") (Ex. B). It is confusing to refer to a "channel" in one part of a claim and refer to the absence of a channel using a different term.

IV. THE PATEL '830 PATENT

A. Description of the Invention

The '830 patent relates to the field of decoupling capacitors. A decoupling capacitor is a device that reduces voltage spikes in electronic circuits. Declaration of Eby Friedman ("Friedman Decl.") ¶11. Voltage spikes occur when there are changes in the amount of current in the power lines (busses) of electronic systems. *Id.* This behavior is particularly problematic in modern integrated circuits, where faster switching speeds exacerbate voltage spikes, leading to malfunctions in circuit logic. *Id.* The capacitors act as reservoirs of charge to smooth out the effect of changes in current. *Id.*

Capacitors are made up of three components: a top plate, a middle layer of insulation, and a bottom plate. A diagram illustrating these three components is found in the left hand side of Friedman Decl. ¶13.

The '830 patent claims significant improvements to the concept of using capacitors to reduce voltage spikes. In particular, it describes such capacitors as being at the substrate level (under the busses). '830 at 6:20-29 (Ex. C). Claim 1 describes the structure of the capacitor as being similar to that of a MOSFET. The bottom plate of the capacitor is a doped region of the substrate. *Id.* at 6:27-29. The top plate is known as a "gate electrode." *Id.* at 6:22-23. The

insulation between the two is referred to as "gate oxide." *Id.* at 6:29-31. A diagram illustrating these components is depicted in the right hand side of Friedman Decl. ¶13.

Claim 5 describes an improvement that is of particular importance. It discloses an embodiment wherein the gate electrode of claim 1 is "divided into a plurality of segments and each of said segments is independently connected electrically" to one of the said busses. '830 at 6:54-56 (Ex. C). This segmented gate is one of the key innovations disclosed by the '830 patent because it reduces electrical resistance and creates redundancy that allows the capacitor to continue to operate even if one segment suffers a fabrication defect or burns out. *Id.* at 5:26-43.

AMD previously asserted the '830 patent in this district in *Oki Am., Inc. v. Advanced Micro Devices, Inc.*, No. C-04-03171-CRB. The parties litigated the validity of claims 1-6. In a "Memorandum and Order" filed November 13, 2006 ("*Oki* Order") (Breyer, J.) (Ex. K), this Court ruled on summary judgment that claims 1-4 were invalid, but declined to find claims 5 and 6 invalid. Here, AMD is asserting only claims 5 and 6. Some of the claim terms were construed in the context of the summary judgment order. *Id.*

B. "Gate Electrode . . . Is Divided into a Plurality of Segments" Means the Segments Must Share a Common Doped Region.

"Gate electrode . . . is divided into a plurality of segments" (asserted claim 5)	
AMD's Construction	**Samsung's Construction**
"For each doped region (lower plate), the gate electrode (upper plate) is divided into a plurality of segments."	"In the improved integrated circuit structure of claim 1, the gate electrode is divided into two or more separate gate electrode segments."

AMD proposes exactly the same construction for this term as the one adopted by this Court in the *Oki* Order:

> First, [claims 5 and 6] do not simply require, as Oki primarily contends, a plurality of MOS capacitors as recited in claim 1; instead, the claims introduce a limitation wherein <u>for each doped region (lower plate), the gate electrode (upper plate) is divided into a plurality of segments</u>, and each is separately wired to the bus. '830 at 6:53-58.

Oki Order at 12 (emphasis added) (Ex. K).

The *Oki* Court's construction should be adopted in this case, because it explains that the gate segments identified in claim 5 must share a common doped region. The concept of a gate electrode divided into "segments" has meaning only if those segments share a common doped region. Friedman Decl. ¶18. If each gate segment had its own doped region, there would simply be a collection of individual capacitors, each containing separate top and bottom plates separated by insulation. *Id.* The word "segment" would lose all meaning in the context of the claim. *Id.*

To illustrate this point, the figure in the top portion of Friedman Decl. ¶19 depicts gate segments sharing a common doped region and the bottom portion illustrates various gates, each paired with their own doped region of the substrate (*i.e.*, separate capacitors). Only the top portion could be referred to as having "segmented" gates. Friedman Decl. ¶19.

If the purpose of claim 5 were simply to require a plurality of individual capacitors, as illustrated in the bottom portion of Friedman Decl. ¶19, then the patentees could have said so in much simpler language. In fact, the patentees did just that in claim 2. There, the patent claims the structure of claim one, wherein the "capacitance means comprise more than one of said MOS capacitors." '830 at claim 2 (Ex. C). The fact that claim 5 does not use this plain language, and instead claims a "segmented" gate, is strong evidence that a different meaning should apply. *See Innova/Pure Water*, 381 F.3d at 1119 (explaining that all claim terms are presumed to have meaning, and a court should strive for a construction that gives meaning to all of its terms).

The specification also supports AMD's claim construction. The specification is "always highly relevant to the claim construction analysis." *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996). The embodiment that corresponds to claim 5 depicts a common doped region. '830 at 5:11-14; *see also* Fig. 16 (Ex. C). This embodiment shows multiple gate electrode segments (structure 18′) sharing a common, underlying doped region without insulation separating the underlying doped regions from each other. *Id.* at 5:18-25; Friedman Decl. ¶20.

The claim language itself is also highly instructive. Claim 5 states that "said gate electrode . . . is divided into a plurality of segments." '830 at 6:54-55 (Ex. C). The antecedent basis for "said gate electrode" is the "gate electrode" of independent claim 1. That claim, in turn, makes clear that the gate electrode overlies "*a* doped region." *Id.* at 6:27-28 (emphasis added).

The specification confirms that "*a* doped region" refers to a single doped region. Although "a" typically means one or more than one following "comprising," "a" is limited to meaning "one" where a plural interpretation would be "inconsistent with" the stated function of the invention. *Insituform Techs., Inc. v. CAT Contracting, Inc.*, 99 F.3d 1098, 1105-06 (Fed. Cir. 1996). This is such a case. Here, the patentee cites lower resistance as an advantage of the structure recited in claim 5. '830 at 5:30-32 (Ex. C). Specifically, the patentee states that by doping the areas in the substrate (N+ regions, shown as region 21 in Figure 16) corresponding to the gaps between the gate segments, "additional vias can be formed through oxide layer to interconnect not only N+ contact regions 20 and 22, but region 21 as well with the overlying bus. . . . This serves to *further lower* the resistance between the Vss bus and channel 24, i.e., the lower plate of capacitor 16." *Id.* at 5:26-32 (emphasis added). In other words, resistance can be lowered by having additional connections to the doped area of the substrate below and in between the gate segments. For this to happen, the gate segments would have to share a common doped region, as depicted in Figure 16. Friedman Decl. ¶22. Further, a person of ordinary skill in the art would understand that having a common doped region would be highly desirable to achieve the goal of lowered resistance. *Id.* As a matter of physics and electrical engineering, a decrease in resistance can only be assured if the bottom plate of the capacitor is a single node or electrical location with multiple connections. *Id.*

C. Two Structures Are "Electrically Connected Directly" if There Is No Active Device Between Them.

"Electrically connected directly between said busses" (claim 1, asserted claim 5)	
AMD's Construction	**Samsung's Construction**
"The bus and the capacitor are connected without any intervening active devices, such as transistors."	"Connected through a direct and physical electrical connection, which includes no intermediate structures, to the Vcc current bus and the Vss bus."

The correct construction of this term begins, as it should, with the language of the claim itself. *Phillips*, 415 F.3d at 1312. The claim requires that there be a direct *electrical* connection

between the capacitor and the bus. '830 at claim 5 (Ex. C). The claim does not recite a direct "physical" connection. In other words, the shape or configuration of any material between the two items does not affect whether the connection is "direct" in an electrical sense, as long as there are no active devices.

From an electrical perspective, a connection is "direct" as long as there is no "active device" (which, in the context of an integrated circuit, means a transistor, which often acts as a switch) between the two points. Friedman Decl. ¶24. If there were an active device between the two points being connected, the connection would be "indirect" because the switch could be turned off and there would be no connection at all. *Id.*

A person of ordinary skill in the art would agree with AMD's construction because it is the one most consistent with the intrinsic record, including the file history. Friedman Decl. ¶24. There, the applicants equated an "indirect" connection with one containing a switch or transistor. For example, in the February 2, 1987 Remarks, the applicants distinguished two prior art references (Kuo and Mao) by stating that "[b]oth of [those] references, as understood, disclose coupling one plate of a capacitor to the source or drain of the switching device in a memory cell while the other plate is connected to the Vcc line." Remarks, Feb. 2, 1987, at 8 (Ex. L). This shows that the patentee distinguished art cited by the examiner by noting that, while one plate of the capacitor connected to the Vcc bus, the other plate connected to an active device—namely, a transistor or "switching" device. The patentee further distinguished the prior art references by drawing a distinction between an indirect connection through a transistor on the one hand, and a direct connection to a bus, on the other:

> While the capacitors of the memory cells of the references each have an upper plate connected to the Vcc (power) bus, the lower plate of their memory capacitors, comprising the channel in the substrate beneath the upper plate gate electrode, is connected directly to the source/drain of the transistor in the memory cell, not to the Vss (ground) bus.

Id. at 8-9 (underlining in original). The Remarks go on to state:

> While the Office Action generically refers to Mao as connecting his capacitor to another bus (his bit line), the "connection" is only an indirect capacitive coupling through a dielectric to a signal bus, i.e.,

> his bit line, not to the Vss (ground) bus. Applicant's capacitance, on the other hand, is connected directly between the power busses, not to the signal busses.

Id. at 10. This provides further evidence to a person of ordinary skill in the art that a connection to an active device, such as a transistor, is not a direct connection to a Vss bus. Friedman Decl. ¶27. The terms "signal bus/bit line" generally refer to a wire that leads to a transistor. *Id*. By stating that the connection in the prior art device was "indirect" because it was connected to a transistor, the patentees clearly described how they used the term "direct."

Samsung's proposed construction is wrong. The construction improperly focuses on the physical connection between the capacitor and the bus. Further, Samsung's proposed language (which would have the jury inquire as to whether there is an "intermediate structure"), is extremely vague and includes no guidance as to what qualifies as an "intermediate structure." For example, a wire from A to B could be an "intermediate structure," yet no one would dispute that A and B, if connected by a single wire, are electrically connected directly.

Samsung's vague construction appears to exclude multi-layer, metal connections, even where there are no active devices. Samsung therefore excludes the patentees' preferred embodiment. *Vitronics*, 90 F.3d at 1583 (claim construction that excludes a preferred embodiment is rarely, if ever, correct). The '830 patent describes an embodiment where the gate electrode is electrically connected to the bus through several physical layers—which are "intermediate" structures apparently excluded by Samsung's construction. Figure 12 shows the gate electrode (structure 18) connecting to a "metal layer" (structure 66 and then 74). '830 at 4:47-53 (Ex. C). Figure 13, in turn, shows that metal layer 74 "in turn communicates with metal line 80 which interconnects gate electrode 18 with Vcc bus 4 as shown schematically in Fig. 3B." *Id.* at 4:53-61. At a minimum, structures 66/74 and 80 are "intermediate" physical structures between the gate electrode and the Vcc bus. Thus, Samsung's proposed construction cannot possibly be correct because it would exclude such "intermediate structures."

D. The "Vcc Current Bus" Is Internal and Supplies Charge.

"Vcc current bus" (claim 1, asserted claim 5)	
AMD's Construction	**Samsung's Construction**
"An internal bus (main conduit) for an integrated circuit that supplies charge for the transistors and capacitors."	"The main external power supply bus that provides current to an integrated circuit that contains input/output pads that are connected to external pins."

Both parties agree that the Vcc bus is a main supply bus or conduit. The parties differ in two respects: (1) where the bus is located and (2) what the bus supplies. AMD's construction provides that the Vcc bus is internal to the integrated circuit, and that it supplies "charge" for the transistors and capacitors. Samsung, in contrast, describes the location of the bus as "external" and asserts that the bus supplies "power."

1. The Bus Is Internal to the Integrated Circuit.

AMD's construction makes clear that the bus is internal to the integrated circuit. This construction is supported by the claims of the patent. Claim 1 opens with the statement that "what is claimed is:"

> In an improved integrated circuit structure comprising a semiconductor substrate having a plurality of active devices formed therein with a Vcc current bus and a Vss bus . . . .

'830 at 6:15-18 (Ex. C). This language refers to a structure that is internal to the integrated circuit (*i.e.*, one that is not off-chip). Friedman Decl. ¶32. The claim further provides that the capacitors are formed beneath at least one of the Vcc or Vss busses, and that the lower plate of the capacitor is a "doped region" of the substrate. '830 at 6:20-21, 6:27-29 (Ex. C). If the capacitors are on the integrated circuit, and the capacitors are formed beneath the busses, then the busses must be internal to the integrated circuit.

Further, the preferred embodiments described in the specification plainly depict the formation of a capacitor on the body of the integrated circuit beneath an internal Vcc bus. For example, Figure 3B shows the capacitor formed in the substrate. The Vcc bus is depicted as the internal line above the gate electrode. '830 at 3:50-65 (Ex. C); Friedman Decl. ¶34.

2. The Bus Supplies Charge.

AMD's construction is preferable to Samsung's because AMD uses the more precise term "charge" rather than "power." "Power" is a more colloquial term that is sometimes used to refer to both the Vcc bus and the other bus (the Vss bus). Friedman Decl. ¶35. Indeed, the specification uses the term "power" to refer to both busses. '830 at 1:30-37 (Ex. C). The term "charge" more precisely describes what the Vcc bus supplies. Friedman Decl. ¶36. Moreover, the specification uses the term "charge" when describing what the Vcc bus supplies. '830 at 3:22-23 (Ex. C).

E. A Gate Segment Is "Independently Connected Electrically" if It Has Its Own Connection.

"Independently connected electrically" (asserted claim 5)	
AMD's Construction	**Samsung's Construction**
"A gate segment is 'independently connected electrically' if it has its own connection or can connect without having to go through another gate segment."	"Each gate electrode segment is connected through a separate electrical path that is not shared by any other gate electrode segment."

AMD's proposed construction is correct because it reflects the plain and ordinary meaning of the terms. The words "independently connected electrically" have no specialized meaning in the art, other than the plain English meaning. Friedman Decl. ¶38. Accordingly, we look to the ordinary meaning of the words. *Phillips*, 415 F.3d at 1312. This is precisely the construction provided by AMD. Being "independent" simply means that one is not dependent or reliant upon another. A gate segment is not dependent or reliant upon another segment's connection if it has its own connection or can connect without having to go through another segment.

AMD's construction is consistent with the portion of the specification that corresponds with claim 5, *i.e.*, Figure 16 and the accompanying text. '830 at 5:11-43 (Ex. C). In Figure 16, the individual gate segments are identified as feature 18′. Each of these gate segments has its own connection (labeled 19′) that leads to the Vcc current bus. Each segment, therefore, can connect electrically to the Vcc bus "without having to go through another gate segment."

AMD's construction is also consistent with the stated goals of independent connections. One stated purpose of the structure of claim 5 is to create redundancy. '830 at 5:33-43 (Ex. C); Friedman Decl. ¶40. Gate segments that have their own connection, or that can connect to the bus without having to go through another segment, enhance redundancy. Friedman Decl. ¶40. If the connection from one gate segment to the bus is broken (whether it suffers a fabrication defect or is otherwise damaged), the remaining gate segments would continue to be connected and would continue to operate. '830 at 5:35-39 (Ex. C); *see also* Friedman Decl. ¶41. This is so because each remaining segment has its own connections, or stated differently, would not be dependent on the broken gate segment's connection. Friedman Decl. ¶41.

Samsung relies on a series of dictionary definitions to support its vague construction. They generally provide that an item is "independent" if it is not dependent upon another item, or does not require or rely upon something else to operate. Applying Samsung's own dictionary definitions, an "independent connection" still means that each segment has its own connection or can connect to the bus without having to go through another segment. Thus, Samsung's dictionaries support AMD's construction.

V. THE PURCELL '434 PATENT

A. Description of the Invention

The '434 patent teaches a circuit that performs multiplication, arithmetic, and logic operations. The '434 invention connects building-block circuits used in the prior art in a novel way to reduce the amount of circuitry required to perform those operations. The '434 patent improves processors by eliminating unnecessary circuitry, which saves both space and power.

Processors typically contain an "arithmetic and logic unit," or ALU, which performs both arithmetic operations, such as addition and subtraction, and logic operations, such as OR and AND. Wolfe Decl. ¶41. Complex operations are performed through combinations of basic arithmetic and logic building blocks. *Id.*

Simple logic operations like OR and AND perform decision functions on binary input values. Wolfe Decl. ¶42. Binary values are either 0 or 1. *Id.* The OR logic operation asks "does either input value equal 1?" Wolfe Decl. ¶43. The AND logic operation asks "do both input

values equal 1?" *Id.* If the answer to the question is yes, the ALU outputs a 1. *Id.* If the answer is no, the ALU outputs a 0. *Id.*

Prior art processors contained multiplication circuitry that was separate from the ALU. '434 at Fig. 1a, 1:15-17 (Ex. D). The multiplication circuitry performed multiplication operations by first using a "carry save stage" to generate a "carry" value and a "sum" value. *Id.* at Fig. 1a, 1:28-37. It then sent those values to a "carry propagate adder" dedicated to adding the "carry" and "sum" values. *Id.* at 1:54-58. By adding those values, the carry propagate adder outputs the final multiplication product. *Id.* The prior art multiplication circuitry did not use the ALU.

The '434 invention connects the outputs of the carry save stage to the ALU so that the ALU can add the "carry" and "sum" values. '434 at Figs. 2-3, 3:2-15 (Ex. D). The separate carry propagate adder, therefore, is not needed. *Id.* at 3:35-45. The '434 invention also places multiplexers between the carry save stage and the ALU. *Id.* at Figs. 2-3, 3:2-10. The multiplexers select between (1) carry and sum ALU inputs; and (2) standard ALU inputs. *Id.* at 3:6-25. The multiplexers allow the ALU to perform its normal operations or to finish multiplication operations by adding the "carry" and "sum" values. This integration of previously independent circuitry provides a fully functional processor that is smaller and more efficient.

B. An "Arithmetic and Logic Unit" Must Be Capable of Performing Both Arithmetic and Logic Functions.

"Arithmetic and logic unit" (asserted claims 1-4, 8, 11)	
AMD's Construction	**Samsung's Construction**
"Unit that can perform both arithmetic and logic operations."	"A conventional circuit which performs arithmetic and logic operations (e.g., addition) within the data processing system and optionally includes registers capable of receiving inputs from multiple sources within that data processing system."

The plain language of "arithmetic and logic unit" means a unit that performs both arithmetic operations and logic operations, as AMD has proposed. Wolfe Decl. ¶41. Samsung's proposed construction raises two issues for the Court to decide. First, Samsung's construction

suggests that a unit that performs only addition is an "arithmetic and logic unit." Therefore, the Court must decide whether an arithmetic and logic unit must be capable of performing both arithmetic operations and logic operations. Second, Samsung's construction adds a clause that the "arithmetic and logic unit" "optionally includes registers." The Court must decide whether a phrase that says "optionally includes" limits the claim in any meaningful way.

Adopting Samsung's construction (which requires only addition) would improperly read the limitation "and logic" out of the claims. *Cohesive Techs., Inc. v. Waters Corp.*, 543 F.3d 1351, 1368 (Fed. Cir. 2008). Samsung's construction therefore cannot be adopted "in the absence of support in the intrinsic record indicating that such a broad meaning was intended." *Nystrom v. TREX Co.*, 424 F.3d 1136, 1145-46 (Fed. Cir. 2005). "Arithmetic and logic unit" does not extend to a circuit that performs only addition because the intrinsic record contains no clear definition to broaden the term's scope. *Helmsderfer*, 527 F.3d at 1383. Instead, the specification explains that the disclosed ALU "performs arithmetic and logic operations." '434 at 1:17-19 (Ex. D).

The specification also contrasts the "arithmetic and logic unit" with a circuit that performs only addition. The prior art circuit in Figure 1a contained both an "arithmetic and logic unit" and a separate circuit dedicated to addition operations, called a "carry propagate adder." '434 at Fig. 1a, 1:17-19, 1:54-58 (Ex. D). The '434 invention eliminated the "carry propagate adder" by instead using the "arithmetic and logic unit" to perform addition operations. *Id.* at 3:35-45. The context of the specification shows that "arithmetic and logic unit" means something different than a basic "adder." According to the plain claim language, an "arithmetic *and logic* unit" must also perform logic operations. Wolfe Decl. ¶41.

During prosecution, the '434 applicants demonstrated that an "arithmetic and logic unit" performs both arithmetic operations and logic operations. The applicants explained that the Vassiliadis reference "teach[es] an ALU which only performs a specified set of addition, subtraction, and logic operations." Amendment, June 28, 1996, at 7 (emphasis original) (Ex. M); *see also* U.S. Pat. No. 5,299,319 at Fig. 1, 7:50-66 (describing an ALU with both add and logic operations) (Ex. N). Vassiliadis' disclosure of an ALU that performs both arithmetic and logic operations further supports AMD's construction. *V-Formation*, 401 F.3d at 1311 (explaining that

intrinsic record includes cited art). The file history, therefore, shows that an "arithmetic and logic unit" must be capable of performing both arithmetic operations and logic operations.

Samsung's proposed "optionally includes" clause does not limit the claim and therefore should not be adopted as part of the construction of a claim limitation. Also, claim 3, which depends from claim 1, recites registers as an element separate from the "arithmetic and logic unit," showing that Samsung's construction is incorrect. *Phillips*, 415 F.3d at 1314 ("[T]he context in which a term is used in the asserted claim can be highly instructive."). Samsung's construction does not limit the claim and contradicts the claim language, so it should be rejected.

C. A "Bus Coupling Said Carry Save Stage to Said ALU" Cannot Be Limited to a Direct Physical Path.

"Bus coupling said carry save stage to said ALU" (asserted claims 1-4)	
AMD's Construction	**Samsung's Construction**
"Bus that can transfer information between the carry save stage and the ALU."	"Direct physical path between the carry save stage and ALU that does not modify the value from the carry save stage."

AMD's proposed construction of "bus coupling" applies the plain meaning of the claim language. In contrast, Samsung's "direct physical path" construction excludes any intervening structures, which contradicts the claim language and excludes all embodiments disclosed in the patent. Samsung's "does not modify" limitation also finds no support in the intrinsic record.

The claims do not recite a "direct physical path" between the carry save stage and the ALU. Samsung's construction, therefore, cannot be adopted absent an express disclaimer or definition in the specification or file history. *Voda*, 536 F.3d at 1320. No such disclaimer or definition exists. Instead the intrinsic record uniformly contradicts Samsung's proposal.

First, the claims recite structures other than buses that are disposed between the carry save stage and the ALU, including "multiplexers" recited in claim 1, and "registers" recited in dependent claim 3. '434 at 4:4-7; 4:15-21 (Ex. D); Wolfe Decl. ¶46. Claim 1 explicitly recites a multiplexer "coupled between said first bus and said ALU," and claim 3 recites a register "coupled between said first multiplexer and said ALU." *Id.* The claims therefore cannot be

limited to a "direct physical path" between the carry save stage and the ALU. The claims' contradiction of a "direct physical path" demands that Samsung's construction be rejected. *Phillips*, 415 F.3d at 1314.

Second, all embodiments disclosed in the specification depict multiplexers and registers between the carry save stage and the ALU. *See* '434 at Figs. 2-3, 3:2-10, 3:18-25 (Ex. D); Wolfe Decl. ¶45. Samsung's "direct physical path" construction excludes all embodiments from claims 1-4 and cannot be correct. *Oatey*, 514 F.3d at 1276-77; *Johns Hopkins Univ. v. CellPro, Inc.*, 152 F.3d 1342, 1355 (Fed. Cir. 1998) ("A patent claim should be construed to encompass at least one disclosed embodiment in the written description portion of the patent specification.").

Finally, the intrinsic record does not specify whether the buses coupling the carry save stage to the ALU modify the values from the carry save stage. Samsung's "does not modify" phrase adds a limitation that is neither claimed nor found in the intrinsic record, so it is incorrect.

AMD's construction adopts the plain meaning of the claim language as informed by the meaning of "coupling" as it is understood by those of skill in the art. *The New IEEE Standard Dictionary of Electrical and Electronics Terms* (1993) at 277 (defining "coupling") (Ex. O); Wolfe Decl. ¶44.

VI. THE PEDNEAU '200 PATENT

A. Description of the Invention

The '200 patent teaches a key logic circuit for controlling the power consumed by testing logic. The key logic circuit determines from its inputs whether or not the testing logic should consume power. The '200 patent therefore allows the processor to reduce the power consumed by testing logic when the testing logic is not being used.

Nearly all processors sold today contain testing logic. Wolfe Decl. ¶20. A single processor may contain many testing logic circuits that each consume power. *Id.*; '200 at Fig. 1 (Ex. E). Testing logic is used to determine if the processor is operating correctly. '200 at 1:13-26 (Ex. E); Wolfe Decl. ¶20. Testing logic is used at the manufacturing stage to test processors before they are shipped, and is used in the field to ensure that the processor works. Wolfe Decl. ¶20. For example, testing logic may be used each time a consumer turns on a cell phone. *Id.*

The '200 patent solved two problems with prior art testing logic. First, prior art testing logic consumed power even when it was not performing tests. '200 at 1:37-47 (Ex. E). Second, standard ways of adjusting power consumption were susceptible to errors and so were not dependable for reducing the power consumed by testing logic. *Id.* at 1:50-53, 4:23-35. The errors would cause the testing logic to consume full power when it was not needed. *Id.*

The '200 invention solves the prior art problems with a key logic circuit for controlling the power consumed by testing logic. As its name suggests, the key logic circuit will not allow the testing logic to consume full power unless the key logic circuit receives the correct "key signal." '200 at 1:61 – 2:2, 3:52-65, 8:38-63 (Ex. E). The key signal must contain the correct bit sequence to activate the testing logic, so the key logic circuit is not susceptible to errors. *Id.* at 4:23-35.

The '200 key logic circuit also decreases the power consumed by testing logic in response to a "reset signal." '200 at 1:61 – 2:2, 3:40-51 (Ex. E). When the key logic circuit receives the reset signal, the circuit adjusts the testing logic power to a "low power state." *Id.* The testing logic remains in this state until it is needed again. At that time, the key signal is sent to the key logic circuit, and the circuit adjusts the testing logic power to a "normal power state."

B. The '200 Intrinsic Record Does Not Exclude Addresses and Instructions from a "Data Pattern."

"Data pattern" (asserted claims 1-3, 5-8, 11-13, 15-17, 19)	
AMD's Construction	**Samsung's Construction**
"Bit sequence."	"A pattern of bits representing information and not representing an address or an instruction."

AMD and Samsung agree that a "data pattern" means a "bit sequence" or a "pattern of bits." Samsung seeks to further limit the term to "bits representing information and not representing an address or an instruction." Samsung's "and not" phrase cannot be adopted without a specific, unequivocal disclaimer in the specification or file history. *Baldwin Graphic Sys.*, 512 F.3d at 1346. That disclaimer does not exist, so AMD requests that the Court enter the

straightforward construction "bit sequence."

The '200 claims do not exclude any type of "data" from the "data pattern." Each asserted '200 claim recites a system that drives a logic testing circuit to a normal power state when a "key signal matches a predetermined data pattern." *See, e.g.*, '200 at 9:34-36 (claim 1) (Ex. E). The term "data," on its face, does not exclude addresses and instructions. Wolfe Decl. ¶¶48-49.

The '200 specification does not disavow "data" that represents addresses or instructions. The specification refers to "data" without a definition or disclaimer. For example, it explains that "[a] valid key signal is a signal that matches a predetermined data pattern." '200 at 3:55-56 (Ex. E). The specification makes no suggestion that "data" excludes an address or instruction. It therefore provides no basis to exclude any kind of "data."

The '200 file history also does not limit "data" or "data pattern." Neither the applicant nor the examiner ever argued that "data" cannot represent an address or instruction. Therefore, nothing in the intrinsic record supports Samsung's proposed construction. AMD requests that the Court adopt AMD's construction: "data pattern" means "bit sequence."

VII. THE ORR '879 PATENT

A. Description of the Invention

The '879 patent teaches a graphical user interface for controlling video in electronic devices that contain a processor and memory. The '879 user interface allows the user to control video that is displayed in the background on a display while keeping other applications visible and active. Wolfe Decl. ¶21. The user does not have to obscure the "foreground" applications in order to control the video in the background. *Id.*

The '879 user interface appears on the display while video is in the background and other applications are "in focus," which the parties have agreed means "actively being displayed and/or being worked upon." Dkt. #92, Joint Claim Construction & Prehearing Statement at 2. The user interface contains a "video control icon." '879 at Fig. 1, 2:5-18 (Ex. F). When that icon is selected, a control panel appears that contains controls for the background video. *Id.* The applications in the foreground are not taken out of focus. *Id.*

The '879 invention provides an improved viewing experience for the user by allowing the

user to control background video without losing focus on foreground applications. '879 at 1:42-50 (Ex. F). The video may be supplied to the display by a television broadcast, cable, DVD player, VCR, or other source. *Id.* at 3:9-12. The control panel may contain any controls for the background video, and in a preferred embodiment contains controls that correspond to particular video sources. *Id.* at 2:32-42. For example, if the video source is cable, then the control panel might contain a volume icon, channel up and channel down icons, and a display of the channel name or number. *Id.* at 2:32-38, 3:37-41. If the video source is a DVD player, the control panel might contain a volume icon, fast forward and reverse icons, and stop icon. *Id.* at 2:39-42, 3:41-43. The '879 invention therefore can be tailored to many types of electronic devices.

The '879 invention provides a great benefit for user interfaces in cell phones and other mobile electronic devices. Consumers now demand more and more functionality from handheld devices, including digital camera, camcorder, and video playback functions. In addition, handheld devices display applications that are important to the user, including indicators for remaining battery life and wireless signal strength. The '879 invention improves the user interface in handheld devices by providing an elegant and flexible way to control video operations while keeping the foreground applications in focus.

B. Neither the "Control Panel" nor Any Other Term Limits the '879 Claims to a Personal Computer.

"Control panel" (asserted claims 11-24)	
AMD's Construction	**Samsung's Construction**
Needs no construction. If a construction is required, AMD agrees to the following portion of Samsung's construction: "Area of the screen containing control functions."	"An area of the personal computer screen containing control functions."

The term "control panel" with respect to an electronic display is easily understood by lay persons as well as those of skill in the art, so it needs no construction. Samsung asks the Court to limit a "control panel" to something that appears on a "personal computer." The Court must decide, therefore, whether some part of the '879 intrinsic record unequivocally excludes all

"control panels" except personal computer "control panels." *Baldwin Graphic Sys.*, 512 F.3d at 1346. Nothing in the intrinsic record supports such a narrow limitation. In fact, no '879 claim term or portion of the intrinsic record supports a specific exclusion of any electronic device.

Asserted '879 claims 11-24 do not recite a "personal computer." '879 at 4:42 – 6:49 (Ex. F). They also do not recite a "computer." *Id.* Instead, they recite a "processing unit" that reads "programming instructions" from memory in order to provide a "control panel" on a "display." *Id.* The claim preambles explain that the invention is a "video graphics processor" (claims 11-16) or "digital storage device" (claims 17-24), not a personal computer. The plain language of the claims, therefore, shows that the patentee chose to define the invention in terms of the processor and programming instructions for controlling video, and did not define the invention by the hardware environment where that video control subsystem is used.

In contrast to the claim language, Samsung argues that a "control panel," found in every claim, should be limited to a "personal computer" control panel. The plain language of the claims does not require a "personal computer." Wolfe Decl. ¶¶50-52. Televisions, for example, contain a "processing unit" and use "programming instructions." Wolfe Decl. ¶52. So do cell phones and other electronic devices. *Id.* On their face, the claims cover each of these devices, because the claims cover only the video graphics subsystem, and do not limit the kind of hardware where that subsystem may be used. *Id.*

The '879 claims recite aspects of the "control panel" that generally are associated with televisions and other devices, not personal computers. Claim 12 recites a "control panel" that may include a "channel up icon" and "channel down icon." '879 at 4:56-62 (Ex. F). Claims 15, 19, and 23 recite similar limitations. The context of the '879 claims therefore conflicts with limiting the "control panel" to a personal computer. *Phillips*, 415 F.3d at 1314 ("[T]he context in which a term is used in the asserted claim can be highly instructive.").

Other '879 claims show that the "control panel" cannot be limited to something on a "personal computer screen." Samsung's limitation of the "control panel" to something that appears on a "personal computer screen" necessarily means that the claimed "display" must be a "personal computer display." But the '879 claims show that the "display" must cover more than a

"computer display." Wolfe Decl. ¶55. Claim 1 recites "(a) . . . live video that is being presented as a background on a display." '879 at 3:58-61 (Ex. F). Claim 5 depends from claim 1, and recites "[t]he method of claim 1 further comprises, within step (a), providing the live video as the background on a computer display, a television, or a monitor." *Id.* at 4:12-14. Claim 5 therefore raises a presumption that the "display" in claim 1 has a broader scope than the display types recited in claim 5. *Halliburton Energy Services*, 514 F.3d at 1251 n.3. That presumption is not rebutted anywhere in the intrinsic record.

Additionally, Samsung's construction cannot be correct because if the term "control panel" in claim 1 requires a "personal computer" display, then the "computer display" recited in claim 5 is redundant and the "television" and "monitor" limitations are meaningless. *Cohesive Techs.*, 543 F.3d at 1368. The broad meaning of "display" in claim 1 should apply to the "display" in asserted claims 11-24, because words are given the same meaning throughout the claims. *Phillips*, 415 F.3d at 1314.

The specification and file history contain no specific disclaimer or definition related to the term "control panel." With no recitation of a personal computer in the claims, and no explicit disclaimer or definition in the intrinsic record, Samsung's construction has no support and must be rejected. *Voda*, 536 F.3d at 1320; *Baldwin Graphic Sys.*, 512 F.3d at 1346.

The specification's references to a "computer" do not limit the claimed "control panel" to something found on a personal computer display. The claims recite only the video graphics subsystem, and do not recite characteristics of the more general environment where the graphics subsystem is used. Wolfe Decl. ¶52. Because each asserted "claim addresses only some of the features disclosed in the specification, it is improper to limit the claim to other, unclaimed features." *Broadcom*, 543 F.3d at 689 (quoting *Ventana Med. Sys., Inc. v. Biogenex Labs., Inc.*, 473 F.3d 1173, 1181 (Fed. Cir. 2006)).

The specification also discloses embodiments that would not be understood by those of skill as parts of "personal computers." Wolfe Decl. ¶¶53-54. The specification explains that "[t]he live video may be displayed on a computer display, a television, or a monitor." '879 at 3:12-14 (Ex. F); Wolfe Decl. ¶54. It also teaches that the invention's "processing unit" can be "a

microprocessor, microcontroller, a digital signal processor, a microcomputer, or any other means for processing digital information based on programming instructions." '879 at 2:53-56 (Ex. F). Of these, only a "microprocessor" generally would represent the processing unit of a "personal computer" to one of skill at the time of the invention. Wolfe Decl. ¶53. A "microcontroller" or "digital signal processor," on the other hand, might serve as the processing unit of a television, cell phone, or other device. *Id.* These embodiments, which fall within the plain meaning of the claims, should not be excluded because the intrinsic record contains no exclusionary disclaimer or definition. *Oatey*, 514 F.3d at 1276-77.

The '879 claims do not recite a "personal computer" or any other hardware environment, and the specification discloses embodiments that would not be found in a "personal computer." AMD therefore requests that the Court either decline Samsung's request to construe "control panel" or adopt "area of the screen containing control functions."

CONCLUSION

AMD's proposed constructions reflect the meanings of the terms as demonstrated by the intrinsic record. AMD respectfully requests that the Court enter the attached proposed order containing AMD's proposed constructions.

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