Exhibit L

Exhibit to the Declaration of Aaron R. Fahrenkrog in Support of Plaintiffs' Opening Claim Construction Brief

Ap 253

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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AL
2-21-87

Applicant:	Patel et al
Serial Number:	817,227
Filed:	January 8, 1986
For:	IMPROVED INTEGRATED CIRCUIT STRUCTURE HAVING COMPENSATING MEANS FOR SELF-INDUCTANCE EFFECTS
Group Art Unit:	253
Examiner:	Edward J. Wojciechowicz

CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in the envelope addressed to: Commissioner of Patents and Trademarks, Washington, D. C. 20231, on 02/03/87.
Signature Quin Rideneur

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AMENDMENT UNDER 37 C.F.R. 1.115

February 2, 1987

The Honorable Commissioner of Patents
and Trademarks
Washington, D.C. 20231

Dear Sir:

The following amendment is made in response to the Office Action, mailed November 5, 1987 in the above-identified application:

IN THE SPECIFICATION:

Page 7, line 15, cancel "on", substitute "in".

Page 9, line 8, cancel "doped", second occurrence.

IN THE CLAIMS:

Cancel claims 1 and 13-23.

Add the following new claims:

24. In an integrated circuit structure having active devices connected to a power bus and a ground bus with self inductance generated in the busses during switching from hi to lo states and from lo to hi states, the improvement which comprises capacitance means electrically connected between the busses and distributed along the length of the busses to compensate for said inductance generated in said busses during said switching.

CM 1/ ~~25~~. In an improved integrated circuit structure comprising a semiconductor substrate having a plurality of active devices formed therein with a Vcc current bus and a Vss bus connected to said active devices thereon, the improvement comprising:

cont'd A'

P1 (a) capacitance means formed beneath at least one of said busses comprising one or more MOS capacitors having a gate electrode forming a first plate of said capacitance means and electrically connected to one of said busses by at least one conductive path between said first plate and said one of said busses;

P1 (b) a doped region formed in said substrate beneath said gate electrode comprising the opposite plate of said capacitance means and separated from said gate electrode by gate oxide means formed on said substrate; and

P1 (c) electrode means comprising a source/drain in said substrate contiguous with said doped region and electrically connecting said doped region of said MOS capacitor to the other of said busses;

P5 whereby inductance voltages induced in said busses during switching will be compensated for by said capacitance means electrically connected directly between said busses and distributed along said busses to thereby reduce the voltage spikes produced by said induced voltages.

NP Amend claim 2 under 37 C.F.R. 1.121(c) as follows:

MC Claim 2, line 1, cancel "1", substitute "24".

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REMARKS

This amendment is in response to the Office Action mailed November 5, 1987. Claims 1 and 13-23 have been cancelled; claim 2 has been amended; and new claims 24 and 25 have been added. Claims 2-12 and 24-25 are now in the case.

I. SUMMARY OF THE NOVEMBER 5, 1986 OFFICE ACTION

A. Restriction Requirement

The Office Action contains a Restriction Requirement restricting the claims of the application under 35 U.S.C. 121 to: Invention I, claims 1-12, drawn to a semiconductor device; or Invention II, claims 13-23, drawn to a process for making semiconductor devices. The Office Action further notes a provisional election with traverse by one of applicants' attorneys, during a telephone conversation, to prosecute the invention of I, claims 1-12. The claims of Invention II have been cancelled by this amendment without prejudice to the filing of a divisional application.

B. Section 112 Rejection

Claims 1-12 were rejected under 35 U.S.C. 112 as vague and indefinite and for failing to particularly point out and distinctly claim the invention. The Rejection states that in claim 1, the overall structure of the claimed device is not defined. The Office Action questions what is meant by the "channel means" formed as the opposite plate of the capacitor in claim 12 and further asks what it is a channel between. The Rejection also raises a question as to how the electrode in claim 12 connects the channel to the

other bus.

C. Section 103 Rejections

Claims 1-12 were rejected under 35 U.S.C. 103 as unpatentable over Kuo et al U.S. Patent 4,536,941 in view of Mao U.S. Patent 4,493,056. The Rejection states that applicants' invention concept appears to reside in the formation of MOS capacitors along the length of voltage busses. Kuo et al is said to show an MOS capacitor structure which forms a channel region that acts as one of the plates of the capacitor and wherein the capacitor is connected to a voltage bus. The Office Action states that the Mao patent shows a related capacitor structure where capacitors are formed between two busses in an MOS structure. The Rejection states that in view of these references, it would be obvious to adjust capacitance by adjusting oxide thickness, etc. The Rejection also says that as seen by the references, alternate bus configurations would also be obvious design variants.

II. THE INVENTION

The invention provides an improved integrated circuit structure wherein induced voltage spikes in the Vss and Vcc busses are compensated for by providing one or more capacitors coupled between the two busses. The capacitors may comprise MOS capacitors wherein the gate is one plate of the capacitor and the channel formed in the substrate beneath the gate comprises the other electrode or plate of the capacitor with the gate oxide functioning as the dielectric therebetween. One of the busses is electrically connected

to the gate electrode while the other bus is connected to the other plate of the capacitor (the channel formed in the substrate) by connecting the bus to source and/or drain regions in the substrate contiguous with the channel.

The capacitor may also be formed by providing either a doped region of the substrate or a metal layer which forms an electrode member beneath one of the busses and electrically isolated therefrom by an insulation layer such as an oxide layer which functions as a dielectric layer. The overlying bus functions as one plate of the capacitor while the electrode member comprising the metal layer or doped substrate region functions as the other plate of the capacitor. The electrode member is then electrically connected to the other bus to provide the desired capacitance between the two busses.

III. THE CITED REFERENCES

A. The Kuo et al Reference

Kuo et al U.S. Patent 4,536,941 discloses a method of making an MOS transistor for a memory cell using a triple level polysilicon process. One of the polysilicon layers also functions as the Vcc line and forms capacitors with portions of the substrate which are in communication with the respective drains of the memory transistors to couple the respective memory transistors to the Vcc line.

B. The Mao Reference

Mao U.S. Patent 4,493,056 describes an electronic memory array comprising a plurality of FET memory cells. Each memory cell includes a capacitance storage region and a FET or MOS device to control the transfer of information

into and out of the capacitive storage region. One electrode or plate of the capacitance storage region is connected to a plate line and the other side is connected to the source or drain of the MOS device through which it is connected to a first bit line. The capacitance storage region is also coupled, through a metal diffusion capacitance, to a second bit line.

IV. DISCUSSION

A. Section 112 Rejections

In response to the Rejection under 35 U.S.C. 112, claim 1 has been rewritten as new claim 24 with further background material which, although not specifically recited in applicants' specification, is notoriously well known to anyone skilled in this art and should provide the requested "overall structure".

With respect to the objections to claim 12, these are not understood. Applicants describe, on page 8 of their specification at lines 24-29, the formation of their capacitor using the gate electrode as one plate of the capacitor and channel 24 as the other plate of the capacitor. (See also Figures 7-12) Applicants chose to use the term "channel" since this is the term commonly used to describe the region in the substrate beneath the gate electrode in an MOS device and applicants have termed their capacitance device an MOS capacitor due to the similarities in construction of the device and an MOS transistor. It is noted that Kuo et al use the term "inverted region" in their specification to describe the lower plate of their capacitor. Since an applicant may be his own lexicographer, it is not under-

stood why applicants' use of this term is objectionable since its meaning is clear from applicants' specification

As to the other questions "what is it a channel between?" and "How does the electrode connect the channel to the other bus?", the answer to the first question will be obvious to anyone skilled in the art relating to MOS devices. Applicants, as discussed above, have used language familiar to those skilled in MOS technology to discuss some of the elements of their capacitor since applicants have termed it an MOS capacitor.

With respect to the second question, the answer is clearly shown in Figure 11 wherein electrodes 20 and 22 are shown connected directly to metal layer 70 which is described in applicants' specification on page 11, lines 18-20, as capable of functioning as the bus. If what is desired is that applicants limit themselves to a particular type of connection between the electrode and the bus, then applicants must protest same as being unduly limiting and in direct contravention of the provisions of 35 U.S.C. 112, second paragraph which permits applicants to claim "...the subject matter <u>which the applicant regards</u> as his invention." (emphasis added).

Applicants have submitted a new claim, claim 25, with different language which may be deemed to be more acceptable to the USPTO.

B. <u>Section 103 Rejections</u>

Both of the references, as understood, disclose coupling one plate of a capacitor to the source or drain of the switching device in a memory cell while the other plate

is connected to the Vcc line. In both instances, the storage capacitor comprises one plate which is a polysilicon strip while the other plate comprises a channel formed in the substrate. The capacitor plate which comprises the channel is coupled to the memory cell transistor through the source or drain of the transistor. The gate of the memory cell transistor is coupled to a word line. In this regard, the only difference between the two references appears to be that the plate of the storage capacitor in Mao comprising the channel which is connected to the source or drain of his transistor is also coupled, through capacitance CMD to one of the bit lines. This coupling capacitor CMD, as understood, comprises a capacitance through the oxide which separates bit line BL1 from the substrate and the other plate of the capacitor as shown in Figure 2 of Mao.

Thus, neither the illustrated capacitors of Kuo et al or Mao function to provide the desired compensating capacitors to counter the inductance generated in either the Vcc or Vss lines respectively during the switching of the lines from high to lo. Rather the capacitors illustrated in the references functions as a part of the memory of the respective memory cells.

Since the memory capacitors of the references do not function in the same manner as do the applicants' capacitors, it is not surprising that they are connected differently. While the capacitors of the memory cells of the references each have an upper plate connected to the Vcc (power) bus, the lower plate of their memory capacitors, comprising the channel in the substrate beneath the upper plate gate electrode, is connected directly to the

source/drain of the transistor in the memory cell, not to the Vss (ground) bus. While the Office Action generically refers to Mao as connecting his capacitor to another bus (his bit line), the "connection" is only an indirect capacitive coupling through a dielectric to a signal bus, i.e., his bit line, not to the Vss (ground) bus. Applicants' capacitance, on the other hand, is connected directly between the power busses, not to the signal busses.

Thus, neither reference suggests the problem which applicants seek to solve and neither reference suggests the solution to this problem. What the references show is that it is known to form capacitors in integrated circuit structures and that such capacitors can be formed using a gate as one electrode and a channel or region formed in the substrate below the gate and separated therefrom by a gate oxide as the other electrode with the gate oxide therebetween forming the dielectric of the capacitor. This does not suggest applicants' claimed structure having capacitance formed directly between the Vcc and Vss busses and applicants' claims should be patentable over this combination.

V. SUMMARY AND CONCLUSION

Neither of the references contains any mention of the problem of self-inductance generated in the power lines or busses of an integrated circuit structure and neither, therefore, contain any suggestion as to applicants' solution by providing capacitance directly coupled electrically between the Vcc and Vss busses. If the examiner in charge of this case feels there are any issues yet unresolved by this amendment, the examiner is urged to contact applicant's undersigned attorney at the telephone number listed below which is in the Pacific Coast Time Zone.

Respectfully Submitted,

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