Exhibit M

Exhibit to the Declaration of Aaron R. Fahrenkrog in Support of Plaintiffs' Opening Claim
Construction Brief

GP 2306
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Stephen C. Purcell

Assignee: Chromatic Research, Inc.

Title: "STRUCTURE AND METHOD OF USING AN ARITHMETIC AND LOGIC UNIT FOR A CARRY PROPAGATION STAGE OF A MULTIPLIER"

Serial No.:   08/281,377   Filed: July 27, 1994

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San Jose, California
June 28, 1996

COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D. C.   20231

AMENDMENT

Sir:

In response to the Office Action mailed March 29, 1996, Applicant respectfully submits the following amendments and remarks.

IN THE SPECIFICATION

Page 6, line 3, change "Figs. 2 and 3" to --Fig. 2--.

IN THE CLAIMS

Please amend Claims 1-2, 5-6, and 8-10 as follows.

1.   (Twice Amended)   A multiplier for use in a data processing system having an arithmetic and logic unit (ALU), said multiplier comprising:

a first input terminal for receiving a first data value;

a second input terminal for receiving a second data value;

a carry save stage coupled to said first and second terminals, wherein said carry save stage generates a carry signal and a sum signal in response to said first and second data values;

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12   a first bus coupling said carry save stage to said

13   ALU, wherein said first bus provides said carry signal to

14   said ALU; [and]

15   a second bus coupling said carry save stage to said

16   ALU, wherein said second bus provides said sum signal to

17   said ALU [, whereby said ALU is capable of adding said

18   carry and sum signals to create a third data value equal

19   to the product of said first and second data values.] ;

20   a first multiplexer coupled between said first bus

21   and said ALU; and

22   a second multiplexer coupled between said second bus

23   and said ALU, whereby said ALU is capable of adding said

24   carry and sum signals to create a third data value equal

25   to the product of said first and second data values.

1   2.   (Twice Amended)   The multiplier of Claim 1,

2   further comprising:

3   [a first multiplexer coupled between said first bus

4   and said ALU;

5   a second multiplexer coupled between said second bus

6   and said ALU;]

7   a third bus coupled between said first terminal and

8   said first multiplexer; and

9   a fourth bus coupled between said second terminal and

10   said second multiplexer.

1   5.   (Twice Amended)   The multiplier of Claim 1,

2   further comprising:

3   a third terminal for receiving a third data value;

4   a fourth terminal for receiving a fourth data value;

5   [a first multiplexer coupled between said first bus

6   and said ALU;

7   a second multiplexer coupled between said second bus

8   and said ALU;]

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9   a third bus coupled between said third terminal and

10   said first multiplexer; and

11   a fourth bus coupled between said fourth terminal and

12   said second multiplexer.

1   6.   (Amended) The multiplier of Claim 5, further

2   comprising:

3   a first register coupled between said first

4   multiplexer and said ALU, wherein said carry signal is

5   stored in said first register; and

6   a second register coupled between said second

7   multiplexer and said ALU, wherein said sum signal is

8   stored in said second register.

1   8.   (Amended) A multiplier for use in a system having an

2   arithmetic and logic unit (ALU), said multiplier comprising:

3   a first input terminal for receiving a first data

4   value;

5   a second input terminal for receiving a second data

6   value;

7   a carry save stage coupled to said first and second

8   terminals, wherein said carry save stage generates a carry

9   signal and a sum signal in response to said first and

10   second data values; [and]

11   means for coupling said carry save stage and said

12   first and second input terminals to said ALU,

13   wherein said carry and sum signals and said first and

14   second data values are transmitted to [first and second

15   input terminals of] said ALU, whereby said ALU is capable

16   of adding said carry and sum signals to provide a third

17   data value equal to the product of said first and second

18   data values; and

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19   means for controlling said means for coupling, said

20   means for controlling having a first and a second state,

21   wherein in said first state said means for controlling

22   causes said means for coupling to route said carry and sum

23   signals to said ALU and to prevent said means for coupling

24   from routing said first and second data values to said

25   ALU, and wherein in said second state said means for

26   controlling causes said means for coupling to route said

27   first and second data values to said ALU and to prevent

28   said means for coupling from routing said carry and sum

29   signals to said ALU.

1   9.   (Amended) A method of multiplying a first data value

2   and a second data value in a system having an arithmetic and

3   logic unit (ALU), said method comprising the steps of:

4   transmitting said first and second data values to a

5   carry save stage[:] ;

6   generating a carry signal and a sum signal within

7   said carry save stage in response to said first and second

8   data values;

9   transmitting said carry and sum signals to said ALU;

10   and

11   adding said carry and sum signals within said ALU to

12   create a third data value equal to the product of said

13   first and second data values.

1   9.   (Amended) A method of multiplying a first data value

2   and a second data value in a system having an arithmetic and

3   logic unit (ALU), said method comprising the steps of:

4   transmitting said first and second data values to a

5   carry save stage;

6   generating a carry signal and a sum signal within

7   said carry save stage in response to said first and second

8   data values;

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9   transmitting said carry signal to a first

10   multiplexer;

11   transmitting said sum signal to a second multiplexer;

12   transmitting said first data value to said first

13   multiplexer;

14   transmitting said second data value to said second

15   multiplexer;

16   transmitting a multiplexer control signal to said

17   first and second multiplexers;

18   routing said carry signal through said first

19   multiplexer to said ALU in response to said multiplexer

20   control signal when said multiplexer control signal is in

21   a first state;

22   routing said sum signal through said second

23   multiplexer to said ALU in response to said multiplexer

24   control signal when said multiplexer control signal is

25   said first state; _and_

26   adding said carry and sum signals within said ALU to

27   create a third data value equal to the product of said

28   first and second data values.

1   (Add new Claim 12 as follows.)

1   --   12.   (New)   A system comprising:

2   a carry save stage coupled to receive a first data

3   value and a second data value, wherein the carry save

4   stage generates a carry signal and a sum signal in

5   response to the first and second data values;

6   a first selector circuit coupled to receive the carry

7   signal and the first data value;

8   a second selector circuit coupled to receive the sum

9   signal and the second data value;

10   a control signal source coupled to the first and

11   second selector circuits, wherein the control signal

12   source causes the first and second selector circuits to

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13 operate in a first mode and a second mode, wherein in the

14 first mode, the first selector circuit passes the carry

15 signal and the second selector circuit passes the sum

16 signal, and wherein in the second mode, the first selector

17 circuit passes the first data value and the second

18 selector circuit passes the second data value; and

19   an arithmetic and logic unit (ALU) coupled to the

20 first and second selector circuits, wherein the ALU

21 receives the signals passed by the first and second

22 selector circuits, and wherein in the first mode, the ALU

23 adds the carry and sum signals to create a third data

24 value equal to the product of the first and second data

25 values.--

REMARKS

The specification has been amended to add clarity. Thus, "Figs. 2 and 3" has been replaced with "Fig. 2" to clarify the subsequent references in that paragraph to multiplier circuit 200. (See, Specification at page 6, line 3). No new matter is added.

Claims 1-12 are pending in the present application. Claims 1-11 have been rejected under 35 U.S.C. §103 as being unpatentable over admitted prior art by applicant in view of Vassiliadis et al. This rejection is respectfully traversed in view of the foregoing amendments to the claims and the following remarks.

Claim 1 recites "a first bus" which "provides said carry signal to said ALU; a second bus" which "provides said sum signal to said ALU; a first multiplexer coupled between said first bus and said ALU; and a second multiplexer coupled between said second bus and said ALU." (Emphasis added.) This advantageously allows the arithmetic and logic unit (ALU) to add "said carry and sum signals to create a third data value equal to the product of said first and second data values."

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The admitted prior art does not teach or suggest "a first multiplexer" and "a second multiplexer" as recited in Claim 1. The admitted prior art has no need for such "a first multiplexer" and "a second multiplexer" because the carry and sum signals are added by a carry propagate adder 118 within multiplier 100.

Vassiliadis et al. do not remedy the shortcomings of the admitted prior art. Rather, Vassiliadis et al. teach that a carry save adder (CSA) be directly wired to a carry-look-ahead adder (CLA). More specifically, Vassiliadis et al. recite:

> The functional blocks supplying the inputs to the CLA;
> therefore, have been reduced to two, the CSA and the
> logical function blocks. The sum, σ, can be directly
> wired to one of the inputs to the CLA as it always
> supplies an appropriate input. (Emphasis added.)
> (Vassiliadis et al., Col. 15, lines 60 - 65.)

As a result, Vassiliadis et al. teach a CSA in which the sum is directly wired to the first input of a CLA. (See, Fig. 7 of Vassiliadis et al.) Vassiliadis et al., therefore, fail to teach or suggest "a first multiplexer" and "a second multiplexer" as recited in Claim 1.

Moreover, Vassiliadis et al. teach an ALU which only performs a specified set of addition, subtraction and logic operations. (See, Vassiliadis et al., Col. 10, lines 51-61). Vassiliadis et al. therefore fails to teach or suggest "[a] multiplier" which provides "a third data value equal to the product of said first and second data values" as recited in Claim 1. (Emphasis added.)

In addition, because Vassiliadis et al. is not directed toward a multiplier, no motivation exists to combine Vassiliadis et al. with the admitted prior art. For these reasons, Claim 1 is allowable over the admitted prior art in view of Vassiliadis et al. Claims 2-7, which depend from Claim 1, are allowable for at least the same reasons as Claim 1.

In addition, Claim 4 recites "multiplexer select means coupled to said first and second multiplexers ... wherein said multiplexer select means [in said second state] causes said

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first multiplexer to <u>route said first data value to said ALU</u> and causes said second multiplexer to <u>route said second data value to said ALU</u>." (Emphasis added.) This advantageously allows the ALU to either add "said carry and sum signals to create a third data value equal to the product of said first and second data values" as recited in Claim 1 <u>or</u> to receive "said first data value" and "said second data value."

The admitted prior art fails to teach or suggest "multiplexer select means" as recited in Claim 4. The admitted prior art has no need for such "multiplexer select means" because multiplier 100 utilizes a carry propagate adder 118 to add the carry and sum signals. That is, multiplier 100 performs <u>complete</u> multiplication operations.

Vassiliadis et al. do not remedy the shortcomings of the admitted prior art. Vassiliadis et al. fail to teach "multiplexer select means coupled to" a "first multiplexer" and a "second multiplexer." As a result, Vassiliadis et al. do not teach or suggest such "multiplexer select means" but rather teach that "[t]he <u>sum</u> ... be <u>directly wired to one of the inputs to the CLA</u>." (Emphasis added.) (Vassiliadis et al., Col. 15, lines 62-63). Thus, Vassiliadis et al. fail to teach or suggest an ALU which is both "capable of adding said carry and sum signals to create a third data value equal to the product of said first and second data values" as recited in Claim 1 and which also comprises "multiplexer select means" which "causes said first multiplexer to route said first data value to said ALU and causes said second multiplexer to route said second data value to said ALU when said multiplexer select means is in said second state" as recited in Claim 4.

For these additional reasons, Claim 4 is allowable over the admitted prior art in view of Vassiliadis et al. Claim 7 which recites "multiplexer select means" is allowable over the admitted prior art in view of Vassiliadis et al. for reasons

similar to those previously described in connection with Claim 4.

Claim 8 is allowable for reasons similar to those previously presented in connection with Claims 1 and 4.

Claim 9 recites "[a] method of multiplying" which includes the step of "adding said carry and sum signals within said ALU to create a third data value equal to the product of said first and second data values". The admitted prior art, which adds carry and sum signals within carry propagate adder 118, does not teach the step of "adding ... within said ALU" as recited in Claim 9. (Emphasis added.) Vassiliadis et al., which is directed toward a specific set of addition, subtraction and logic operations, does not teach or suggest multiplication. Because Vassiliadis et al. is not directed toward a multiplier, no motivation exists to combine Vassiliadis et al. with the admitted prior art. Claim 9 therefore is allowable over the admitted prior art in view of Vassiliadis et al.

Claim 10 is allowable for reasons similar to those set forth above in connection with Claim 1. More specifically, the admitted prior art fails to teach or suggest the steps of "routing said carry signal through said first multiplexer to said ALU in response to said multiplexer control signal" and "routing said sum signal through said second multiplexer to said ALU in response to said multiplexer control signal" as recited in Claim 10. (Emphasis added.) This is because the multiplier 100 of the admitted prior art performs complete multiplication operations.

Vassiliadis et al. do not remedy the shortcomings of the admitted prior art. On the contrary, as discussed previously, Vassiliadis et al. teach that "[t]he sum ... be directly wired to one of the inputs to the CLA." (Emphasis added.) (Vassiliadis et al., Col. 15, lines 62-63).

For these reasons, Claim 10 is allowable over the admitted prior art and Vassiliadis et al. Claim 11, which depends from

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Claim 10, is allowable for at least the same reasons as Claim 10 and also for reasons similar to those set forth above in connection with Claim 4.

Applicant has added Claim 12. Claim 12 is allowable over the admitted prior art and Vassiliadis et al. for at least the following reasons. Claim 12 recites "<u>a first mode and a second mode</u>." (Emphasis added.) In "the first mode, the ALU adds the carry and sum signals to create a third data value equal to the product of the first and second data values." In "the second mode, the first selector circuit passes the first data value and the second selector circuit passes the second data value." This advantageously allows the ALU to either "create a third data value equal to the product of the first and second data values" <u>or</u> to receive "the first and second data values."

The admitted prior art fails to teach or suggest such "<u>a first and a second mode</u>." (Emphasis added.) The admitted prior art has no need for a first and a second mode because multiplier 100 utilizes a carry propagate adder 118 to add the carry and sum signals. Thus, multiplier 100 performs <u>complete</u> multiplication operations.

Vassiliadis et al. do not remedy the shortcomings of the admitted prior art. Vassiliadis et al. fail to teach or suggest a "first mode" in which an ALU "adds the carry and sum signals to create a third data value equal to the product of the first and second data values" and a "second mode" in which an ALU "receives the signals [, the first and second data values,] passed by the first and second selector circuits" as recited in Claim 12. (See, Figs. 6, 7, 8, and 9 of Vassiliadis et al.)

For these reasons, Claim 12 is allowable over the admitted prior art and Vassiliadis et al. Claim 12 is also allowable for reasons similar to those set forth above in connection with Claims 1 and 4.

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Claims 1-11 were pending in the present application and stand rejected. Claims 1-2, 5-6, and 8-10 have been amended; and Claim 12 has been added. For the reasons presented above, Applicant respectfully requests reconsideration and allowance of pending Claims 1-12. If there are any questions, please telephone the undersigned at (408) 453-9200 ext. 1204 to expedite prosecution of this case.
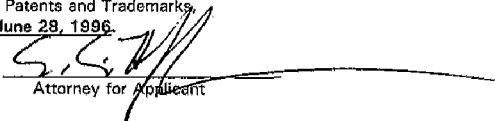
Respectfully submitted,

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Date of Signature   Attorney for Applicant

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