Exhibit H

Exhibit to the Declaration of Aaron R. Fahrenkrog in Support of Plaintiffs' Opening Claim Construction Brief

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Pearl Po-Yee Cheng et al.

Assignee: Advanced Micro Devices, Inc.

Title: "MEMORIES HAVING A BURST MODE SEQUENTIAL ACCESS"

Serial No.: 08/328,337 Filing Date: 10/24/94

Examiner: S. Nadig Group Art Unit: 2312

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San Jose, California
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COMMISSIONER OF PATENTS AND TRADEMARKS
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AMENDMENT AFTER FINAL OFFICE ACTION (37 C.F.R. 1.312)

Sir:

In response to the Office Action dated January 27, 1995, please amend the above-identified application as follows:

IN THE TITLE

Please replace the title to read --MEMORIES HAVING A BURST MODE SEQUENTIAL ACCESS--.

IN THE SPECIFICATION

Page 5, line 20, replace "330.L" by --320.L--.

IN THE CLAIMS

1. (Twice Amended) A memory comprising:

a plurality of rows of memory locations;

a plurality of first registers, each first register for receiving a row address;

a plurality of row decoders, each row decoder for activating a portion of a row identified by signals from one of said first registers;

one or more sense amplifiers for amplifying contents of said memory locations in the row portions; and

an output for providing output signals from said

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sense amplifiers,

wherein at least two locations L1 and L2 in different rows having different row addresses in [of] said memory can be read out to said output in burst mode such that the memory receives an address of one of said locations and provides in response contents of a plurality of memory locations, including the locations L1 and L2, in the sequence of consecutive addresses, so that while one of said row decoders is activating a row portion comprising said location L1 and contents of said location L1 are being transferred from one or more of said sense amplifiers to said output, another one of said row decoders is activating a row portion comprising said location L2 and contents of said location L2 are being transferred from said location L2 to one or more of said sense amplifiers.

13. (Amended) The memory of Claim 12 wherein when the locations L1 and L2 are read out in burst mode and when the contents of said location L1 are being transferred from one or more of said sense amplifiers to said output and the contents of said location L2 are being transferred from said location L2 to one or more of said sense amplifiers, the sense amplifiers from which the contents of said location L1 are being transferred are enabled and the sense amplifiers to which the contents of said location L2 are being transferred are disabled, but these latter sense amplifiers become enabled subsequently for amplifying the contents of said location L2.

14. (Twice Amended) In a memory having a plurality of rows of memory locations and having a plurality of row decoders and one X-register for each said row decoder, a method of reading in a burst mode operation a plurality of consecutively addressed memory locations spanning more than one row, said

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method comprising the steps of:

providing to said X-registers a row address of a first location to be read in said burst mode operation;

for each row containing a location to be read in said burst mode operation, performing the steps of:

providing by at least one of the X-registers to at least one of the row decoders signals identifying said row;

activating by one of said row decoders at least a portion of said row;

sensing and amplifying contents of at least one location of said row; and

transferring amplified contents of at least one location of said row to an output of said memory;

wherein for at least two locations L1 and L2 of said plurality which are in different rows <u>having different row addresses in</u> [of] said memory, the step of sensing and amplifying the contents of said location L2 overlaps in time with the step of transferring the amplified contents of said location L1 to said output of said memory.

<u>REMARKS</u>

Claims 2-26 are pending in the application and stand rejected. Claims 2, 4 and 14 are amended. Reconsideration and withdrawal of the rejections are respectfully requested.

The Office Action objects to the title of the application. The title is amended to overcome the objection.

Claim 2-14 and 18-20 are rejected under 35 U.S.C. 102(b) over Pinkham. Claims 14-17 and 21-26 are rejected under 35 U.S.C. 103 over Pinkham in view of Rao. These rejections are respectfully traversed.

Claim 2 distinguishes from Pinkham and Rao, taken singly or together, by reciting a burst mode in which a memory receives an address of one location and provides in response

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contents of a plurality of locations in rows having different row addresses.

Claim 2 is supported by Applicants' specification, page 6, line 12 and page 8, lines 5-13. In the burst mode operation described therein, a memory receives, on lines A0-A4, the address of location M-1 (specification, page 6, line 12). The memory provides in response the contents of a plurality of locations including: (1) location M-12 having a row address 1, and (2) location M-16 having a row address 2 (specification, page 8, lines 5-13).

The Office Action erroneously states in page 3:

> A burst mode transfer is nothing more than a beginning mode address and an ending address which is equivalent to serial transfer ... .

This is incorrect. A burst mode transfer as claimed in Claim 2 is not any serial transfer but a serial transfer in which the contents of a plurality of locations are provided in response to the address of one location. The contents of a plurality of locations could be provided in response to the addresses of the plurality of locations in a serial transfer. Each location could be read out in response to its respective address. Such a serial transfer would not be a burst mode transfer as claimed in Claim 2.

In Pinkham, in response to an address A0-A7 (Fig. 1), the data "in the addressed row" are transferred to a shift register for serial output (col. 5, lines 19-20). While Pinkham teaches transferring data in one "address row", Pinkham does not teach or suggest transferring data in different rows having different row addresses in response to the same address A0-A7 as recited in Claim 2. Thus, Pinkham does not teach or suggest Applicants' invention.

Rao is no more pertinent to Claim 2 than Pinkham. Rao's memory receives an address on inputs 15, 19, 32 (Fig. 1). Bits from a "selected row" of the memory are moved to a shift

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register and then to an output line (col. 4, lines 19-22). Rao does not teach or suggest that bits from different rows having different row addresses can be moved out in response to the same address on inputs 15, 19, 32 (Fig. 1) as recited in Claim 2. Claim 2 and its dependent Claims 3-6, 18, and 19 are therefore believed to be allowable.

Claim 4 dependent from Claim 2 further distinguishes from Pinkham and Rao, taken singly or together, by reciting that when the contents of a location L1 are being transferred in burst mode from one or more sense amplifiers to the memory output and the contents of another location L2 are being transferred from L2 to one or more sense amplifiers, the sense amplifiers from which the contents of L1 are being transferred are enabled and the sense amplifiers to which the contents of L2 are being transferred are disabled, but these latter sense amplifiers become enabled subsequently for amplifying the contents of L2.

Claim 4 is supported by the specification, page 8, line 23 through page 9, line 11. In some burst mode transfers, sense amplifier 330.R-2 (Fig. 3B) is enabled when the contents of location M-14 are being transferred from this sense amplifier to the memory output DOUT. At the same time, the contents of location M-18 (Fig. 3A) are being transferred to sense amplifier 330.L-2, but sense amplifier 330.L-2 is disabled. *See* page 9, lines 1-4. Sense amplifier 330.L-2 becomes enabled subsequently in the same transfer to amplify the contents of M-18. Disabling the sense amplifier 330.L-2 during part of the burst mode transfer "provides significant power saving". Specification, page 9, line 8.

Pinkham stores data "in the output of the associated sense amps" (col. 15, lines 38-39), and places the data "on the input of the shift bits" (col. 15, lines 47-48). The bits are subsequently shifted out (col. 15, lines 54-55). Pinkham does not teach or suggest a burst mode transfer in which one of his

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sense amps is enabled and another sense amp is disabled but becomes enabled subsequently in the same transfer, as recited in Claim 4. Thus, Pinkham does not teach or suggest Applicants' invention and does not provide the attendant advantage of power saving.

Rao actuates his sense amplifiers 11 (Fig. 1) to move bits of a selected row into a shift register (col. 4, lines 16 and 19-21). Rao does not teach or suggest a burst mode transfer in which one of his sense amplifiers 11 is enabled and another sense amplifier is disabled but becomes enabled subsequently in the same transfer as recited in Claim 4. Thus, Rao is no more pertinent to Claim 4 than Pinkham. Claim 4 is believed to be allowable for this additional reason.

Claim 7 distinguishes from Pinkham and Rao, taken singly or together, by reciting a burst mode operation in which while the contents of one location are being transferred from a sense amplifier means to a memory output, the contents of another location are being provided to the sense amplifier means for amplification and subsequent transfer to the output.

In Pinkham, "the data is stored in the output of the associated sense amps", and "shifted out" (col. 15, lines 38-39 and 54). Pinkham does not teach or suggest a burst mode operation in which while one bit of data is shifted out, another bit is being provided to a sense amp for amplification as recited in Claim 7. Thus, Pinkham does not teach or suggest Applicants' invention.

Rao also does not teach or suggest a burst mode operation such that while any one of his bits is moved to the output line, another bit is provided to a sense amplifier 11 for amplification as recited in Claim 7. *See* Rao's col. 4, lines 19-21 and 23. Thus, Rao is no more pertinent to Claim 7 than Pinkham. Claim 7 and its dependent Claims 8-13 and 20 are therefore believed to be allowable.

Claim 14 and its dependent Claims 15, 21 and 22 are

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believed to be allowable for reasons similar to the reasons discussed above in connection with Claim 2.

In addition, Claim 15 is believed to be allowable for reasons similar to the reasons discussed above in connection with Claim 4.

Claim 16 and its dependent Claim 17 are believed to be allowable for reasons similar to the reasons discussed above in connection with Claim 7.

In addition Claim 17 is believed to be allowable for reasons similar to the reasons discussed above in connection with Claim 4.

Claim 23 distinguishes from Pinkham and Rao, taken singly or together, by reciting: (1) a plurality of subarrays each of which comprises groups of columns; (2) an X-decoder for each subarray; and (3) a Y-select circuit for each subarray to select all the columns that occupy a selected position in the groups of the subarray.

Claim 23 is supported by Figs. 3A, 3B. Subarray 314.L includes column groups 0 through 3. Subarray 314.R includes column groups 4 through 7. X-decoders 316.L, 316.R are provided for respective subarrays 314.L, 314.R. Y-select circuit 320.L of subarray 314.L selects either the first columns in each group 0 through 3 or the second columns, that is, either the columns in position 1 or in position 2. *See* Applicants' specification, page 5, lines 20-22. Y-select circuit 320.R of subarray 314.R also selects either the columns in position 1 or the columns in position 2 (page 5, lines 31-33).

In Rao's array 10a (Fig. 1), Y decoder 16 selects only one column (Rao, col. 3, line 46) rather than all the columns in a given position as recited in Claim 23.

Rao's arrays 10b-10d "are constructed for only serial access" (col. 7, lines 1-2) and thus do not provide column selection. However, suppose for the sake of argument that

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Rao's serial access of any one of arrays 10b-10d for example, of array 10b, implies selection of all the columns of the respective array. Suppose also, for the sake of argument, that the Claim 23 selection of all the columns that occupy a selected position in the groups reads on Rao's selection of all the columns of array 10b during serial access. Then if Claim 23 were read on Rao, the Claim 23 columns that occupy a selected position in the groups would correspond to columns of Rao's array 10b. Since each group in Claim 23 has columns in other positions besides the selected position, in Rao a group would have columns in at least one other array 10a, 10c, 10d besides columns in array 10b. Since each group of Claim 23 belongs to a subarray, a subarray in Rao would have columns both in array 10b and in at least in at least one of the other arrays 10a, 10c, 10d. However, Claim 23 recites an "X-decoder" for each subarray, and Rao does not have an X-decoder for a subarray that includes columns both in array 10b and in at least one of the other arrays 10a, 10c, 10d. Indeed, each X-decoder 12 of Rao is associated with only one of arrays 10a-10d (col. 3, lines 38-39) and not with columns in different ones of arrays 10a-10d. Thus, Rao does not teach or suggest Applicants' invention.

Pinkham is no more pertinent to Claim 23 than Rao. Claim 23 and its dependent Claims 24-26 are therefore believed to be allowable.

In addition, Claim 25 is believed to be allowable for reasons similar to the reasons discussed above in connection with Claim 7.

The specification is amended to correct a typographical error and conform the specification to Fig. 3A.

The present amendment merely clarifies the claims and does not raise new issues that would require further consideration or search. More particularly, Claim 2 is amended to recite that certain different rows have different row addresses. This

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is merely a clarification that does not raise new issues.

The amendment to Claim 4 clarifies that a transfer recited therein takes place in burst mode. Claim 4 depends from Claim 2, and Claim 2 already recited, before the present amendment, that the transfer took place in burst mode. Thus, the amendment to Claim 4 also does not raise new issues.

The amendment to Claim 14 does not raise new issues for reasons similar to the reasons discussed above in connection with Claim 2.

In summary, Claims 2-26 are pending in the application and stand rejected. Claims 2-26 are believed to be allowable, and early passage of this case to issue is respectfully requested. If any matters remain outstanding after consideration of this amendment, the Examiner is requested to telephone the undersigned at the number below to expedite prosecution of this case.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C., 20231, on April 27, 1995.

4-27-95 Michael Shenker

Date of Signature Attorney for Applicants

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