Exhibit I

Exhibit to the Declaration of Aaron R. Fahrenkrog in Support of Plaintiffs' Opening Claim Construction Brief

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Pearl Po-Yee Cheng et al.

Assignee: Advanced Micro Devices, Inc.

Title: MEMORIES HAVING A BURST MODE SEQUENTIAL ACCESS

Serial No.: 08/328,337 Filed: 10/24/94

Examiner: S. Nadig Group Art Unit: 2312

Attorney Docket No.: M-2013-1C US

#37
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San Jose, California
September 27, 1995

COMMISSIONER OF PATENTS AND TRADEMARKS
BOX AF
Washington, D. C. 20231

APPEAL BRIEF TRANSMITTAL

Sir:

Pursuant to Rule 37 CFR 1.191 and 1.192, Applicants herewith submit the Appeal Brief and Appendix (in triplicate) in the above-identified application. The Notice of Appeal for this application was mailed to the Patent Office on May 30, 1995. Pursuant to Rule 37 CFR 1.17(f), the Commissioner is hereby authorized to charge our Deposit Account No. 19-2386 in the amount of $270.00 for filing the above documents, and any other fees which may be required to complete the filing.

This transmittal is being submitted in triplicate.

Respectfully submitted,

Michael Shenker

Michael Shenker
Attorney for Applicant(s)
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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C., 20231, on September 27, 1995.

9-27-95 Michael Shenker

Date of Signature Attorney for Applicant(s)

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APPEAL BRIEF

Sir:

This Appeal Brief follows the Notice of Appeal filed by Applicants on May 30, 1995 in the above-identified application.

REAL PARTY IN INTEREST

The real party in interest is Advanced Micro Devices, Inc., a corporation having a place of business in Sunnyvale, California.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF CLAIMS

Claim 1 is cancelled.

Claims 2-26 are rejected. The rejection of Claims 2-26 is being appealed in this appeal.

STATUS OF AMENDMENTS

An AMENDMENT AFTER FINAL OFFICE ACTION was filed on April 27, 1995. The Advisory Action mailed May 18, 1995 indicated that that amendment would be entered upon filing an appeal.

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A SECOND AMENDMENT AFTER FINAL OFFICE ACTION and a PROPOSED AMENDMENT TO DRAWINGS are being filed with this Appeal Brief. The SECOND AMENDMENT corrects errors in the specification and does not amend the claims.

SUMMARY OF THE INVENTION

Applicants' invention is directed to memories having a burst mode access. Burst mode access is a sequential access in which the memory receives the address of one memory location and provides in response the contents of a plurality of consecutive memory locations. Burst mode access is sometimes faster than "random" access in which a separate address is provided to the memory for each location to be accessed.

A prior art memory having a burst mode access is illustrated in Fig. 2. In this memory, four locations in the same memory row can be read in burst mode in response to one address.

§ 1. According to one feature of Applicants' invention, memory locations in different rows having different row addresses can be read in burst mode in response to one address. This feature is recited in Claim 2, lines 12-16.

Some embodiments having this feature are illustrated in Figs. 3A, 3B. The memory of Figs. 3A, 3B has two rows. The first row, of locations M-0 through M-15, has row address 0. The second row, of locations M-16 through M-31, has row address 1. A burst mode read operation described in Applicants' specification, page 6, line 13 through page 8, line 14 accesses locations M-12 through M-15 in row 0 (page 8, line 1) and locations M-16 through M-19 in row 1 (page 8, lines 8-9). Thus, fast sequential access is provided to memory locations in different rows having different row addresses.

§ 2. Another patentable feature of Applicants' burst mode is that while the contents of one memory location are being transferred from sense amplifiers to the memory output, the contents of another location are being transferred from this

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other location to the sense amplifiers. This feature is recited in the last eight lines of Claim 2.

In the embodiment of Fig. 4, during time period t5 the contents of locations M-12 through M-15 are transferred from sense amplifier circuits 330.R-0 through 330.R-3 to the memory output DOUT (page 8, lines 11-13). At the same time, the contents of locations M-16 through M-19 are transferred to sense amplifier circuits 330.L-0 through 330.L-3 (page 8, lines 8-10) in preparation for transfer to the memory output. Overlapping the transfer to the sense amplifier circuits for some locations with the transfer to the memory output for other locations makes the reading operation faster.

Due to this feature, in some embodiments the time needed to transfer the contents of a location to the sense amplifier circuits does not contribute to the total reading time for each location starting with the second location to be read in burst mode. Thus, in some embodiments, every location starting with the second location is read out within the time "tOE" that it takes to transfer the contents of the location from sense amplifier circuits to the memory output. Some such embodiments are covered by Claim 13. *See* the last six lines of Claim 13.

§ 3. According to another feature of Applicants' invention, one or more sense amplifiers that participate in a burst mode operation are disabled during part of the operation. *See* the last six lines of Claim 4.

Some embodiments having this feature are described in page 8, line 23 through page 9, line 4. An advantage of some such embodiments is explained in page 9, lines 4-11 as follows:

> Since sense amplifier circuits have a large power consumption (in some embodiments, 50% of the entire power consumed by the memory), disabling some sense amplifier circuits during burst mode access provides significant power saving. Alternatively, the power consumption in each sense amplifier can be increased to provide higher speed at the expense of smaller or no power saving.

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§ 4. Another feature of Applicants' burst mode is wrap-around. This feature is recited in Claim 7, line 12. Referring to the embodiment of Figs. 3A, 3B, the specification explains in page 8, lines 16-22:

> The burst mode read can wrap around so that after reading the last location M-31, locations starting with M-0 can be read in sequence. Thus memory 310 allows boundaryless burst mode access in which any number of consecutive locations, starting with any location, can be read in one burst mode operation.

§ 5. Another feature of Applicants' invention is recited in Claim 23. Claim 23 recites: (1) a plurality of subarrays each of which comprises groups of columns; (2) a Y-decoder for each subarray; and (3) a Y-select circuit for each subarray, the Y-select circuit being responsive to the Y-decoder of the subarray to select all the columns that occupy a selected position in the groups of the subarray.

In the embodiments of Figs. 3A, 3B, subarray 314.L includes column groups 0 through 3 (specification, page 4, lines 30-31). Subarray 314.R includes column groups 4 through 7. Y-decoders 318.L, 318.R are provided for respective subarrays 314.L, 314.R. Y-select circuit 320.L of subarray 314.L selects either the first columns in each group 0 through 3, or the second columns, that is, either the columns in position 1 or the columns in position 2 (page 5, lines 20-22). Y-select circuit 320.R of subarray 314.R also selects either the columns in position 1 or the columns in position 2 (page 5, lines 31-33).

ISSUES

Issue 1 is whether Claims 2-14 and 18-20 are unpatentable under 35 U.S.C. 102(b) over Pinkham.

Issue 2 is whether Claims 14-17 and 21-26 are unpatentable under 35 U.S.C. 103 over Pinkham in view of Rao.

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GROUPINGS OF CLAIMS

ISSUE 1

With respect to Issue 1, the claims of each of the following Groups I through VIII stand or fall together; the claims of each of Groups I through VIII are separately patentable from the claims of every other one of Groups I through VIII.

Group I consists of Claims 2, 3, 18 and 19.

Group II consists of Claim 4.

Group III consists of Claim 5.

Group IV consists of Claim 6.

Group V consists of Claims 7-9, 11, 12 and 20.

Group VI consists of Claim 10.

Group VII consists of Claim 13.

Group VIII consists of Claim 14.

ISSUE 2

With respect to Issue 2, the claims of each of the following Groups IX through XIII stand or fall together; the claims of each of Groups IX through XIII are separately patentable from the claims of every other one of Groups IX through XIII.

Group IX consists of Claims 14, 21 and 22.

Group X consists of Claim 16.

Group XI consists of Claims 15 and 17.

Group XII consists of Claims 23, 24 and 26.

Group XIII consists of Claim 25.

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ARGUMENT

A. ISSUE 1 -- whether Claims 2-14 and 18-20 are unpatentable under 35 U.S.C. 102(b) over Pinkham.

A.1. Claims 2, 3, 18 and 19 (Group I)

A.1.1. Claim 2 distinguishes from Pinkham by reciting, in lines 12-16, a burst mode in which a memory receives an address of one location and provides in response contents of a plurality of locations in different rows having "different row addresses".

Claim 2 is supported by Applicants' specification, pages 6-8. In a burst mode operation described therein, the memory of Figs. 3A, 3B receives, on lines A0-A4, the address of location M-1 (page 6, line 12). The memory provides in response the contents of a plurality of locations including: (1) location M-12 in the first row having a row address 0 (page 8, line 13), and (2) location M-16 in the second row having a row address 1 (page 8, line 8). (The row address is given by the most significant address bit, such as bit A4 for the address A0-A4. *See* page 6, lines 16-17.)

In Pinkham, in response to an address A0-A7 (Fig. 1 and col. 4, line 32), data "in the addressed row" are transferred to a shift register for serial output (col. 5, lines 19-20). Pinkham transfers data in one "addressed row", and does not teach or suggest transferring data in different rows having different row addresses in response to the same address A0-A7 as recited in Claim 2.

A.1.2. In addition, Claim 2 distinguishes from Pinkham by reciting that, in burst mode, while the contents of a location L1 are being transferred from one or more sense amplifiers to a memory output, the contents of another location L2 in a differently addressed memory row are being transferred from L2

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to one or more sense amplifiers. *See* Claim 2, lines 12-13 and 18-25.

This recitation is supported by Figs. 3A, 3B and 4. L1 reads on location M-12 in memory row 0 (Fig. 3B). L2 reads on M-16 in row 1 (Fig. 3A). During time period t4 (Fig. 4), the contents of M-12 in row 0 are transferred from M-12 to sense amplifier circuit 330.R-0 (page 8, lines 1-3). Then, during time period t5:

(1) the contents of M-12 are transferred from sense amplifier circuit 330.R-0 to memory output DOUT (page 8, lines 11-13), and

(2) at the same time, the contents of M-16 in row 1 are transferred from M-16 to sense amplifier circuit 330.L-0 (page 8, lines 8-10).

The burst mode read is fast as a result.

Pinkham does not teach or suggest simultaneous transfer in different memory rows for locations to be read out in response to the same address A0-A7 as recited in Claim 2. Claim 2 and its dependent Claims 3-6, 18 and 19 are therefore believed to be allowable over Pinkham.

A.2. Claim 4 (Group II)

Claim 4 dependent from Claim 2 is separately patentable over Pinkham because Claim 4 recites that in a burst mode read of locations L1 and L2, the sense amplifiers from which the contents of L1 are being transferred to the memory output are enabled while other sense amplifiers are disabled, but these latter sense amplifiers become enabled subsequently for amplifying the contents of L2. *See* the last six lines of Claim 4.

Claim 4 is supported by the specification, page 8, line 23 through page 9, line 11. In a burst mode read of Fig. 4, during time period t5 sense amplifier circuit 330.R-2 is enabled when the contents of M-14 are being read from this

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sense amplifier circuit to the memory output DOUT (page 8, lines 11-13 and page 9, lines 1-3). At the same time, sense amplifier circuit 330.L-2 is disabled (page 9, lines 3-4). However, word line WL.L-1 is asserted to transfer the contents of M-18 to sense amplifier circuit 330.L-2 (page 8, lines 5-10). Sense amplifier circuit 330.L-2 becomes enabled subsequently in the same burst mode operation to amplify the contents of M-18. Disabling the sense amplifier circuit 330.L-2 during part of the burst mode operation "provides significant power saving" (page 9, line 8).

In Pinkham, data are transferred to "the output of the associated sense amps" (col. 15, lines 38-39), then to "the input of the shift bits" (col. 15, line 48), and then are shifted out (col. 15, lines 53-55). Pinkham does not teach or suggest that in this operation one of his sense amps is enabled and another sense amp is disabled but becomes enabled subsequently in the same operation, as recited in Claim 4. Claim 4 is therefore separately patentable over Pinkham.

A.3. Claim 5 (Group III)

Claim 5 dependent from Claim 2 is separately patentable over Pinkham because, as explained below, Claim 5 recites (in line 9) a timing relationship not recited in Claim 2 and not taught or suggested by Pinkham.

Claim 5 reads on Applicants' Figs. 3A, 3B, 6 and 7 as follows. Pluralities S-1, ..., S-k of Claim 5 read on respective subarrays 314.L, 314.R of Figs. 3A, 3B (with k=2) and on subarrays 1 through k of Fig. 7. The sense amplifiers for each plurality S-i of Claim 5 read: (1) in Figs. 3A, 3B, on sense amplifier circuits 330.L-0 through 330.L-3 for subarray 314.L, and sense amplifier circuits 330.R-0 through 330.R-3 for subarray 314.R (m=4 in Figs. 3A, 3B); and (2) in Fig. 7, on sense amplifier circuits 330.i for each subarray i.

The time tARA of Claim 5 reads on tARA of Fig. 6. The

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time tOE reads on tOE of Fig. 6. Specification, page 10, lines 13-19.

Claim 5 is separately patentable over Pinkham because Claim 5 recites, in line 9, the following timing relationship for a sequential read of locations in different rows having different row addresses:

tARA does not exceed m * (k-1) * (tOE).

This recitation is supported by page 11, line 8 for Fig. 7 and by page 10, line 22 for Figs. 3A, 3B. This timing relationship enables one in some embodiments to read each datum starting with the second "within time tOE" which is the time to transfer a sense amplifier output to the memory output, rather than within a larger time tARA+tOE. Specification, page 10, line 21.

Pinkham does not teach or suggest such a timing relationship for a sequential read operation covering locations in different rows having different row addresses as in Claim 5. Claim 5 is therefore separately patentable over Pinkham.

A.4. Claim 6 (Group IV)

Claim 6 dependent from Claim 2 is separately patentable over Pinkham because Claim 6 recites, for a sequential read of locations in different rows having different row addresses, that a time in which each location except one particular location is read out to the memory output after a previous location has been read out to the output is shorter than the time in which the one particular location is read out to the output.

Claim 6 is supported by page 10, lines 12-13 and 21. As explained therein, the first data output is provided after time tARA+tOE. Each subsequent datum is read out within shorter time tOE.

Pinkham does not teach or suggest such timing for a sequential read of locations in different rows having different

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row addresses as in Claim 6. Claim 6 is therefore separately patentable over Pinkham.

A.5. Claim 7-9, 11, 12 and 20 (Group V)

Claim 7 is separately patentable over Pinkham because Claim 7 recites a burst mode operation combining the following features.

A.5.1. One feature is that a plurality of consecutively addressed locations L1 through Ln are read with "wrap around" so that the next location, if any, to be read out after the location Ln is the first location L1. *See* lines 11-13 of Claim 7.

This feature is supported by the specification, page 8, line 16-19. *See* SUMMARY OF THE INVENTION § 4, above.

A.5.2. The second feature is a burst mode operation in which while the contents of one location are being transferred from a sense amplifier means to a memory output, the contents of another location to be read in response to the same address are being provided to the sense amplifier means for amplification and subsequent transfer to the output. *See* the last seven lines of Claim 7.

This feature is supported by the original disclosure, as explained above in section A.1.2 (in connection with Claim 2).

In Pinkham, in response to an address A0-A7, "the data is stored in the output of the associated sense amps", and then "shifted out" (col. 15, lines 38-39 and 54). Pinkham does not teach or suggest that while one bit of data is shifted out in response to A0-A7, another bit to be read in response to the same address A0-A7 in a serial read with wrap-around is provided to a sense amp as recited in Claim 7. Claim 7 and its dependent Claims 8-13 and 20 are therefore believed to be allowable.

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A.6. Claim 10 (Group VI)

Claim 10 dependent from Claim 7 is separately patentable over Pinkham because Claim 10 recites, in lines 8-9, a timing relationship, similar to that of Claim 5, for a sequential read with wrap-around.

Pinkham does not teach or suggest such a timing relationship for a sequential read with wrap-around.

A.7. Claim 13 (Group VII)

Claim 13 dependent from Claim 7 is separately patentable over Pinkham because Claim 13 recites that:

(1) the first location to be read out in a burst mode operation is read out to the memory output after time tARA+tOE (lines 4-5 of Claim 13), and

(2) every other location is read out within time tOE (last two lines of Claim 13).

Pinkham does not teach or suggest such timing for a sequential read with wrap-around.

A.8. Claim 14 (Group VIII)

A.8.1. Claim 14 distinguishes from Pinkham because Claim 14 recites reading, in a burst mode operation, memory locations in different rows having different row addresses (*see* lines 4 and 21-22). Thus, Claim 14 is believed to be allowable for reasons similar to the reasons given above in Section A.1.1 in connection with Claim 2.

A.8.2. Claim 14 is separately patentable over Pinkham because Claim 14 recites, in the last four lines, that the step of "sensing and amplifying" the contents of a location L2 in one row "overlaps in time" with the step of transferring to the memory output the amplified contents of a location L1 in a different row having a different row address.

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This recitation is supported by Figs. 3A, 3B and 4. More particularly, during time period t5 of Fig. 4:

(1) the contents of M-12 through M-15 in row 0 are transferred from respective sense amplifiers circuits 330.R-0 through 330.R-3 to memory output DOUT (page 8, lines 11-13), and

(2) at the same time, word line WL.L-1 of row 1 is asserted, and the contents of M-16 through M-19 in row 1 are transferred to respective sense amplifier circuits 330.L-0 through 330.L-3 (page 8, lines 6-10).

Moreover, when the contents of M-14 are transferred from respective sense amplifier circuit 330.R-2 to the memory output, sense amplifier circuits 330.L-0 and 330.L-1 are enabled (page 9, lines 1-3) to sense and amplify the contents of respective locations M-16, M-17. Thus, the step of sensing and amplifying the contents of M-16, M-17 overlaps in time with the step of transferring to the memory output the amplified contents of M-14.

Pinkham does not teach or suggest overlapping in time in different memory rows as recited in Claim 14. Claim 14 is therefore believed to be allowable.

B. ISSUE 2 -- whether Claims 14-17 and 21-26 are unpatentable under 35 U.S.C. 103 over Pinkham in view of Rao.

B.1. Claims 14, 21 and 22 (Group IX)

Claim 14 distinguishes from Pinkham and Rao, taken singly or together, by reciting "reading in a burst mode operation ... memory locations ... in different rows having different row addresses" (lines 3-5 and 21-22).

Pinkham does not teach or suggest the invention of Claim 14. *See* section A.9.1 above.

Rao is no more pertinent than Pinkham. Rao's "serial read operation" is described in Rao's col. 4, lines 12-24. In that

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operation, in response to "an address on the inputs 15" (col. 4, line 13), Rao's memory provides bits from a single "selected row" (col. 4, line 20) rather than from different rows having different row addresses as recited in Claim 14. Thus, Rao and Pinkham, taken singly or together, do not teach or suggest a burst mode operation accessing different rows having different row addresses as recited in Claim 14.

Moreover, Claim 14 distinguishes from Pinkham and Rao, taken singly or together, by reciting, in the last four lines, that the step of "sensing and amplifying" the contents of a location L2 in one row "overlaps in time" with the step of transferring to the memory output the amplified contents of a location L1 in a different row having a different row address.

Pinkham does not teach or suggest overlapping in time for different memory rows as recited in Claim 14. *See* section A.9.2, above.

Rao also does not teach or suggest such overlapping in time, and thus is no more pertinent than Pinkham. Claim 14 and its dependent Claims 15, 21, and 22 are therefore believed to be allowable.

B.2. Claim 16 (Group X)

Claim 16 is separately patentable over Pinkham and Rao because Claim 16 recites a burst mode read with "wrap around" in which, for a location L and another location to be read in response to the same address, the step of transferring amplified contents of location L to a memory output "overlaps in time" with the step of sensing and amplifying the contents of the other location. *See* lines 4, 9-14 and 16-19 of Claim 16.

Claim 16 is supported by the specification, page 8, lines 16-19 and page 9, lines 1-3. In particular, page 9, lines 1-3 state that when sense amplifier circuit 330.R-2 is read to the memory output to provide the contents of one location, sense

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amplifier circuit 330.L-0 is enabled to sense and amplify the contents of another location. *See* also page 8, lines 28-32.

In Pinkham, in response to an address A0-A7, "the data is stored in the output of the associated sense amps", and then "shifted out" (col. 15, lines 38-39 and 54). Pinkham does not teach or suggest that the step of shifting out a bit of data in response to address A0-A7 overlaps in time with the step of sensing and amplifying another bit to be read in response to the same A0-A7 in a sequential read with wrap-around, as recited in Claim 16.

Rao also does not teach or suggest that in his "serial read operation", the step of moving a data bit to his output line overlaps in time with the step of sensing and amplifying another bit by his sense amplifiers 11, or that his "sequential read" is performed with wrap-around as recited in Claim 16. *See* Rao's col. 4, lines 12-24 describing Rao's "serial read operation." Claim 16 and its dependent Claim 17 are therefore believed to be allowable.

B.3. Claims 15 and 17 (Group XI)

Claim 15 dependent from Claim 14 is separately patentable because Claim 15 recites that, in burst mode, a sense amplifier circuit for sensing and amplifying the contents of a location LL1 is enabled and a sense amplifier circuit for sensing and amplifying the contents of another location LL2 is disabled, but this latter sense amplifier circuit is enabled subsequently during the step of sensing and amplifying the contents of LL2. *See* the last eight lines of Claim 15.

Claim 15 is supported by the original disclosure as discussed above in section A.2 (in connection with Claim 4) and in SUMMARY OF THE INVENTION § 3. As discussed therein, some embodiments of Claim 15 provide "significant power saving" (specification, page 9, line 8).

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Pinkham does not teach or suggest the invention of Claim 15 and does not provide the attendant advantages. *See* section A.2 above.

Rao is no more pertinent to Claim 15 than Pinkham. Rao's "serial read operation starts with an address on inputs 15" (col. 4, lines 12-13). Then sense amplifiers 11 (Fig. 1) are actuated to move bits from a selected row into a shift register (col. 4, lines 16 and 19-21). Rao, alone or with Pinkham, does not teach or suggest that one of his sense amplifiers 11 is actuated and another sense amplifier is not actuated but becomes actuated subsequently in the same serial read operation in response to the same address on inputs 15, as recited in Claim 15. Claim 15 is therefore believed to be allowable.

Claim 17 dependent from Claim 16 is separately patentable for similar reasons. Note the last paragraph of Claim 17.

B.4. Claims 23, 24 and 26 (Group XII)

Claim 23 is separately patentable over Pinkham and Rao, taken singly or together, because Claim 23 recites: (1) a plurality of subarrays each of which comprises groups of columns; (2) a Y-decoder for each subarray; and (3) a Y-select circuit for each subarray, the Y-select circuit being responsive to the Y-decoder of the subarray to select all the columns that occupy a selected position in the groups of the subarray.

Claim 23 is supported by Figs. 3A, 3B as described above in SUMMARY OF THE INVENTION §5.

Rao does not teach or suggest a Y decoder for each of plural subarrays as recited in Claim 23. Indeed, Rao's memory of Fig. 1 has only one Y decoder 16 associated with Rao's array 10a (col. 3, lines 44-45). Rao does not teach or suggest a Y decoder for his other arrays 10b-10d. On the contrary, as Rao explains in col. 7, lines 1-2, "arrays 10b-10d are constructed

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for only serial access", and Rao's serial access does not require a Y-decoder. For example, Rao's serial read access involves transferring memory bits "from the selected row" into a shift register, and then moving the bits out in "serial format". Rao, col. 4, lines 20 and 23. No Y-decoder is required.

Moreover, Rao's Y decoder 16 selects only one column in array 10a (Rao, col. 3, line 46) and not all the columns in a selected position as recited in Claim 23. Thus, Rao does not teach or suggest Applicants' invention.

Pinkham also does not teach or suggest Applicants' separate Y-decoders for each subarray. Indeed, Pinkham provides only one column decoder for his arrays of Fig. 1:

> Although the ... column decoders are shown separate, each of the arrays 10-16 shares ... a common column decoder . . . .

Pinkham, col. 4, lines 45-48.

Moreover, Pinkham teaches away from separate column decoders by teaching that separate column decoders "would significantly increase the circuit density on a . . . chip." Pinkham, col. 6, lines 56-57. Thus, "instead of suggesting" Applicants' separate Y-decoders, Pinkham "deliberately seeks to avoid them; it warns against rather than teaches [Applicants'] invention." *In re Fine*, 5 USPQ2d 1596, 1599 (Fed. Cir. 1988). It is "error to find obviousness where references 'diverge from and teach away from the invention at hand'". *Id.* Claim 23 and its dependent Claims 24-26 are therefore believed to be allowable.

B.5. Claim 25 (Group XIII)

Claim 25 dependent from Claim 23 is separately patentable because Claim 25 recites a burst mode read operation in which "while data from the sense amplifier circuits of one of the subarrays are provided to the memory output, the sense amplifier circuits of another one of the subarrays develop

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output signals corresponding to data in said other one of the subarrays". This feature is separately patentable for reasons similar to the reasons discussed above in section B.2 in connection with Claim 16.

Claim 25 is separately patentable from Claim 16 because Claim 25 combines its feature with elements of Claim 23 which are not recited in Claim 16.

C. CONCLUSION

In view of the above, Claims 2-26 are believed to be allowable. Reversal of the Examiner's rejections and passage of this case to issue are respectfully requested.

Respectfully submitted,

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