Goodard v. Google, Inc.
Doc. 128 Att. 9

Exhibit J

Exhibit to the Declaration of Aaron R. Fahrenkrog in Support of Plaintiffs' Opening Claim Construction Brief

Dockets.Justia.com

#18 2312 PATENT

MAIL ROOM
MAR 24 1994
PAT. & TRADEMARK OFF.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Pearl Po-Yee Cheng et al.

Assignee: Advanced Micro Devices, Inc.

Title: "MEMORIES WITH BURST MODE ACCESS"

Serial No.: 07/836,667 Filing Date: 02/14/92

Examiner: S. Nadig Group Art Unit: 2312

Attorney Docket No.: M-2013 US

San Jose, California
March 21, 1994

COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D. C. 20231

RECEIVED
APR 12 1994
GROUP 2300

AMENDMENT

Sir:

In response to the Office Action dated October 19, 1993, please amend the above-identified application as follows.

IN THE TITLE

Please amend the title to read: --MEMORIES HAVING A BURST MODE SEQUENTIAL ACCESS--.

IN THE SPECIFICATION

Page 4, lines 15-16, delete "Figs. 3-28 illustrate memories according to the present invention." and substitute the following text:

--Figs. 3A, 3B diagram a memory according to the present invention.

Fig. 4 is a timing diagram for the memory of Figs. 3A, 3B.

Fig. 5 is a circuit diagram of memory cells of a memory according to the present invention.

Fig. 6 shows a timing scheme for the memory of Figs. 3A, 3B.

Fig. 7 is a block diagram of a memory according to the present invention.

Figs. 8A, 8B diagram a memory according to the present

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 283-1222
FAX (408) 283-1233

MAIL ROOM
MAR
24
1994
PAT. & TRADEMARK OFF.

invention.

Fig. 9 is a table illustrating the position and the logical numbering of the columns in the memory of Figs. 8A, 8B.

Fig. 10 is a timing diagram for the memory of Figs. 8A, 8B.

Fig. 11 diagrams a circuit that generates signals for the memory of Figs. 8A, 8B.

Fig. 12 diagrams a circuit that generates a signal for the circuit of Fig. 11.

Figs. 13A, 13B diagram a Y-register of the memory of Figs. 8A, 8B.

Fig. 14 illustrates portions of the Y-register of Figs. 13A, 13B.

Figs. 15A, 15B diagram a Y-register of the memory of Figs. 8A, 8B.

Fig. 16 diagrams an X-register of the memory of Figs. 8A, 8B.

Fig. 17A, 17B diagram a portion of the X-register of Fig. 16.

Figs. 18A, 18B diagram a portion of the X-register of Fig. 16.

Fig. 19 diagrams a circuit generating a signal for the X-register of Fig. 16.

Fig. 20 diagrams a circuit generating a signal for the X-register of Fig. 16.

Fig. 21 diagrams an X-register of the memory of Figs. 8A, 8B.

Figs. 22A, 22B diagram a portion of the X-register of Fig. 21.

Figs. 23A, 23B diagram a portion of the X-register of Fig. 21.

Fig. 24 diagrams a circuit generating a signal for the X-register of Fig. 21.

Figs. 25A, 25B diagram a control circuit of the memory of

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 283-1222
FAX (408) 283-1235

Figs. 8A, 8B.

Fig. 26 illustrates portions of the control circuit of Figs. 25A, 25B.

Fig. 27 diagrams a portion of the circuit of Figs. 25A, 25B.

Fig. 28 illustrates a control circuit of the memory of Figs. 8A, 8B.--

Page 16, line 13, replace "ATL3-ATL6" by --AQL3-AQL6--.

IN THE CLAIMS

Please amend the claims as follows.

2. (Amended) A memory comprising:

a plurality of rows of memory locations;

[one or more sense amplifiers for amplifying contents of said memory locations;]

a plurality of [row decoders] first registers, each [row decoder] first register for receiving a row address [and];

a plurality of row decoders, each row decoder for activating a portion of a row [which row is] identified by [said address] signals from one of said first registers; [and]

one or more sense amplifiers for amplifying contents of said memory locations in the row portions; and

an output for providing output signals from said sense amplifiers,

wherein at least two locations L1 and L2 in different rows of said memory can be read out to said output in burst mode such that the memory receives an address of one of said locations and provides in response contents of a plurality of memory locations, including the locations L1 and L2, in the sequence of consecutive addresses, so that while one of said row decoders is activating a row portion comprising said location L1 and [the] contents of said

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110

location L1 are being transferred from one or more of said sense amplifiers to said output, another one of said row decoders is activating a row portion comprising said location L2 and [the] contents of said location L2 are being transferred from said location L2 to one or more of said sense amplifiers.

3. (Amended) The memory of Claim 1 [having a burst mode in which the memory receives an address and provides in response to the address, in sequence, the contents of a plurality of memory locations], said memory [also] having a random mode in which the memory receives an address and provides in response the contents of a unique memory location,

wherein, both in burst mode and in random mode, while the contents of said location L1 are being transferred from one or more of said sense amplifiers to said output, the contents of said location L2 are being transferred from said location L2 to one or more of said sense amplifiers.

4. (Amended) The memory of Claim 1 wherein:

said memory [set of locations] comprises k [subsets] pluralities S-1, ..., S-k of locations wherein k is [an integer] a number of said pluralities and is greater than or equal to two;

for each [subset] plurality S-i, said sense amplifiers can receive simultaneously the contents of a number m of locations from said [subset] plurality S-i, wherein m is a positive integer; and

time tARA does not exceed m * (k-1) * (tOE), wherein:

tARA is measured from the time that an address of a location is made available to said memory to the time when one or more of said sense amplifiers develop an output signal indicative of the contents

LAW OFFICES OF
BEJEREVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE

of said location; and

tOE is the time to transfer an output of any one of said sense amplifiers to said output of said memory.

6. (Amended) The memory of Claim 1 [having a burst mode operation in which the memory receives an address of said location L1 and provides in response to the address, in sequence, the contents of consecutively addressed memory locations from L1 through at least L2,]

wherein, in [said] burst mode [operation], a time in which each location of said plurality except [L1] said one of said locations is read out to said output after a previous location has been read out to said output is shorter than a time in which said [location L1] one of said locations is read out to said output after said address of said [location L1] one of said locations has been received by said memory.

7. (Amended) A memory comprising:

a set of consecutively addressed memory locations L1, ..., Ln;

sense amplifier means for amplifying contents of said memory locations; and

an output for providing output signals from said sense amplifier means,

wherein said memory has a burst mode [an] operation for receiving an address and reading out to said output, in response to said address, any given number of memory locations in the sequence of consecutive addresses with wrap around so that the next location, if any, to be read out after said location Ln is said location L1, such that during said operation while the contents of any location L to be read out other than the last location to be read out

are being transferred from said sense amplifier means to said output, the contents of another location to be read out after said location L are being provided to said sense amplifier means for amplification and subsequent transfer to said output.

14. (Amended) In a memory having a plurality of rows of memory locations and having a plurality of row decoders and one X-register for each said row decoder, a method of reading in a burst mode operation a plurality of consecutively addressed memory locations spanning more than one row, said method comprising[, for each location of said plurality,] the steps of:

providing [an address of said location] to [one of] said [row decoders] X-registers a row address of a first location to be read in said burst mode operation;

for each row containing a location to be read in said burst mode operation, performing the steps of:

providing by at least one of the X-registers to at least one of the row decoders signals identifying said row;

activating by [said one of said row decoders a row portion which comprises said location] one of said row decoders at least a portion of said row;

sensing and amplifying contents of [said] at least one location of said row; and

transferring amplified contents of [said] at least one location of said row to an output of said memory;

wherein for at least two locations L1 and L2 of said plurality which are in different rows of said memory, the step of sensing and amplifying the contents of said location L2 overlaps in time with the step of transferring the amplified contents of said location L1 to said output of said memory.

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE
SUITE 700

~~15.~~ 16 (Amended) The method of Claim ~~14~~ 15 wherein:

said memory comprises a plurality of sense amplifier circuits, and each sensing and amplifying step is performed by at least one of said sense amplifier circuits; and

for at least two locations LL1 and LL2 of said plurality, during the step of transferring the amplified contents of said location LL1 to said output the sense amplifier circuit for sensing and amplifying the contents of said location LL1 is enabled and the sense amplifier circuit for sensing and amplifying the contents of said location LL2 is disabled, but said sense amplifier circuit for sensing and amplifying the contents of said location LL2 is enabled subsequently during the step of sensing and amplifying the contents of said location LL2.

~~16.~~ 19 (Amended) In a memory comprising a set of consecutively addressed memory locations L1, ..., Ln, a method of reading out in burst mode a sequence of locations addressed consecutively with wrap around so that the next location to be read out after location Ln is location L1, said method comprising the steps of:

receiving an address of a first location to be read out in burst mode; and

in response to said address, for each location of said sequence[,] performing the steps of:

sensing and amplifying contents of said location; and

transferring amplified contents of said location to an output of said memory,

wherein for any location L of said sequence other than the last location to be read out in said sequence, the transferring step for the location L overlaps in time with the sensing and amplifying step for another location to be read out after said

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110

location L in said sequence.

Please add the following claims.

16. The memory of Claim 1 wherein said memory is fabricated in an integrated circuit.

17. The memory of Claim 1 further comprising:

a plurality of second registers, each second register for receiving at least a portion of a column address; and

a circuitry for each second register for selecting in response to signals from one of the second registers a plurality of columns to be read by the sense amplifiers.

18. The memory of Claim 8 wherein said memory is fabricated in an integrated circuit.

19. The method of Claim 15, further comprising the steps of:

providing at least a portion of a column address of the first location to be read in said operation to at least one of Y-registers of said memory; and

providing, by at least one of the Y registers, signals identifying a plurality of columns of the memory such that memory locations in said plurality of columns in one row have consecutive addresses,

wherein the sensing and amplifying step comprises the step of sensing and amplifying contents of memory locations in said plurality of columns.

20. The method of Claim 17 wherein the transferring step comprises the step of transferring the amplified contents to the output consecutively in the sequence of addresses.

LAW OFFICES OF
BEJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE
SUITE 700

~~23~~. 20 An integrated memory comprising:

an array of memory locations, the array comprising a plurality of subarrays, each subarray comprising a predetermined number of groups of columns of the memory locations such that for any given column position in a group, the memory locations in any given row in the columns at said given position in the groups of the subarray have consecutive addresses;

one X-decoder for each subarray;

one X-register for each X-decoder;

one Y-decoder for each subarray;

one Y-register for each Y-decoder;

one Y-select circuit for each subarray, the Y-select circuit being responsive to the Y-decoder of the subarray to select all the columns that occupy a selected position in the groups of the subarray;

a plurality of sense amplifier circuits for each subarray, each sense amplifier circuit for amplifying signals from a column selected by the Y-select circuit of the subarray;

a memory output; and

a control circuit for selecting one of the sense amplifier circuits to provide data to the memory output,

wherein in a burst mode read operation, at least one X-register provides to its respective X-decoder signals identifying a row in one of the subarrays, and at least one Y-register provides to its respective Y-decoder signals identifying a position of columns in the groups of one of the subarrays.

~~24~~. 21 The memory of Claim ~~23~~ 20 wherein said subarrays are two in number.

~~25~~. 22 The memory of Claim ~~23~~ 20 wherein in the burst mode read

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 283-1222
FAX (408) 283-1233

operation while data from the sense amplifier circuits of one of the subarrays are provided to the memory output, the sense amplifier circuits of another one of the subarrays develop output signals corresponding to data in said other one of the subarrays.

23. The memory of Claim 20 wherein in the burst mode read operation, the control circuit enables the sense amplifier circuit selected to provide data to the memory output and at the same time disables one or more sense amplifier circuits not selected to provide data to the memory output.

IN THE ABSTRACT

Please amend the abstract to read as follows.

--To provide a boundaryless burst mode access, a memory array is divided into two or more subarrays. Each subarray has its own row and column decoders. The columns of each subarray are divided into groups. A sense amplifier circuit is provided for each group of columns. The column decoder of each subarray selects simultaneously one column from each group so that the memory locations in one row in the selected columns have consecutive addresses. The memory locations in the selected row and columns are read by the sense amplifier circuits. While the contents of the sense amplifier circuits of one subarray are transferred one by one to the memory output, consecutive memory locations of another subarray are read to the sense amplifier circuits. In some embodiments, to save power, sense amplifier circuits are disabled when their outputs are not transferred to the memory output.--

REMARKS

Claims 2-17 are pending in the application and are rejected. Claims 2, 3, 5-7, and 14-16 are amended and Claims 18-26 are added. Reconsideration and withdrawal of the

rejections and objections is respectfully requested.

The title of the invention is objected to as not descriptive. A more descriptive title is provided.

Figs. 3B, 6, 7, 19, 24, 25A, 25B, 27 and 28 are objected to. A proposed amendment to drawings is filed herewith to overcome the objection to Figs. 3B, 6, 7, 19, 24, 27 and 28.

Regarding Figs. 25A, 25B, the Examiner states that reference numbers for boxed information are necessary. However, reference numbers SHL-0 through SHL-3, SHR-0 through SHR-3, and 25 are already provided for the boxed information.

The Brief Description of the Drawings is amended as required by the Examiner.

The Abstract of the Disclosure is objected to. The Abstract is amended to overcome the objection.

Claims 2-17 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. This rejection is respectfully traversed.

Regarding Claim 2, the Examiner states:

> "receiving row address" -- lack of antecedent basis; also, how will the row decoder receive addresses?

Claim 2 recites not "receiving row address" but "receiving a row address" (emphasis added). Thus, a separate antecedent basis is not required.

Claim 2 is amended not to recite a row decoder for receiving addresses.

Further regarding Claim 2, the Examiner states:

> "for activating a portion ..." -- what is the method or means of activation?

Claim 2 need not be limited by any particular method or means of activation. MPEP § 703.03(d) states:

> The fact that a claim is broad does not necessarily justify a rejection on the ground that the claim as vague and indefinite ... .

Further regarding Claim 2, the Examiner states:

> "the contents" -- lack of antecedent basis.

LAW OFFICES OF
BEJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 283-1222
FAX (408) 283-1233

Claim 2 is amended to provide antecedent basis.

The rejection of Claims 3 and 4 on the grounds of a lack of antecedent basis is overcome by the amendment to Claim 2. Of note, Claims 3 and 4 depend from Claim 2.

Regarding Claim 5, the Examiner states:

> "said set of locations" -- what locations are being referred to here? What is the subset of?

The terms "set" and "subsets" are deleted from Claim 5.

Further regarding Claim 5, the Examiner states:

> "k ... S-1 ... S-i ... m ..." -- all symbols and letters must be defined as to their usage and purpose ... .

All the symbols and letters are defined in Claim 5. In particular, each of symbols S-1, ..., S-k is defined as denoting a plurality of memory locations. (Pluralities S-1, ..., S-k read on respective subarrays 314.1, ... 314.k of Fig. 7 and on subarrays 314.L, 314.R of Figs. 3 and 8A, 8B.) "k" is defined as a number of the pluralities S-1, ..., S-k (k=2 in Figs. 3 and 8A, 8B). S-i denotes generically one of the pluralities S-1 through S-k. "m" is defined as a number of locations of the plurality S-i such that the contents of m locations can be received simultaneously by the sense amplifiers. (For example, in the embodiment of Fig. 3, m=1, 2, 3 or 4; see the specification, page 9, line 30.). Such use of symbols and letters is permissible in the claims as illustrated, for example, by U.S. patent No. 5,280,594, Claim 5, col. 6, lines 39-44. Claim 5 of U.S. patent No. 5,280,594 is attached hereto as Exhibit A.

Further regarding Applicants' Claim 5, the Examiner asks:

> what is the relationship between m and the subsets?

The relationship is that the contents of m locations in the plurality S-i can be received simultaneously by the sense amplifiers.

Further regarding Claim 5, the Examiner states:

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 283-1222
FAX (408) 283-1233

> "time tARA ... tOE" --abbreviations must be expanded when first introduced.

"tARA" and "tOE" are not abbreviations but symbols denoting certain lengths of time as defined in the last two paragraphs of Claim 5. For an example of such symbols, see U.S. Patent No. 5,280,594, Claim 5, col. 6, line 40 (Exhibit A attached hereto).

Claims 10 and 13 are rejected for the same reasons as Claim 5. The term "set of locations" in Claims 10 and 13 is defined in Claim 7 from which Claims 10 and 13 depend. (The "set of locations" reads on locations M-0 through M-31 in Figs 3A, 3B.) The "subsets" of Claim 10 are subsets of the set of Claim 7. (Each subset reads on subarray 314.L or 314.R in Figs. 3A, 3B.)

The remaining rejections of Claims 10 and 13 under 35 U.S.C. § 112 are traversed for reasons similar to the reasons discussed above in connection with Claim 5.

The rejection of Claim 6 on the ground of a lack of antecedent basis is overcome by the present amendment to Claim 6.

In paragraph 6 of the Office Action the Examiner states:

> no correspondence between claim language and drawings is found; specifically, L1 and L2 in claims 2, 6, 7, 14 & 16 and LL1 and LL2 in claims 15 & 17.

Locations L1 and L2 in Claims 2 and 14 correspond, for example, to locations M-15 and M-16 in Figs. 3A, 3B. "L1" and "L2" are deleted from Claim 6.

Locations L1, ..., Ln in Claims 7 and 16 correspond, for example, to locations M-0, ..., M-31 in Figs. 3A, 3B.

Locations LL1, LL2 in Claim 15 correspond, for example, to locations M-0, M-4 in Figs. 3A, 3B. See Applicants' specification, page 8, lines 33-35. Location LL in Claim 17 corresponds, for example, to location M-1 in Figs. 3A, 3B. Specification, page 8, lines 33-35.

The Examiner states also in paragraph 6 of the Office

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 283-1222
FAX (408) 283-1233

Action:

> uncertainty as to whether both row decoders are being activated simultaneously by the same signal or source or whether they are activated separately arises within the examiner.

The Examiner does not specify whether this statement refers to any particular claims or to any embodiments described in the specification.

Claim 2 recites row decoders but does not state that row decoders are activated.

In the embodiment of Figs. 3A, 3B, X-decoders 316.L, 316.R are responsive to respective X-registers 340.L, 340.R.

Claims 2-17 are rejected under 35 U.S.C. § 102(e) over Kobayashi et al. This rejection is respectfully traversed.

Claim 2 distinguishes from Kobayashi et al. by reciting a memory having a burst mode in which mode the memory receives an address of one memory location "and provides in response contents of a plurality of memory locations ... in the sequence of consecutive addresses".

Claim 2 is supported by Applicants' Figs. 3 and 8. In the embodiments of Figs. 3 and 8, the burst mode provides a fast sequential memory access because contents of several locations are provided in response to one address. Specification, page 2, lines 27-28.

Kobayashi et al. disclose in Fig. 4 a memory that receives address signals A and B from different external interfaces. See Kobayashi et al., column 4, lines 63-65 and column 5, lines 8-10. Kobayashi et al. do not teach or suggest that their memory provides contents of a plurality of locations in response to address signal A, or that their memory provides contents of a plurality of locations in response to address signal B, as recited in Claim 2. Hence Kobayashi et al. do not teach or suggest a burst mode as in Claim 2. Claim 2 and Claims 3-6, 18 and 19 dependent therefrom are therefore believed to be allowable.

LAW OFFICES OF
BEJEREVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 285-1222
FAX (408) 285-1235

Claim 4 dependent from Claim 2 further distinguishes from Kobayashi et al. by reciting a memory in which some sense amplifiers are enabled while other sense amplifiers are disabled.

Claim 4 is supported by the specification, page 8, line 23 through page 9, line 11. Disabling some sense amplifiers "provides significant power saving" in some embodiments. Specification, page 9, line 8.

Kobayashi et al. disclose in Fig. 4 two sense amplifiers 5A for two corresponding memory blocks 31, 32. See Kobayashi et al., column 5, lines 26-28. Kobayashi et al. do not teach or suggest disabling one of their sense amplifiers while enabling the other amplifier as recited in Claim 4. Claim 4 is believed to be allowable for this additional reason.

Claim 5 dependent from Claim 2 further distinguishes from Kobayashi et al. by reciting the relationship that the time tARA does not exceed m * (k-1) * (tOE), wherein tARA, m, k, and tOE are parameters defined in Claim 5.

Claim 5 is supported by Applicants' Figs. 6 and 7 and the specification, page 10, lines 13-19 and page 11, line 8. In the embodiment of Fig. 7, the relationship between tARA, m, k and tOE allows reading in burst mode each datum starting from the second datum in the time tOE that it takes to transfer a sense amplifier output to the output of the memory rather than in a longer time that includes address decoding. See the specification, page 11, lines 6-7.

Kobayashi et al. do not teach or suggest the relationship recited in Claim 5. Claim 5 is believed to be allowable for this additional reason.

Claim 7, reciting a burst mode, and Claims 8-13 and 20 dependent therefrom are believed to be allowable for reasons similar to the reasons discussed above in connection with Claim 2.

In addition, Claim 8 and Claim 9 dependent therefrom are

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 283-1222
FAX (408) 283-1233

believed to be allowable for reasons similar to the reasons discussed above in connection with Claim 4.

Further, Claim 10 is believed to be allowable for reasons similar to the reasons discussed above in connection with Claim 5.

Claim 14 and Claims 15, 21 and 22 dependent therefrom are believed to be allowable for reasons similar to the reasons discussed above in connection with Claim 2.

Further, Claim 15 is believed to be allowable for reasons similar to the reasons discussed above in connection with Claim 4.

Claim 16 and Claim 17 dependent therefrom are believed to be allowable for reasons similar to the reasons discussed above in connection with Claim 2.

In addition, Claim 17 is believed to be allowable for reasons similar to the reasons discussed above in connection with Claim 4.

Claim 23 and Claims 24-26 dependent therefrom are believed to be allowable for reasons similar to the reasons discussed above in connection with Claim 2.

Further, Claim 26 is believed to be allowable for reasons similar to the reasons discussed above in connection with Claim 4.

On April 17, 1992, Applicants filed an Information Disclosure Statement listing, among other things, U.S. patent applications 07/558,033 and 07/557,899. Per the Office Action, paragraph 16, the Examiner did not consider these patent applications apparently on the grounds that the patent applications were not referenced in Applicants' "Background of the Invention". However, 37 C.F.R. §§ 1.56, 1.97 and 1.98 that govern filing of information disclosure statements do not require that patent applications cited in such statements be referenced in the Background of the Invention. Therefore, Applicants respectfully request consideration of patent

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 285-1222

applications 07/558,033 and 07/557,899.

In summary, Claims 2-17 were pending in the present application and were rejected. Claims 2, 3, 5-7 and 14-16 are amended and Claims 18-26 are added. Claims 2-26 are believed to be allowable, and early passage of this case to issue is respectfully requested. If any matters remain outstanding after consideration of this amendment, the Examiner is requested to telephone the undersigned at the number below to expedite prosecution of this case.

Respectfully submitted,

Michael Shenker

Michael Shenker
Attorney for Applicants
Reg. No. 34,250
Telephone: (408) 283-1222

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C., 20231, on March 21, 1994.

March 21, 1994 Michael Shenker
Date of Signature Attorney for Applicants

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE
SUITE 700