

# EXHIBIT C



**UNITED STATES DEPARTMENT OF COMMERCE  
Patent and Trademark Office**

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SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/179,926	01/11/94	BLOMGREN	J RM1
			EXAMINER VU, V
		B3M1/0627	ART UNIT PAPER NUMBER
			2315 4
			DATE MAILED: 06/27/94

This is a communication from the examiner in charge of your application.  
COMMISSIONER OF PATENTS AND TRADEMARKS

This application has been examined  Responsive to communication filed on 5-9-94  This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), 0 days from the date of this letter.  
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

**Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:**

- Notice of References Cited by Examiner, PTO-892.
- Notice of Draftsman's Patent Drawing Review, PTO-948.
- Notice of Art Cited by Applicant, PTO-1449.
- Notice of Informal Patent Application, PTO-152.
- Information on How to Effect Drawing Changes, PTO-1474.
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**Part II SUMMARY OF ACTION**

- Claims 1-20 are pending in the application.  
Of the above, claims \_\_\_\_\_ are withdrawn from consideration.
- Claims \_\_\_\_\_ have been cancelled.
- Claims \_\_\_\_\_ are allowed.
- Claims 1-20 are rejected.
- Claims \_\_\_\_\_ are objected to.
- Claims \_\_\_\_\_ are subject to restriction or election requirement.
- This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
- Formal drawings are required in response to this Office action.
- The corrected or substitute drawings have been received on \_\_\_\_\_. Under 37 C.F.R. 1.84 these drawings are  acceptable;  not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).
- The proposed additional or substitute sheet(s) of drawings, filed on \_\_\_\_\_, has (have) been  approved by the examiner;  disapproved by the examiner (see explanation).
- The proposed drawing correction, filed \_\_\_\_\_, has been  approved;  disapproved (see explanation).
- Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has  been received  not been received  been filed in parent application, serial no. \_\_\_\_\_; filed on \_\_\_\_\_.
- Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
- Other

**EXAMINER'S ACTION**

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**PART III: DETAIL OF ACTION**

1. The applicants are reminded to indicate all related co-pending applications in the cross-references to related applications section of the specification. It appears in the PTO-1449 cited by the applicants and received at the office on May 9, 1994 that a related co-pending application serial no. 08/180,023 was not indicated earlier in this application.

2. Claims 2-13 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The following language lacks of proper antecedent basis:

In claim 2, line 5, "the next instruction". It is not clear what particular next instruction the claim refers to.

In claim 3, line 2, "the instruction". It is not clear what particular instruction the claim refers to.

In claim 6, line 3, "the execution unit".

Other dependent claims not specifically cited above are also rejected because of the deficiency of their respective parent claims.

The examiner further suggests the applicants to include line numbers for each claim instead of for the whole page because errors

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and corrections can be located much easier especially in the long claims.

The examiner further suggests changing "the" to --said-- whenever possible for more clearly identifying the referenced object elements in the claims. For example: in claim 1, line 2, "the CPU", line 4, "the first", line 6, "the second", "the first", line 7, "the second", line 8, "the first", "the second", line 9, "the decoded", "the first", line 10, "the second", line 11, "the select", line 12, "the first", "the second", line 13, "the CPU".

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4 are rejected under 35 U.S.C. § 102(b) as being clearly anticipated by Ueda et al (hereafter Ueda), U.S. pat. no. 4,821,187.

5. Ueda teaches the claimed invention, a system capable of executing two different instruction sets (see abstract). In particular, the system comprises two separate decoders for decoding first and second set of instructions respectively,

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execution units for executing the decoded first and second instructions, control units for controlling switching execution of first and second instruction sets (see summary).

6. The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 C.F.R. § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 U.S.C. § 102(f) or (g) prior art under 35 U.S.C. § 103.

8. Claims 1-20 are rejected under 35 U.S.C. § 103 as being unpatentable over de Nicolas et al (hereafter Nicolas), U.S. pat. no. 5,167,023.

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9. As to claims 1-4, Nicolas teaches a system substantially as claimed for emulating the execution of second set of instructions (target instructions) which are not directly executable by the host system (see abstract). In particular, the system is capable of directly executing native RISC instructions in a normal mode and executing CISC target instructions in an emulation mode. Nicolas describes a number of prior art systems, one of which was implemented the instruction execution emulation with hardware (see background). It would have been obvious to one of ordinary skill in the art at the time of the invention that such hardware emulation would have included a second decoder for decoding target instructions, and other control units for controlling the emulation mode for executing target instructions.

10. As to claims 5-10, Nicolas particularly teaches emulating the execution of CISC instructions using software where each CISC instruction execution is emulated by executing a routine comprising a plurality of individual RISC instructions, and where the emulation mode is initiated by an interrupt signal (see background). Nicolas further teaches using a translation look-aside buffer (TLB) for providing dynamic address conversion for executed instructions (see summary). It is noted that the TLB would be utilized in executing native RISC instruction in both normal and emulation modes. Nicolas does not particularly teach

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incorporating both hardware and software emulation in the same machine as claimed. It would have been obvious to one of ordinary skill in the art at the time of the invention to realize such software and hardware combination because it would bring the advantages of both techniques into the system, e.g. the inexpensive and flexibility of the software emulation and the speed of the hardware emulation.

11. As to claim 11, it would have been obvious to one skilled in the art to modify the TLB when additional instructions are added to the emulation instruction sets so that the TLB could operate properly.

12. As to claims 12-13, it would have been obvious to one skilled in the art to switch from the normal mode to the emulation mode in response to signal from the host execution unit or from a reset signal.

13. Claims 14-20 are rejected for the same rationales set forth above for claims 1-13.

14. All pending claims are rejected in this office action.

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15. The following references are cited by the examiner as of general interest.

- a. Wilburn et al, U.S. pat. no. 4,633,417: emulator for non-fixed instruction set VLSI devices.
- b. Kashiwagi, U.S. pat. no. 4,780,819: emulator system utilizing a program counter and a latch coupled to an emulator memory for reducing fetch time of instructions stored in the emulation memory.
- c. Simpson, U.S. pat. no. 4,794,522: method for detecting modified object code in an emulator.
- d. Adachi, U.S. pat. no. 4,812,975: emulation method.
- e. Mitchell et al, U.S. pat. no. 4,841,476: extended floating point operations supporting emulation of source instruction execution.
- f. Nakayama, U.S. pat. no. 4,942,519: coprocessor capable of checking address mapping.
- g. Cooper et al, U.S. pat. no. 5,077,657: emulator assist unit which forms addresses of user instruction operands in response to emulator assist unit commands from host processor.
- h. Bresford et al, U.S. pat. no. 5,230,069: apparatus and method for providing private and shared access to host address and data spaces by guest programs in a virtual machine computer system.
- i. Jen et al, U.S. pat. no. 5,291,586: hardware implementation of complex data transfer instruction.



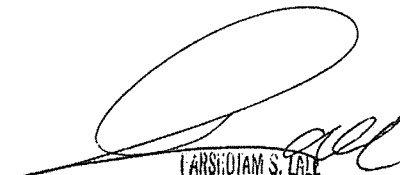
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16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to V. Vu whose telephone number is (703) 305-9597.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.



V. Vu  
Art Unit 2315  
6/15/94



IAN S. TALE  
SUPERVISORY PATENT EXAMINER  
ART UNIT 231

TO SEPARATE, HOLD TOP AND BOTTOM EDGES, SNAP-APART AND DISCARD CARBON

*AKH*

FORM PTO-892 (REV. 2-92)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		SERIAL NO. 08/179,926	GROUP ART UNIT 2315	ATTACHMENT TO PAPER NUMBER 4		
NOTICE OF REFERENCES CITED				APPLICANT(S) Blomgren				
U.S. PATENT DOCUMENTS								
	DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE		
A	4833417	12-30-86	Wilburn et al	364	550			
B	4780819	10-25-88	Kashinagi	395	500			
C	4794522	12-27-88	Simpson	395	500			
D	4812975	3-14-89	Adachi et al	395	500			
E	4821187	4-11-89	Ueda et al	395	<del>596</del> 375			
F	4841476	6-20-89	Mitchell et al	395	500			
G	4942519	7-17-90	Nakayama	395	<del>298</del> 375			
H	5077657	12-31-91	Cooper et al	395	500			
I	5167023	11-24-92	de Nicolas et al	395	<del>529</del> 375			
J	5230069	7-20-93	Brelsford et al	<del>345</del>	6400			
K	5291586	3-1-94	Jen et al	395	500			
FOREIGN PATENT DOCUMENTS								
	DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHTS. DWG. PP. SPEC.	
L								
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OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)								
R								
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U								
EXAMINER V. Vu				DATE 6-15-94				
* A copy of this reference is not being furnished with this office action. (See Manual of Patent Examining Procedure, section 707.05 (a).)								