EXHIBIT G

UNITED STATES DEPARTMENT OF COMMERCE
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SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/179,926	01/11/94	BLOMGREN	

EXAMINER	
VU, V	
ART UNIT	**PAPER NUMBER**
2315	8

E3M1/0405

STUART T. AUVINEN
429 26TH AVE.
SANTA CRUZ, CA 95062

DATE MAILED: 04/05/95 (KS)

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☐ This application has been examined ☒ Responsive to communication filed on 2-16-95 ☒ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), 0 days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☐ Notice of Draftsman's Patent Drawing Review, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____.

Part II SUMMARY OF ACTION

1. ☒ Claims 1-20 are pending in the application.
   Of the above, claims _____ are withdrawn from consideration.
2. ☐ Claims _____ have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☒ Claims 1-20 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____. has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed _____, has been ☐ approved; ☐ disapproved (see explanation).
12. ☐ Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____.
13. ☐ Since this application apppears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION

PTOL-326 (Rev. 2/93)

PART III: DETAIL OF ACTION

1. This office action responds to applicants' amendment filed on February 16, 1995. Claims 1-20 remain pending.

2. The text of 35 U.S.C. § 103 cited in the first office action is hereby incorporated by reference.

3. The rejection of claims 1-5, 14-16 and 18-20 under 35 U.S.C. § 103 as being unpatentable over Portanova et al (hereafter Portanova), U.S. pat. no. 4,992,934 in view of Onishi, U.S. pat. no. 3, 764,988 set forth in the previous office action mailed November 16, 1994 is hereby incorporated by reference.

4. The rejection of claims 6-13 and 17 under 35 U.S.C. § 103 as being unpatentable over Portanova and Onishi and further in view of Bullions, III et al (hereafter Bullions), U.S. pat. no. 4,456,954 set forth in the previous office action mailed November 16, 1994 is hereby incorporated by reference.

5. All pending claims are rejected in this office action. Applicants' arguments filed on February 16, 1995 have been fully considered but they are not deemed to be persuasive.

6. As to the remarks, applicants argue that the claimed invention is not obvious over the applied arts of record for the following reasons:

a) Portanova's disclosure is not enabling because Portanova teaches only software implementation to emulate CISC capability in a RISC-core processor and that Portanova fails to teach the detailed hardware implementation of CISC emulation.

b) Onishi's teaching is directed to a different problem.

c) there is no reason to combine Portanova and Onishi.

d) Bullions' teachings cannot be combined with other references to render the claimed invention obvious.

Regarding point a, it is submitted that applicants' argument that Portanova's disclosure is not enabling is without merit because the reference does not have to be enabling its entire contents in order for the reference to be used. Indeed, any piece of teaching or suggestion in the reference can be very well applied against the present claimed invention provided that such teaching or suggestion is within the level of ordinary skill in the art. Applicants are reminded that 35 U.S.C 112 first paragraph is to be applied to the claims and not to the reference. There is absolutely no precedent case law to support the allegation that the reference must meet 35 U.S.C 112 first paragraph to the extent as applicants asserted before it can be applied against the claims. Indeed, like the present application, the reference obligates to

provide enabling disclosure only to what being claimed, not to what not being claimed.

Returning to the Portanova reference, Portanova explicitly teaches an exemplary system that employs software implementation of CISC emulation in which each guest CISC instruction is emulated by a series of host RISC instructions. Portanova, however, clearly suggests that hardware implementation of CISC emulation could have been done as an alternative approach (see col 29, line 60 - col 30, line 12). The question now is whether or not such alternative approach can be done regarding the level of ordinary skill in the art. Portanova clearly shows different well-known approaches to implement the CISC (see figures 9-12). Applicants assert that such approaches are applied only to single instruction set, i.e. CISC, and not to processor supporting both RISC and CISC. This argument fails because Portanova suggests the implementation of CISC in the context of dual-instruction-set processor and not single-instruction-set processor, i.e., such approaches are suggested to implement the CISC part of the processor. Moreover, to the extent of employing hardware implementation to execute a sub-set of instructions, Onishi teaches a system that employs two instruction decoders, one for normal instructions and one for branch instructions. The use of two decoders as opposed to one decoder in a conventional processor allows the system to decode instructions more efficiently because decoding of a branch instruction usually

takes longer than that of a normal instruction. Tanenbaum further teaches that considering either hardware or software implementation is a matter of design choice since hardware and software implementations are indeed interchangeable. Further evidences of hardware implementation as opposed to software implementation can also be seen in two newly cited references, Lee et al and Agnew et al. Both references clearly teach that the execution of a sub-set of instructions can be implemented with either hardware or software (see abstracts in Lee et al and Agnew et al).

Thus, in light of level of ordinary skill in the art as evidenced by the above cited arts, it is again submitted that employing wholly or partly hardware implementation to execute the guest instructions (CISC) in Portanova could have been done and such hardware implementation approach would have been obvious to one skilled in the art at the time the invention was made. Here, although the detail of hardware implementation for executing CISC was not specified by either reference, to the extent of the scope of the claims to design a processor capable of executing dual instruction sets where a subset of second instruction set is implemented partly with hardware, the teachings and suggestions from the applied references sufficiently meet the claim limitations. It is further noted that although these teachings of the applied references may no longer be sufficient in considering further detail of the implementation of the CISC emulation in a

dual-instruction-set processor, applicants however have failed to point out the details in the claims that define the invention over the prior art.

Regarding point b, the examiner submits that applicants attempt to show non-obviousness by using piecemeal analysis of the references. Applicants are reminded that one cannot show non-obviousness by attacking references individually where, as here, the rejections are based on combinations of references.

Regarding point c, it is submitted that the combination of the reference is clearly motivated by the explicit suggestion from Portanova to implement CISC emulation wholly or partly with hardware (see Portanova, col 29, line 60 - col 30, line 12, figures 9-12).

Regarding point d, the examiner again submits that applicants attempt to show non-obviousness by applying piecemeal analysis of the references in which applicants construe each reference narrowly to a specific application. In contrary to applicants' assertion, it is submitted that Bullions' teaching of using a translation look-aside buffer to address emulated instructions is not to be applied exclusively to CISC type processor. It would have obvious that Bullions' teachings can also be applied to other processors including the dual-instruction-set processor taught by Portanova.

In summary, it is submitted that applicants' rationale of non-obviousness was made by improperly ignoring skill level in the art.

Applicants have made arguments of non-obviousness based solely on what was explicitly taught in the references and what was not explicitly taught in the references. In the contrary, it is submitted that the claimed invention was clearly rendered obvious by the teachings and suggestions of the applied art of record as set forth in the previous office action and the above discussion.

7. The following references are cited by the examiner as of general interest.

a. Agnew et al, U.S. pat. no. 4,514,803: methods for partitioning mainframe instruction sets to implement microprocessor based emulation thereof.

b. Lee et al, U.S. pat. no. 4,763,242: computer providing flexible processor extension, flexible instruction set extension and implicit emulation for upward software compatibility.

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR

RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to V. Vu whose telephone number is (703) 305-9597.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.

V. Vu
Art Unit 2315
3/31/95

WILLIAM S. LALL
SUPERVISORY PATENT EXAMINER
ART UNIT 231

TO SEPARATE, HOLD TOP AND BOTTOM EDGES, SNAP-APART AND DISCARD CARBON

FORM PTO-892 (REV. 2-92)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	SERIAL NO.	GROUP ART UNIT	ATTACHMENT TO PAPER NUMBER
NOTICE OF REFERENCES CITED		08/179,926	2315	8
		APPLICANT(S) Blomgren et al		

U.S. PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
	A	4514803	4-30-85	Agnew et al	395	500	
	B	4763242	8-9-88	Lee et al	395	500	
	C						
	D						
	E						
	F						
	G						
	H						
	I						
	J						
	K						

FOREIGN PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHTS. DWG.	PERTINENT PP. SPEC.
	L								
	M								
	N								
	O								
	P								
	Q								

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

R	
S	
T	
U	

EXAMINER	DATE
V. Vu	3-31-95

* A copy of this reference is not being furnished with this office action.
(See Manual of Patent Examining Procedure, section 707.05 (a).)