EXHIBIT H

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Stuart T. Auvinen, Reg. No. 36,435

Date 5/22/95

EXPEDITED PROCEDURE - AF
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	)	
	)	
Blomgren et al.	)	Examiner: V. Vu
	)	
Serial No. 08/179,926	)	Group Art Unit: 2315
	)	
Filed: 1/11/94	)	
	)	
For: Dual-Instruction-Set Architecture CPU with Hidden Software Emulation Mode	)	
	)	

AMENDMENT AFTER FINAL REJECTION UNDER 37 C.F.R. § 1.116

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Hon. Commissioner of Patents and Trademarks
Washington, DC 20231

Sir:

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In response to the third office action mailed 4/5/95, Applicant requests that this amendment be entered to place the application in a condition for allowance or a better form for appeal:

20 **In the claims:**

Please amend claim 18 as follows:

18. (three times amended) A microprocessor for executing instructions belonging to a

25 reduced instruction set computer (RISC) instruction set and for executing instructions

belonging to a complex instruction set computer (CISC) instruction set, said microprocessor comprising:

RISC instruction decode means, for decoding instructions belonging to said RISC instruction set;

CISC instruction decode means, for decoding only a subset of instructions belonging to said CISC instruction set;

mode register means for indicating a current operating mode of said microprocessor;

enable means, coupled to said RISC instruction decode means and said CISC instruction decode means, for enabling said decoding of instructions belonging to said RISC instruction set or belonging to said CISC instruction set, said enable means responsive to said current operating mode of said microprocessor; and

an execution unit, coupled to said [first] RISC instruction decode means and said [second] CISC instruction decode means, for executing instructions belonging to said [first] RISC instruction set and instructions belonging to said [second] CISC instruction set,

whereby instructions from said RISC instruction set and instructions from said CISC instruction set can be executed by said execution unit.

REMARKS

Under 35 USC § 103, claims 1-5, 14-16, and 18-20 were rejected as obvious over Portanova et al (US Pat. No. 4,992,934) in view of Onishi (U.S. Patent No. 3,764,988). Claims 6-13 and 17 were rejected under 35 USC § 103 as obvious over Portanova in view of Onishi as set forth for claims 1-5, and further in view of Bullions, III, et al (U.S. Patent No. 4,456,954). All claims were thus rejected.

Claim 18 has been amended to remove an antecedent problem found by Applicant.

New Prior Art Cited

Two new references have been cited in the final action. These references were used as showing the *background level of skill in the art*. The Examiner has not raised the issue of the background skill level until the final action. Thus the background skill level is a new issue for the final rejection. Applicant believes that these new references are improperly being introduced at the final rejection under the new argument of "background skill level" since the primary references clearly do not teach hardware execution of two instruction sets, or part of a second instruction set.

Applicant requests that the final action be withdrawn as being premature due to the introduction of two new references and the introduction of the new issue of background skill level.

Explicit Teaching and Suggestion Lacking from Portanova

The references clearly do not teach hardware execution of two different instruction sets. The Examiner agrees that hardware execution of two instruction sets is not explicitly taught (page 7, first paragraph of action) but is suggested. However, Applicant is unable to find any language in the cited page (col 29 - col 30) of the reference containing this suggestion. In the prior amendment, Applicant discussed each of "prior-art" Figures 9, 10, 11, and 12 in the cited page, and was not able to find any such suggestion or teaching that a hardware pipeline could execute two native instruction sets. Instead these prior-art figures show how Portanova's RISC processor can be used to emulate in software a CISC instruction set for several well-known CISC architectures, such as 68000, VAX, S/370.

Portanova Teaches Away - Design RISC 1st, then code CISC

Portanova clearly teaches away from hardware execution of both RISC and CISC when he teaches a two-step process:

1.) The RISC hardware is first built without regard for CISC.

2.) Then the software emulator is written for any of the CISC architectures of Figures 9-12 (col 30, lines 39-64).

Hardware execution would REQUIRE that CISC be considered when the hardware is designed. Designing CISC hardware with RISC hardware would slow down the design process, and nullify Portanova's advantage stated at col 30.

Request for Identification of Basis for Suggestion

If such language suggesting *hardware* execution of *two* instruction sets exist, Applicant requests that Examiner explicitly point out what figure and what line it occurs in, rather than broadly referring to a page with four prior-art figures. This will help define the issues for appeal and ensure that Applicant and Examiner are not "discussing two completely different cases" (PTO Day 1994, pages 357-9). Something in the Prior art must suggest the desirability of making the combination (*Uniroyal, Inc. v. Rudkin-Wiley Corp.*, 837 F.2d at 1050-51, 5 USPQ2d at 1438). The claimed invention must not be used as a blueprint.

Piecemeal Attack of References Proper

Examiner objected to Applicant's thorough and specific analysis of the references, stating that "Applicants attempt to show non-obviousness by piecemeal analysis of the references. Applicants are reminded that one cannot show non-obviousness by attacking references individually where, as here, the rejections are based on combinations of references." (page 6).

Applicant strongly disagrees. When the Examiner cites a portion of a reference as teaching a claim element, the Applicant can show that such reliance is in error. For example, if an Examiner states that reference P teaches X while reference Q teaches Y, then Applicant can properly argue that reference P does not, in fact, teach X.

In the present case, Examiner has relied on Portanova for a suggestion of hardware execution of two instruction sets. Examiner states that "Portanova, however, clearly suggests that hardware implementation of CISC emulation could have been done as an alternative approach (see col 29, line 60 - col 30, line 12)." Applicant can properly show that Examiner's reliance on the cited portion of the reference to be in error. Applicant has done this by a through analysis of this cited portion of Portanova.

Applicant may also show that it is improper to combine references, such as when a secondary reference solves a different problem (*In Re Clay*, 23 USPQ 2d 1058). Since Onishi solves the problem of branch decoding by splitting a decoder into two parts, Applicant has pointed out that the branch decoder does not solve the problem of decoding two entirely different instruction sets, such as CISC and RISC. Both of Onishi's decoders merely decode different parts of a single instruction set.

Strained Combination of References

Portanova fails to provide any detail of CISC hardware implementation, since Portanova only emulates CISC instructions with RISC instructions. Examiner has attempted to rely on brief prior-art descriptions in Portanova of well-known CISC architectures for CISC hardware execution. This attempt fails because Portanova teaches away by showing that the RISC hardware can be used to emulate ANY of these different CISC architectures by first designing generic RISC hardware without regard to CISC, and then writing CISC emulation code containing RISC instructions. This speeds up his design time.

Examiner also cannot rely on these brief prior-art descriptions because they fail to disclose the structure recited in Applicant's claims. For example, having two instructions decoders (RISC and CISC) but only one execution unit is claimed by the elements of claim 18. However, Portanova does not disclose a CISC instruction decoder nor an execution unit capable of executing both RISC and CISC instructions.

Onishi is brought in as showing two instruction decoders, but this fails because Onishi's second decoder is merely a branch decoder, and not a decoder for a second (CISC) instruction set.

Onishi, like Portanova, completely lacks any teaching or suggestion of an

"execution unit, coupled to said RISC instruction decode means and said CISC instruction decode means, for executing instructions belonging to said RISC instruction set and instructions belonging to said CISC instruction set,

whereby instructions from said RISC instruction set and instructions from said CISC instruction set can be executed by said execution unit." (claim 18, emphasis added).

Now Tanenbaum, Lee et al., and Agnew et al. have been added to further strain the combination of references. Examiner is using Tanenbaum to suggest that software or hardware is merely a design choice. The two newly-cited references are used as "further evidences of hardware implementation as opposed to software implementation". However, neither reference teaches or suggests the hardware claimed by Applicant, such as the execute unit receiving decoded RISC and decoded CISC instructions. A "design choice" is another way saying "obvious to try".

Newly-Cited References Show Extensions of One Instruction Set

Applicant has reviewed the two newly-cited references. Lee et al. is clearly directed to an extension of a single instruction set rather than a separate second instruction set. Lee et al. teach an "assist" that is attached to the main processor via a set of busses (col 2, lines 40-45). Thus the "assist" appears to be the co-processor embodiment with a new name. Co-processors execute in hardware extensions of a single instruction set.

Agnew et al. also teach a single instruction set that is partitioned into two or more subsets, each possibly implemented in a different chip or emulated by software. His Figure 3 again shows a co-processor embodiment connected to a bus.

In contrast, Applicant's claim 1 recites "two separate instruction sets", and claim 18 recites a RISC and a CISC instruction set. Claim 1 clearly disallows a mere extension of a single instruction set by stating: "said first encoding of instructions independent from said second encoding of instructions". Mere extensions of instruction sets must have dependent encodings since otherwise one opcode could be used for two instructions. However, two separate instruction sets, such as RISC and CISC, will have one opcode with two different instructions. (Specification, page 25, lines 2-6.)

Examiner appears to be using these three new references to show that Portanova's RISC hardware can be modified to execute native CISC instructions. However, these newly-cited references only show separate co-processors that would have separate execute units. Also, these references show mere extensions to a single instruction set, such as for floating point instructions. Thus, even if these references were used as secondary references in a non-final action, these references do not teach or suggest a single execute unit that executes both RISC and CISC instructions.

Identification of Points of Agreement

Applicant believes that both parties agree that Portanova does not explicitly teach hardware execution of both RISC and CISC instruction sets. Portanova emulates all CISC instructions with routines of RISC instructions. Examiner acknowledges that "Portanova explicitly teaches an exemplary system that employs software implementation of CISC emulation in which each guest CISC instruction is emulated by a series of host RISC instructions." (page 4, lines 3-5, third action) Applicant understands this statement to mean that Portanova explicitly teaches only RISC hardware execution and only CISC software emulation.

Identification of Points of Disagreement for Appeal

Examiner believes that Portanova *suggests* hardware execution of CISC instructions in an otherwise RISC processor. This suggestion appears somewhere in col 29-30. Applicant has been unable to find this suggestion and has requested that the Examiner specifically point out what he is relying on. Applicant asserts that the CISC embodiments labeled "prior-art" for Figures 9-12 are nothing more than old processors that can only decode and execute just one instruction set.

It is not reasonable that a prior-art VAX combined with Portanova's RISC emulating CISC would suggest a single execute unit executing both RISC and CISC. Instead Portanova clearly teaches software ***emulation*** of CISC by RISC, so the CISC VAX would be implemented by software emulation. Simple statements that software and hardware are equivallent belittle microprocessor design and fail to teach or suggest a single RISC and CISC execute unit.

Examiner also asserts (page 4) that Applicant's argument that Portanova's Figures 9-12 apply only to a single instruction set fails because Portanova's context is a dual-instruction set processor. However, Portanova's definition of dual-instruction-set processor is one that emulates CISC by executing RISC. Applicant's definition of dual-instruction-set processor is one that executes both CISC and RISC. Thus the mere use of the term "dual-instruction-set processor" does not change what Portanova teaches or suggests, unless Applicant's definition of dual-instruction-set processor is used as a blueprint.

Examiner believes that it is within the ordinary skill level to have a single execute unit execute both RISC and CISC instructions. Examiner also believes that it is within the ordinary skill level to modify Onishi's branch decoder to decode a second instruction set, such as adding a CISC instruction decoder to a RISC processor. These beliefs are not reasonable.

Examiner's motivation for using Onishi's two decoders is that it "allows the system to decode instructions more efficiently because decoding of a branch instruction usually takes longer than that of a normal instruction." Applicant asserts that the fact that branch instructions may take longer to decode is not a relevant motivation to having separate RISC and CISC decoders, since both would decode branch instructions. Thus the motivation provided for combining Onishi with Portanova is irrelevant and not reasonable. The cited motivation shows Onishi to be directed to a different problem.

Scope of the Claims

Examiner admits that the detail of hardware implementation was not specified by either reference. However, "to the extent of the scope of the claims to design a processor capable of executing dual instructions sets where a subset of second instruction set is implemented partly with hardware, the teachings and suggestions from the applied references sufficiently meet the claim limitations." (page 5).

Applicant disagrees that Applicant is merely claiming a "processor capable of executing dual instructions sets", regardless of whether the second instruction set is wholly or partially implemented in hardware. That is not what the claims state. The claims recite at least a RISC and a CISC instruction decoder, and an execute unit that receives decoded RISC and decoded CISC instructions and executes both RISC and CISC instructions. Putting a PowerPC™ Mac and a 486 PC on a desk would allow execution of both a RISC and a CISC instruction set, but would not meet claim limitations of having the RISC and CISC decoders feed a single execute unit. Likewise putting Portanova's RISC CPU emulating CISC with a CISC VAX does not teach claim limitaions. Also a CPU die that has a RISC pipeline in one corner and a CISC pipeline in another corner would not meet the claim limitations since decoded RISC instructions are sent to the RISC execute pipeline while decoded CISC instructions are sent to the CISC execute pipeline.

Portanova, while appearing to "execute" dual instruction sets, also fails to teach or suggest claim limitations of a RISC and a CISC decoder which feed decoded instructions to an execution unit. The fact that Portanova discusses prior-art CISC architectures such as VAX and 68000 does not mean that he suggests executing both RISC and CISC decoded instructions on the same execute unit ! Portanova specifically teaches that these prior-art CISC architectures can be emulated with his RISC processor. As the official action notes, emulation means replacing a CISC instruction with a plurality of RISC instructions.

The official action on page 5 has thus broadened the scope of Applicant's claims. Even without the limitation of only a subset of the second instruction set being executed by the execute unit, the scope of the claims is narrower than merely executing dual instruction sets. The structure of two instruction-set decoders using a single execute unit is claimed but not taught or suggested by any cited reference. Indeed, Applicants believe that they have significantly advanced the state of the art by their invention which efficiently uses a single execute pipeline but two instruction decoders. Others will waste precious CPU die area by having two separate complete CISC and RISC execute pipelines. Applicant's invention is efficient and the public would benefit by its disclosure.

Other Claims Not Obvious & Show More Detail of Implementation

Some elements of dependent claims have not been shown in any of the references. For example, claim 3 claims a "mode register means, coupled to the select means, for indicating an instruction set to be decoded and executed." Examiner has not cited any reference with such a mode register. Further details of this mode register and control are presented in claims 4-5, 8, 13. Claims 18-19 recite that the mode register means indicates RISC mode, CISC mode, or an emulation mode. Nowhere has the Examiner

shown a teaching or suggestion for such a mode register indicating one of RISC, CISC, or emulation modes.

These claims were summarily rejected with no attempt at an element-by-element analysis. If these features are truly conventional, then the Examiner is obliged to cite references for these features or submit an affidavit. M.P.E.P. § 706.02(a). Clearly the scope and subject of these claims differ from the scope of other claims, and the Applicant deserves to have these claims examined too. M.P.E.P. §§ 904, 904.02. Applicant requests that all claims be given a complete examination.

In view of the above, it is submitted that claims 1-20, as amended, are in a position for allowance. Applicant requests that the requirement for formal drawings be held in abeyance until allowance. Applicant believes that a full and complete response to the office action has been made. Reconsideration and re-examination is respectfully requested. Allowance of the claims at an early date is solicited.

If the Examiner believes that a telephone interview would expedite prosecution of this application, he is invited to telephone the undersigned at (408) 476-5506.

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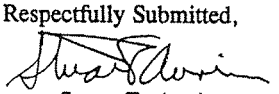
Respectfully Submitted,



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