EXHIBIT O

TABLE B: Applicant's limitation of the '750 invention to one that processes RISC and CISC instruction sets specifically		
Location in Prosecution History	**Reference(s) Distinguished**	**Applicant's Distinguishing Argument**
Amendment and Response at 12, Sept. 20, 1994 (Ex. D)	de Nicolas	"Nicolas neither teaches nor suggests a processor that can execute both CISC and RISC instructions in hardware."
Amendment and Response at 8, May 22, 1995 (Ex. H)	Portanova	"Applicant's definition of dual-instruction set processor is one that executes both CISC and RISC."
Amendment and Response at 9, May 22, 1995 (Ex. H)	Onishi	"The claims recite at least a RISC and a CISC instruction decoder, and an execute unit that receives decoded RISC and decoded CISC instructions and executes both RISC and CISC instructions."
Brief on Appeal at 2, Aug. 29, 1995 (Ex. I)		"A dual-instruction-set CPU is able to execute x86 CISC (complex instruction set computer) code or PowerPC RISC (reduced instruction set computer) code."
Brief on Appeal at 15, Aug. 29, 1995 (Ex. I)		"The claims recite at least a RISC and a CISC instruction decoder."
Reply Brief at 2, Nov. 29, 1995 (Ex. J)	Portanova	"The fact that Portanova is an emulator drives to the heart of this appeal: the complete, total absence of prior art showing both RISC and CISC hardware execution."