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EXHIBIT 13

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Pearl Po-Yee Cheng et al.

Assignee: Advanced Micro Devices, Inc.

Title: "MEMORIES HAVING A BURST MODE SEQUENTIAL ACCESS"

Serial No.: 07/836,667 Filing Date: 02/14/92

Examiner: S. Nadia Group Art Unit: 2312

Attorney Docket No.: M-2013 US

San Jose, California
September 23, 1994

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COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

AMENDMENT AFTER FINAL OFFICE ACTION

Sir:

In response to the Office Action dated June 23, 1994, please amend the above-identified application as follows.

IN THE SPECIFICATION

Page 10, line 30, replace "in" by --into--;

Page 10, line 31, before "subdivided" insert --is--;

Page 10, line 31, replace "in" by --into--.

REMARKS

Claims 2-26 are pending in the application and stand rejected. Reconsideration and withdrawal of the rejections is respectfully requested.

Claims 2-14 and 18-20 were rejected under 35 U.S.C. 102(b) over Pinkham. Claims 14-17 and 21-26 were rejected under 35 U.S.C. 103 over Pinkham in view of Rao. These rejections are respectfully traversed.

Claim 2 is directed to a memory that can overlap reading of memory locations in different memory rows. Claim 2 distinguishes from Pinkham and Rao, taken singly or together, by reciting a memory with a plurality of row decoders wherein at least two locations L1 and L2 in different memory rows can

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be read so that while one row decoder is activating a row portion comprising the location L1 and the contents of L1 are being transferred from one or more sense amplifiers to a memory output, another row decoder is activating a row portion comprising the location L2 in a different row and the contents of L2 are being transferred from L2 to one or more sense amplifiers.

Claim 2 is supported by Figs. 3A, 3B and 4. L1 reads on location M-12 in the first memory row (Fig. 3B). L2 reads on M-16 in the second row (Fig. 3A). The transfers recited in Claim 2 read on memory operations during time period t5 of Fig. 4. More particularly, prior to t5, X-decoder 316.R (Fig. 3B) activates a portion of the first row (specification, page 6, lines 25-26). During time period t4 still prior to t5, the contents of M-12 in the first row are transferred to sense amplifier 330.R-0 (Fig. 4). Then, during t5:

(1) the contents of M-12 are transferred from amplifier 330.R-0 to output DOUT, and

(2) at the same time, X-decoder 316.L (Fig. 3A) activates a portion of the second row (specification, page 8, lines 5-7), and the contents of M-16 are transferred from M-16 to amplifier 330.L-0.

The burst mode reading operation is fast as a result.

Pinkham does not teach or suggest simultaneous transfer in different memory rows as recited in Claim 2. Further, Pinkham does not teach or suggest plural row decoders to enable such a transfer as recited in Claim 2. Indeed, col. 4, lines 45-47 of Pinkham state with respect to his Fig. 1:

> Although the row . . . decoders are shown separate, each of the arrays 10-16 shares a common row decoder . . . .

Rao also does not teach or suggest simultaneous transfer in different memory rows as recited in Claim 2. Further, while Rao suggests the possibility of two X decoders (Rao, col. 3, line 40), Rao does not teach or suggest simultaneous activation

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of portions of different rows by his X-decoders as recited in Claim 2.

Thus Pinkham and Rao, taken singly or together, do not teach or suggest simultaneous transfer in different rows or simultaneous activation of portions of different rows as recited in Claim 2 and do not provide the attendant advantages. Claim 2 and Claims 3-6, 18 and 19 dependent therefrom are therefore believed to be allowable.

Claim 4 dependent from Claim 2 further distinguishes from Pinkham and Rao, taken singly or together, by reciting that when the contents of L1 are being transferred from one or more sense amplifiers to the memory output and the contents of L2 are being transferred from L2 to one or more sense amplifiers, the sense amplifiers from which the contents of L1 are being transferred are enabled and the sense amplifiers to which the contents of L2 are being transferred are disabled, but these latter sense amplifiers become enabled subsequently for amplifying the contents of L2.

Claim 4 is supported by the specification, page 8, line 23 through page 9, line 11. Sense amplifier 330.L-0 (Fig. 3A) is disabled while the contents of M-16 are being transferred to this sense amplifier and the contents of M-12 (Fig. 3B) are being transferred from sense amplifier 330.R-0 to the output. At the same time, sense amplifier 330.R-0 is enabled. Sense amplifier 330.L-0 becomes enabled subsequently. This technique "provides significant power saving". Specification, page 9, line 8.

Pinkham and Rao, taken singly or together, do not teach or suggest selective disabling of sense amplifiers as recited in Claim 4 and do not provide the attendant advantages. Claim 4 is believed to be allowable for this additional reason.

Claim 7 distinguishes from Pinkham and Rao, taken singly or together, by reciting a burst mode operation in which a plurality of memory locations are read out in response to one

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address and in which the memory locations are read with wrap-around so that the next location, if any, to be read out after the last-addressed location Ln is the first-addressed location L1.

Pinkham and Rao, taken singly or together, do not teach or suggest reading the first-addressed location after the last-addressed location in response to the same address as recited in Claim 7.

Moreover, Claim 7 distinguishes from Pinkham and Rao, taken singly or together, by reciting that while the contents of any location L to be read out other than the last location to be read out are being transferred from a sense amplifier means to a memory output, the contents of another location to be read out in response to the same address are being provided to the sense amplifier means for amplification and subsequent transfer to the output. Claim 7 and its dependent Claims 8-13 and 20 are therefore believed to be allowable.

In addition, Claim 8 dependent from Claim 7 and Claim 9 dependent from Claim 8 are believed to be allowable for reasons similar to the reasons discussed above in connection with Claim 4.

Claim 14 and its dependent Claims 15, 21 and 22 are believed to be allowable for reasons similar to the reasons discussed above in connection with Claim 2.

In addition, Claim 15 dependent from Claim 14 is believed to be allowable for reasons similar to the reasons discussed above in connection with Claim 4.

Claim 16 and its dependent Claim 17 are believed to be allowable for reasons similar to the reasons discussed above in connection with Claim 7.

In addition, Claim 17 is believed to be allowable for reasons similar to the reasons discussed above in connection with Claim 4.

Claim 23 distinguishes from Pinkham and Rao, taken singly

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or together, by reciting a memory having a plurality of subarrays with an X-decoder for each subarray and a Y-decoder for each subarray.

Claim 23 is supported by Figs. 3A, 3B showing X-decoders 316.L, 316.R and Y-decoders 318.L, 318.R for respective subarrays 314.L, 314.R. Providing an X-decoder and a Y-decoder for each subarray 314.L, 314.R allows simultaneous independent row and column selection in each subarray.

Pinkham provides only one row decoder and only one column decoder for his arrays of Fig. 1:

> Although the row and column decoders are shown separate, each of the arrays 10-16 shares a common row decoder and a common column decoder . . . .

Pinkham, col. 4, lines 45-48.

Moreover, Pinkham teaches away from separate column decoders by teaching that separate column decoders "would significantly increase the circuit density on a . . . chip." Pinkham, col. 6, lines 56-57.

Rao also teaches only one Y-decoder 16 (Fig. 1) which is associated with his array 10a (col. 3, line 45). Rao does not teach or suggest a Y-decoder for his other arrays 10b-10d. On the contrary, as Rao explains in col. 7, lines 1-2, his "arrays 10b-10d are constructed for only serial access", and Rao's serial access does not require a Y-decoder. More particularly, Rao's serial read access involves transferring memory bits "from the selected row" into a corresponding serial register, and then "shifting the data out serially". Rao, col. 6, lines 38-39 and 41. No Y-decoder is required.

Thus, Pinkham and Rao, taken singly or together, do not teach or suggest a Y-decoder for each of a plurality of subarrays as recited in Claim 23. Moreover, Pinkham teaches away from such Y-decoders, and Pinkham does not teach or suggest an X-decoder for each subarray as recited in Claim 23. Further, Pinkham and Rao do not provide simultaneous independent row and column selection as in some embodiments of

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Claim 23. Claim 23 and its dependent Claims 24-26 are therefore believed to be allowable.

In addition, Claim 26 is believed to be allowable for reasons similar to the reasons discussed above in connection with Claim 4.

Regarding paragraph 11 of the Office Action, Applicants thank the Examiner for considering the U.S. Patent No. 5,280,594 under Rule 56, and the undersigned attorney apologizes for inadvertently listing the U.S. patent application 07/557,899 as a "U.S. Patent Document" in the PTO 1449 form filed April 17, 1992. However, it is respectfully submitted that the application 07/557,899 should also be considered under Rule 56. Indeed, contrary to the suggestion in the Office Action, that application need not be listed as "Other Art" on PTO 1449. See MPEP § 609, last paragraph. Further, a statement of relevance mentioned in the Office Action need not be provided because the application 07/557,899 is in the English language. See 37 C.F.R. § 1.98(a)(3). The information regarding the application 07/557,899 was timely submitted under 37 C.F.R. § 1.97(b)(1) within three months of the filing date of the present application. Consideration of application 07/557,899 is therefore respectfully requested.

The specification is being amended to correct typographical errors.

In summary, Claims 2-26 were pending in the application and were rejected. Claims 2-26 are believed to be allowable, and early passage of this case to issue is respectfully requested. If any matters remain outstanding after consideration of this amendment, the Examiner is requested to

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telephone the undersigned at the number below to expedite prosecution of this case.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C., 20231, on September 23, 1994.

9-23-94 Michael Shenker

Date of Signature Attorney for Applicants

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