

EXHIBIT 14



UNITED STATES DEPARTMENT OF COMMERCE
 Patent and Trademark Office
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SERIAL NUMBER	FILED DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
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08/226,337 10/24/94 CHENG

P M20131CUG

EXAMINER RUDOLPH

EPHL/0205

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ART UNIT	PAPER NUMBER
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2312

281/H

DATE MAILED:

02/05/96

NOTICE OF ALLOWABILITY

PART I.

- This communication is responsive to *the Appeal Brief of October 2, 1995*
- All the claims being allowable. PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice Of Allowance And Issue Fee Due or other appropriate communication will be sent in due course.
- The allowed claims are *2-26*
- The drawings filed on *2/22/93* are acceptable
- Acknowledgment is made of the claim for priority under 35 U.S.C. 119. The certified copy has been received. not been received. been filed in parent application Serial No. _____ filed on _____
- Note the attached Examiner's Amendment.
- Note the attached Examiner Interview Summary Record, PTOL-413.
- Note the attached Examiner's Statement of Reasons for Allowance.
- Note the attached NOTICE OF REFERENCES CITED, PTO-892.
- Note the attached INFORMATION DISCLOSURE CITATION, PTO-1449

PART II.

A SHORTENED STATUTORY PERIOD FOR RESPONSE to comply with the requirements noted below is set to EXPIRE THREE MONTHS FROM THE "DATE MAILED" indicated on this form. Failure to timely comply will result in the ABANDONMENT of this application. Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

- Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.
- APPLICANT MUST MAKE THE DRAWING CHANGES INDICATED BELOW IN THE MANNER SET FORTH ON THE REVERSE SIDE OF THIS PAPER.
 - Drawing informalities are indicated on the NOTICE RE PATENT DRAWINGS, PTO-948, attached hereto or to Paper No. _____. CORRECTION IS REQUIRED.
 - The proposed drawing correction filed on *10/2/95, 3/24/94, 2/22/93, 10/8/92* has been approved by the examiner. CORRECTION IS REQUIRED.
 - Approved drawing corrections are described by the examiner in the attached EXAMINER'S AMENDMENT. CORRECTION IS REQUIRED.
 - Formal drawings are now REQUIRED.

Any response to this letter should include in the upper right hand corner, the following information from the NOTICE OF ALLOWANCE AND ISSUE FEE DUE: ISSUE BATCH NUMBER, DATE OF THE NOTICE OF ALLOWANCE, AND SERIAL NUMBER.

Attachments:

- | | |
|---------------------------------------------------------------------------------|------------------------------------------------------------------|
| <input checked="" type="checkbox"/> Examiner's Amendment | <input type="checkbox"/> Notice of Informal Application, PTO-152 |
| <input checked="" type="checkbox"/> Examiner Interview Summary Record, PTOL-413 | <input type="checkbox"/> Notice re Patent Drawings, PTO-948 |
| <input checked="" type="checkbox"/> Reasons for Allowance | <input type="checkbox"/> Listing of Bonded Draftsmen |
| <input type="checkbox"/> Notice of References Cited, PTO-892 | <input type="checkbox"/> Other |
| <input type="checkbox"/> Information Disclosure Citation, PTO-1449 | |

Rebecca L. Rudolph

REBECCA L. RUDOLPH
 PRIMARY EXAMINER
 GROUP 2300

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1. An Examiner's Amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 C.F.R. § 1.312. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the Issue Fee.

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Authorization for this Examiner's Amendment was given in a telephone interview with Michael Shenker on February 1, 1996.

2. The application has been amended as follows:

Please cancel claims 8 and 17.

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17. (Twice amended) A memory comprising:

a set of consecutively addressed memory locations L1, ..., Ln;

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a plurality of sense amplifier circuits [sense amplifier means] for amplifying contents of said memory locations; and

an output for providing output signals from said plurality of sense amplifier circuits [sense amplifier means],

wherein said memory has a burst mode operation for receiving an address and reading out to said output, in response to said address, any given number of memory locations in the sequence of consecutive addresses with wrap around so that the next location, if any, to be read out after said location Ln is said location L1, such that during said operation while the contents of any location L to be read out other than the last location to be read out are being transferred from said plurality of sense amplifier circuits [sense amplifier means] to said output, the contents of another location to be read out after said location L are being provided to said plurality of sense amplifier circuits [sense

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amplifier means] for amplification and subsequent transfer to said output

said memory further comprises a control circuit for selectively enabling said sense amplifier circuits so that said control circuit enables a sense amplifier circuit whose output signals are being transferred to the output of said memory but said control circuit does not enable all said sense amplifier circuits at the same time.

Claim 9, line 1, replace "8" by --7--.

10. (Amended) The memory of Claim 7 wherein:

said set of locations comprises k subsets S-1, ..., S-k wherein k is greater than or equal to two, such that, for a positive integer m and for any subset S-i, the contents of m consecutively addressed locations from said subset S-i can be transferred simultaneously to said plurality of sense amplifier circuits [sense amplifier means]; and

in said operation, time tARA does not exceed $m * (k-1) * (tOE)$, wherein:

tARA is measured from the time that an address of the first location to be read out in said operation is made available to said memory to the time when said plurality of sense amplifier circuits [sense amplifier means] develops an

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X2
output signal indicative of the contents of said first location; and

tOE is the time to transfer the contents of any one of said locations from said plurality of sense amplifier circuits [sense amplifier means] to said output.

13. (Amended) The memory of Claim 7 wherein in said operation any number of said locations addressed consecutively with wrap around can be read out to said output so that:

the first location to be read out in said operation is read out to said output after time $t_{ARA} + t_{OE}$ wherein:

X3
tARA is measured from the time that an address of said first location is made available to said memory to the time when said plurality of sense amplifier circuits [sense amplifier means] develops an output signal indicative of the contents of said first location; and

tOE is the time to transfer the contents of any one of said locations from said plurality of sense amplifier circuits [sense amplifier means] to said output of said memory; and

every other location to be read out in said operation is read out to said output within time tOE.

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14. (Twice Amended) In a memory comprising a set of consecutively addressed memory locations L1, ..., Ln, and a

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plurality of sense amplifier circuits, a method of reading out in burst mode a sequence of locations addressed consecutively with wrap around so that the next location to be read out after location Ln is location Ll, said method comprising the steps of :

receiving an address of a first location to be read out in burst mode; and

in response to said address, for each location of said sequence performing the steps:

sensing and amplifying contents of said location;

and

transferring amplified contents of said location to an output of said memory,

wherein for any location L of said sequence other than the last location to be read out in said sequence, the transferring step for the location L overlaps in time with the sensing and amplifying step for another location to be read out after said location L in said sequence; and for at least one location LL of said sequence, before the sensing and amplifying step for said location LL, the sense amplifier circuit which is to perform the sensing and amplifying step for the location LL is enabled, and after the transferring step for location LL, the sense amplifier circuit that has performed the sensing and amplifying step for location LL is disabled, and another sense amplifier circuit

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which is to perform the sensing and amplifying step for another location to be read out in said sequence is enabled.

3. The following is an Examiner's Statement of Reasons for Allowance:

Upon consideration of the Appellant's arguments in the Appeal Brief, it is apparent that the prior art does not teach or suggest the claimed invention. For example, claim 2 includes the features of a plurality of first registers and a plurality of row decoders where Pinkham (U.S. Patent No. 4,636,986) only teaches one. The plurality of registers and decoders is critical to the claims recitation of accessing at least two locations in different rows. Pinkham can only access one row at a time. Rao (U.S. Patent No. 4,347,587) also does not teach this feature. Claims 14 and 23 include similar language.

Claims 7 and 16 include the feature of selectively enabling and disabling sense amplifier circuits which is taught by neither Pinkham, Rao or Young et al. (U.S. Patent No. 5,280,594).

4. Any comments considered necessary by applicant must be submitted no later than the payment of the Issue Fee and, to avoid processing delays, should preferably **accompany** the Issue Fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

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UNITED STATES DEPARTMENT OF COMMERCE
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**NOTICE OF ALLOWANCE
AND ISSUE FEE DUE**

- Note attached communication from the Examiner
- This notice is issued in view of applicant's communication filed _____

SERIES CODE/SERIAL NO.	FILING DATE	TOTAL CLAIMS	EXAMINER AND GROUP ART UNIT	DATE MAILED
First Named Applicant				

TITLE OF INVENTION

ATTY'S DOCKET NO.	CLASS-SUBCLASS	BATCH NO.	APPLN. TYPE	SMALL ENTITY	FEE DUE	DATE DUE

THE APPLICATION IDENTIFIES ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED.

THE ISSUE FEE MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED.

HOW TO RESPOND TO THIS NOTICE:

- I. Review the SMALL ENTITY Status shown above.
 - If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:
 - A. If the status is changed, pay twice the amount of the FEE DUE shown above and notify the patent and Trademark Office of the change in status, or
 - B. If the Status is the same, pay the FEE DUE shown above.
 - If the SMALL ENTITY is shown as NO:
 - A. Pay FEE DUE shown above, or
 - B. File verified statement of Small Entity Status before, or with, pay of 1/2 the FEE DUE shown above.
- II. Part B of this notice should be completed and returned to the Patent and Trademark Office (PTO) with your ISSUE FEE. Even if the ISSUE FEE has already been paid by charge to deposit account, Part B should be completed and returned. If you are charging the ISSUE FEE to your deposit account, Part C of this notice should also be completed and returned.
- III. All communications regarding this application must give series code (or filing date), serial number and batch number. Please direct all communication prior to issuance to Box ISSUE FEE unless advised to contrary.

IMPORTANT REMINDER: Patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.