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EXHIBIT 17

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RESPONSE UNDER 37 C.F.R. §1.116
EXPEDITED PROCEDURE - EXAMINING GROUP [258]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

RECEIVED
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GROUP 250

In re Application	PATENT APPLICATION
Inventor: SAKAMOTO	
SC/Serial No.: 07/660,522	Art Unit: 258
Filed: 02/25/91	Examiner: Loke, S.
Title: IGFET AND METHOD OF FORMING	

CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8
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(Attorney Signature)
Gideon Gimlan, Esq., Reg. No. 31,955
Signature Date: July 7, 1992

Please enter amendment C, Loke. 7/14/92

RESPONSE UNDER 37 C.F.R. § 1.116
TO FINAL OFFICE ACTION

Box AF
Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

This RESPONSE is in reply to the Office action mailed May 19, 1992.

Amendments

Please amend the above-identified application as follows:

In the Drawings,

Subject to the approval of the Examiner, please amend FIG's. 1-9 of the drawings as shown in red and yellow on the enclosures, yellow indicating a region where lines/characters have been removed and red indicating a region where lines/characters have been added or clarified.

Please Replace the English Specification filed 2/25/91 with the Substitute English Specification also filed 2/25/91, and

In the Substitute Specification,

On page S1, line 10, please replace "date" with --gate--.

On page S2, line 22, replace "VG" with --V_G--.

On page S3, line 1, replace "Vs" with --V_{sub}--.

On page S3, line 12, replace "VD" with --V_D--.

On page S3, line 13, replace "VG" with --V_G--.

On page S3, line 16, replace "VD" with --V_D--.

On page S3, line 17, replace "VG" with --V_G--.

On page S5, line 17, replace "insulted" with --insulated--.

On page S8, line 6, replace "VG" with --V_G--.

On page S8, line 13, replace "V1" with --V_G--.

On page S8, line 20, replace "VG" with --V_G--.

On page S8, line 20, replace "VD" with --V_D--.

On page S10, line 14, replace "oxide film 2" with --new oxide film 2'--.

On page S10, line 17, replace "oxide film 2" with --new oxide film 2'--.

On page S10, line 18, replace "boron ions P+" with --boron ions B+ --.

In the Claims,

Please cancel claims 5 and 6 without prejudice.

Please amend claims 1 and 2 as indicated below.

-- 1. (Amended twice) An insulated gate field effect device comprising:

a first main conductivity type semiconductor substrate having a main surface; [,]

said semiconductor substrate having a concave [with a curved] surface formed on said main surface extending to a prespecified depth below the main surface;

an insulating film formed on [the main surface including] said concave surface;

a conductive gate electrode formed above said insulating film, overlying the concave surface;

first and second impurity regions of a second conductivity type respectively formed in the substrate, in the vicinity of said main surface, self-aligned to [of said semiconductor substrate,] and at one side and the other side of said gate electrode [concave] respectively; and [,]

a [said] first conductivity type region located in [of] said semiconductor substrate between said first and second impurity regions for defining [having] a channel region and a channel-free region (Lg2) extending conformably under and [formed] along said concave surface; [and]

[a conductive layer formed above said channel region with said insulating film interposed therebetween;]

wherein the depth of said concave surface is set to a value which ranges between one and two times the depth of said first and second impurity regions, and [and its twofold.]

Subt E1

C1

wherein the concave surface is continuously curved in the vicinity of at least one of the first and second impurity regions to produce smooth merger of a conforming first depletion region formed around the at least one impurity region and a conforming second depletion region formed in the vicinity of the gate electrode so that excessive field concentration will not develop in the vicinity where the first and second depletion regions meet.--

C1 concl'd.

-- 2. (Amended once) An insulated gate film effect device according to Claim 1, wherein one of said first and second impurity regions constitutes [one of a source region and] a drain region of said insulated gate field effect device, the other of said first and second impurity regions constitutes a [the other of said] source region [and said drain region, and said conductive layer constitutes a gate electrode of said insulated gate field effect device.] and wherein the concave surface is continuously curved at least in the vicinity of the drain region, where the channel-free region (Lg2) develops during an off state of the device, to produce smooth merger of the conforming first depletion region which develops in the vicinity of the channel-free region (Lg2) and the drain region and the conforming second depletion region formed in the vicinity of the gate electrode so that excessive field concentration will not develop in the vicinity of the channel-free region (Lg2).--

(Claim 3 was cancelled previously.)

Claim 4 continues to read as follows:

4. An insulated gate field effect device according to claim 1, which comprises a metal oxide semiconductor (MOS) transistor, and wherein said insulating film comprises an oxide film.

NOT ENTERED

Please add new claims 7-14 as shown below.

-- 7. (New) An insulated-gate field effect transistor comprising:

a substrate having a substantially planar main surface and a concave surface portion extending continuously from the main surface to a predetermined depth below the main surface;

an insulating layer conformably disposed on the main surface and the concave surface portion;

a gate conformably disposed on the insulating layer, overlying the concave surface portion, the gate having opposed first and second sides;

implanted source and drain regions disposed within the substrate and self-aligned to the respective first and second opposed sides of the gate; and

a channel-region formed between the source and drain regions, for defining a channel that conducts current between the source and drain regions when the transistor is in a turned-on state;

wherein a channel-free zone develops in the substrate, under the gate and between the source and drain regions, when the transistor is in a turned-off state; and

wherein the gate and concave surface portion are curved at least in the vicinity of the channel-free zone such that a smoothly curved depletion zone boundary will develop in the vicinity of the channel-free zone when the transistor is in the turned-off state.--

C2 cont'd.

-- 8. (New) An insulated-gate field effect transistor according to Claim 1 wherein the concave surface portion is curved in a transverse cross-sectional plane extending through the transistor between but not intersecting the first and second sides of the gate so as to provide an effective channel width greater than the width of the channel as projected onto the plane of the main substrate surface.--

-- 9. (New) An insulated-gate field effect transistor according to Claim 8 wherein the concave surface portion is curved both in the transverse cross-sectional plane and in a non-transverse cross-sectional plane, extending between and joining the first and second sides of the gate, so as to provide an effective channel surface area greater than the area of the channel as projected onto the plane of the main substrate surface.--

-- 10. (New) An insulated-gate field effect transistor according to Claim 9 wherein the concave surface portion is equally curved both in the transverse cross-sectional plane and in the non-transverse cross-sectional plane, so as to provide a sheet-like depletion region having a uniform thickness and a smooth bottom boundary underlying the channel region and the source and drain regions, when the transistor is in a turned-off state.--

C2 contd.

-- 11. (New) An insulated-gate field effect transistor according to Claim 7 wherein the concave surface portion is continuously curved from the point where it descends below and away from the main surface of the substrate to the point where it ascends to re-join the main surface of the substrate.--

-- 12. (New) An insulated-gate field effect transistor according to Claim 7 wherein the gate fills the void created by the concave surface portion and insulating layer at least from the level where the concave surface portion and insulating layer descend below the level of the main surface of the substrate.--

-- 12. (New) An insulated-gate field effect transistor according to Claim 7 wherein the concave surface portion is defined by isotropic plasma etching or focal ion beam etching.--

13. (New) An insulated-gate field effect transistor according to Claim 7 wherein the depth of the concave surface portion is set to a value which ranges between one and two times the depth of the source and drain regions.--

14. (New) An insulated-gate field effect transistor according to Claim 7 wherein the depth of the drain region is 0.5 to 0.6 microns and the depth of the concave surface portion is set to approximately one micron.-

Remarks

The above Amendments and these Remarks are in reply to the Office action mailed MAY 19. 1992.

Claims 1, 2 and 4 remain pending in the application.

Claims 1 (amended once), 2 and 4 were finally rejected for lack of support in the original disclosure. These claims were also rejected as being fully anticipated by the newly applied Takeda reference (IEEE Trans. Electron Devices, June 1983).

Applicant's amendment of 3/9/92 was objected to because Fig.s 6-9 were not labeled "prior art" and because the requested insertion/deletions of words on pages 1, 5 and 8 could not be found. Reconsideration and allowance are requested.

Summary of Amendment

Claims 1 and 2 are amended. Claims 5 and 6 are withdrawn as requested by the Examiner. Claims 7-14 are newly submitted. The Specification and Drawings are also amended to correct various informalities.

Request for Withdrawal of Action Finality

The Substitute English Specification which was filed 2/25/91, states at page S10, line 22 - page S11, line 8:

> [T]he depth of the concave ... is preferably set to the same value of depth of the source 4 and drain 5. The effect of the embodiment of the invention is most significant **when the depth of the concave is set to a value which ranges between the depth of the source 4 and drain 5 and its twofold.**

> [Underlining, bolding and bracketed text are added for emphasis.]

The same text is also found in the original English Specification (which specification is a translation of the Japanese priority document also filed 2/25/91) at page 12, lines 9-21.

The Examiner justifies the finality of the latest Office Action as being necessitated by Applicant's previous amendment, presumably because the Examiner finds a lack of support in the Specification for Applicant's application to Claim 1.

The above replicated portion of the Specification makes it clear that the basis for final rejection is not justified and thus premature. Withdrawal of the finality is therefore respectfully requested.

Alternatively, if the finality is not reversed, entry of the above amendments is requested pursuant to 37 C.F.R. §1.116. The amendments were not earlier presented because the relation of the newly-applied Takeda reference to claims of record was not understood.

Advantages of the Disclosed Invention

The invention is primarily concerned with deleterious

effects that develop in an insulated-gate field-effect transistor (IGFET) while the IGFET is turned off.

Application Fig. 7 (prior art) shows a depletion region comprised of sections 20 and 29 being formed conformably under curved source/drain regions 4, 5 and under planar gate 21 of a prior-art device.

Because the curvatures of source/drain regions 4, 5 merge abruptly into the planar shape at the bottom of gate 21 (and the top planar surface of substrate 6), a trapezoidal region 20 with sharp corners develops as part of the depletion region. The sharp corners produce undesirable field concentration (the "fringe effect" mentioned at Specification page S4), particularly in the vicinity of drain region 5.

Application Fig. 9 (prior art) shows that the bottom-right corner of trapezoidally-shaped depletion region 20 develops in the vicinity of the channel-free length, L_{g1}, which is a small portion of the overall channel length, where the channel stops during device shut-off and the drain-to-source voltage gradient develops. (See Specification page S3, lines 17-22.)

Application Fig. 1 shows a depletion region comprised of sections 10 and 9 being formed conformably under curved source/drain regions 4, 5 and under curved gate 1 of a device in accordance with the invention. Because the curvature of depletion section 10 merges smoothly into the curved shape of depletion sections 9 (defined by source/drain regions 4, 5), the overall depletion region, 9, 10 takes on a smooth sheet-like shape (recited as "strip" like in the English translation at Specification page S9, lines 15-24). The smooth merger of

sections 9 and 10 reduces undesirable field concentration, particularly in the vicinity of drain region 5.

Application Fig. 4 shows that the channel-free length L_{g2} changes little as a function of gate length. Accordingly, very small devices can be made without the problem of subthreshold current flow. (See Specification page S9, lines 23-24.)

Differences Between Claim 1 and Art of Record

Claim 1 is amended to recite "wherein the concave surface is continuously curved in the vicinity of at least one of the first and second impurity regions to produce smooth merger of a conforming first depletion region formed around the at least one impurity region and a conforming second depletion region formed in the vicinity of the gate electrode so that excessive field concentration will not develop in the vicinity where the first and second depletion regions meet."

Support for this amendment is found in Application Fig. 4 and in the overall language of the Specification. It should be understood that the present Specification was derived from a Japanese-language original (the priority document, which was also filed 2/25/91), and as such, certain differences of language usage and idiomatic problems have made their way into the translation process.

In particular, Specification page S9, lines 15-24 speak of a "strip" depletion layer 10 formed "along" the concave of Fig.s 2 and 4 and distinguish this "strip" depletion layer 10 from the trapezoid configuration 20 of Fig.s 7 and 9 and the "fringe effect" associated therewith. Those skilled in the art

will recognize this language as referring to the smoothness with which the gate depletion region meets with the drain depletion region and the electric field concentration which develops in the vicinity of the channel-to-drain juncture (L_{g1} of Fig. 9 vs. L_{g2} of Fig. 4).

The applied art neither teaches nor suggests a device according to Claim 1.

The newly applied Takeda reference (Grooved Gate MOSFET with DSC structure) is interested in creating a nonimplanted region between the drain and channel in order to reduce electric field at the drain (page 681, left column, last 3 lines). Takeda Fig. 2(e) shows how this is done. Prior to boron (B+) implant, overhangs are formed by side-etching to cover the left and right ends of the channel groove. The channel groove, incidentally, is shown to have a trapezoidal shape in Fig. 2(e). The overhangs protect the dashed-circled corners of the trapezoidal groove from boron bombardment (page 682, left column, lines 7-15).

Takeda et al use grooving merely as a convenient means for creating the overhangs and subsequent DSC (Drain Separated from Channel) structure. They do not recognize the advantages of a "curved" grooved structure for minimizing fringe effects. They actually teach away from such a direction by stating at page 685, last line through page 686, first paragraph:

> Also it would be better to realize the DSC MOS structure without the groove. ... If such a simple DSC structure were realized, it would become an ideal MOS structure.
> [Underlining added.]

Moreover, Takeda et al admit that their proposed structure

lacks self-alignment between the gate and the source/drain junctions (page 685, last paragraph). This is evident from Takeda Fig. 2(c) where the N+ doping for the source/drain regions occurs prior to gate formation (Fig. 2(h)).

Claim 1 has been amended to recite "first and second impurity regions of a second conductivity type respectively formed in the substrate, in the vicinity of said main surface, self-aligned to and at one side and the other side of said gate electrode respectively". This clearly distinguishes the subject matter of Claim 1 over the Takeda reference.

With regard to the earlier applied Kotani reference (No. 52-15274), it is not clear from the abstract whether the source and drain are self-aligned to the gate, but this is irrelevant since the gate groove is not continuously curved as recited in Claim 1 of the present case.

Differences Between Claim 7 and Art of Record

Claim 7 is newly introduced to clarify certain aspects of the invention not covered by Claim 1.

Claim 7 recites "wherein a channel-free zone develops in the substrate, under the gate and between the source and drain regions, when the transistor is in a turned-off state; and wherein the gate and concave surface portion are curved at least in the vicinity of the channel-free zone such that a smoothly curved depletion zone boundary will develop in the vicinity of the channel-free zone when the transistor is in the turned-off state."

The prior art of record neither teaches nor suggests such

a structure for the same reasons applied to Claim 1. Claim 7 and all its dependencies should be found patentably distinguishable over the art of record at least for this reason.

Differences Between Dependencies of Claim 7 and the Art of Record

Claim 8 is newly introduced to point out the differences between the transverse cross-sections of Application Fig.s 3 and 8. Note that Fig. 3 shows a curved, and thus effectively larger, channel width, W_{e2}.

The art of record does not disclose such a configuration. Takeda et al mention a "narrow-channel effect" at page 682, last paragraph. But the method by which the latter is overcome according to Takeda is through side-etching in the direction of the channel width (page 683, left column, first paragraph).

Claim 10 is newly introduced to point out further differences between the transverse cross-sections of Application Fig.s 3 and 8. Note that the concave surface portion in Fig. 3 shows a curve similar to that shown in the non-transverse cross section of Fig. 2. This indicates that the concave surface can be curved in two directions, and the resulting sheet (strip) of depletion formed under the gate is uniformly and smoothly curved in both directions. The art of record is silent in this regard.

Claim 11 is newly introduced to point out that the illustrated concave surface of Application Fig.s 1-5 is continuously curved. This maximizes the effective channel length (and width) relative to the drawn length (and width) while meeting other objectives of the invention (e.g. avoiding

excessive field concentration). The Takeda reference does not teach this concept in full. Fig. 1 of Takeda indicates a effective channel length (L_{eff}=2.7 microns) greater than the drawn length (L_D=2.5 microns) but the groove has a substantially flat bottom portion. It is not continuously curved. Thus, it does not take full advantage of the concept and does not minimize the space occupied by the transistor for a given channel length.

Claim 12 is newly introduced to point out that the illustrated gate of Application Fig.s 1-5 fills the void created by the concave surface portion and the conforming insulating layer. The art of record does not show such a structure. Note that the void-filling gate of the present invention helps to better mask the underlying channel region during boron implant.

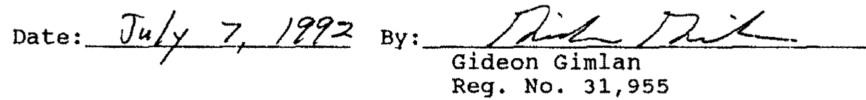
Claim 14 recites the specific dimensions given at Specification page S11, lines 3-5.

With regard to the drawings, Fig.s 6-9 have been labeled "prior art" as requested by the Examiner. The channel-free length (L_{g1}) of Fig. 9 has been more prominently marked to clarify the points being made by that figure and its accompanying text. Support for the change is found at Specification page S3, lines 17-19.

In view of the above Amendments and Remarks, reconsideration of Claims 1, 2 and 4 is requested and consideration of newly added Claims 7-14 is also requested.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 06-1325 for any matter in connection with this response, including any fee for extension of time, which may be required.

Respectfully submitted,



Date: July 7, 1992 By: ______________________
Gideon Gimlan
Reg. No. 31,955

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application	PATENT APPLICATION
Inventor: SAKAMOTO	
SC/Serial No.: 07/660,522	Art Unit: 258
Filed: 02/25/91	Examiner: Loke, S.
Title: IGFET AND METHOD OF FORMING	

CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8

I hereby certify that this correspondence is being deposited in the United States Postal Service with sufficient postage as first class mail in an envelope addressed to **Commissioner of Patents and Trademarks, Box AF, Washington, D.C. 20231**, on July 7, 1992.

______________________(Attorney Signature)
Gideon Gimlan, Esq., Reg. No. 31,955
Signature Date: July 7, 1992

RESPONSE TRANSMITTAL LETTER

Box AF
Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

Transmitted with this communication in connection with the above-identified application are the following:

___ A Response under 37 C.F.R. § 1.111 to the Office Action dated _____.

X A Response under 37 C.F.R. § 1.116 to the Final Office Action dated May 19, 1992.

___ A Petition for an Extension of Time under 37 C.F.R. §1.136.

___ A Verified Statement pursuant to 37 C.F.R. §1.27 to establish small entity status under 37 C.F.R. §1.9(f).

The fee associated with this communication has been calculated as shown below:

___ No fee is required with this communication.

___ Small entity status of this application under 37 C.F.R. §1.9 and §1.27 has been established.

___ A fee for extension of time for response under 37 C.F.R. §1.136 filed within __ month(s) after the original time for response of $______ is due.

___ A fee for addition of claims under 37 C.F.R. § 1.17 is due as follows:

Claims Remaining After Amendment	Highest Previously Paid For	Number Extra	Rate Small entity/ Other Than Small Entity
Total Claims 14 -	[20 or more]=	0 X	$ 10.00 $ 20.00 = $ 0.00
Independent Claims 2 -	4 =	0 X	$ 36.00 $ 72.00 = $ 0.00
First Presentation of Multiple Dependent Claim(s) ____			$110.00 $220.00 = $

*If the difference is less than zero, enter "0".

Additional Fee $ 0.00

The total fee required with this communication is $0.00 and is to be paid as follows:

___ Please charge Deposit Account No. 06-1325 in the amount of $_________. A duplicate copy of this authorization is enclosed.

___ A check in the amount of $______ is enclosed.

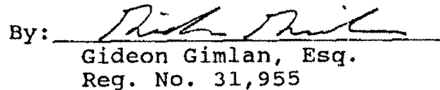
_X_ The Commissioner is hereby authorized to charge underpayment of any fees, including the following fees, associated with this communication or credit any overpayment to Deposit Account No. 06-1325. A duplicate copy of this authorization is enclosed.

_X_ Any filing fees under 37 C.F.R. §1.16 for the presentation of additional claims.

_X_ Any patent application processing fees under 37 C.F.R. §1.17 including any applicable fee for extension of time.

Respectfully submitted,

Date: July 7, 1992

By: 
Gideon Gimlan, Esq.
Reg. No. 31,955

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Attach

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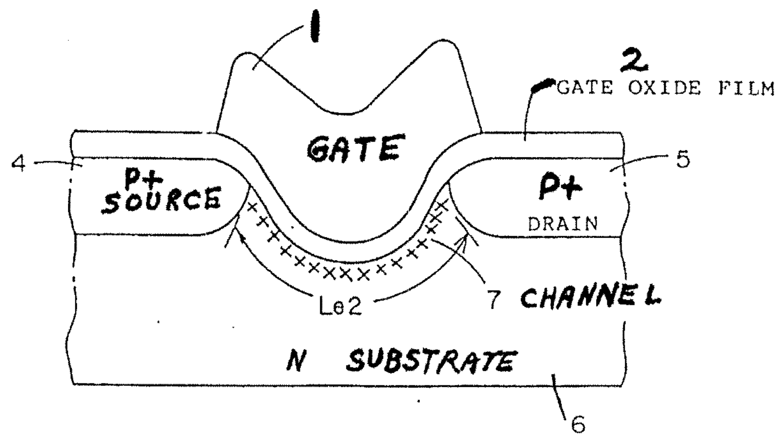

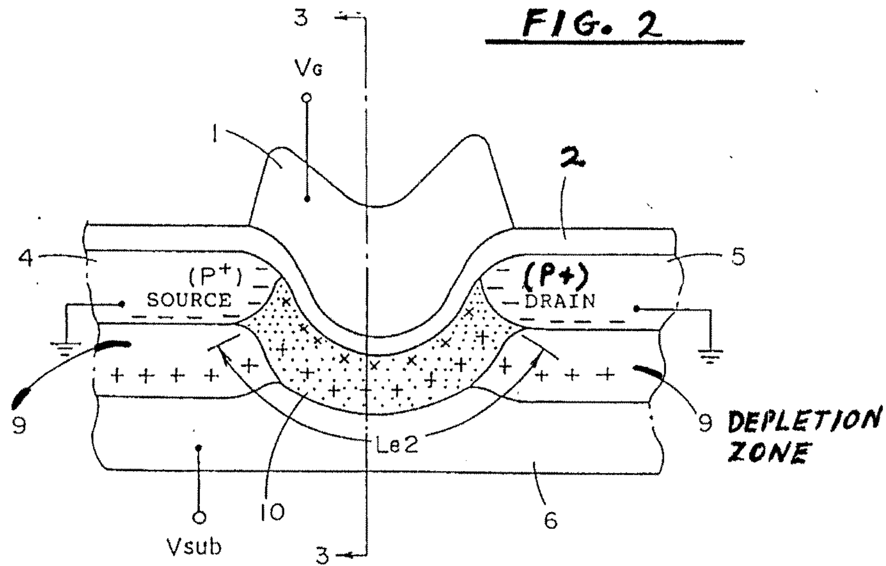

approved
Loke
7/14/92

FIG. 3

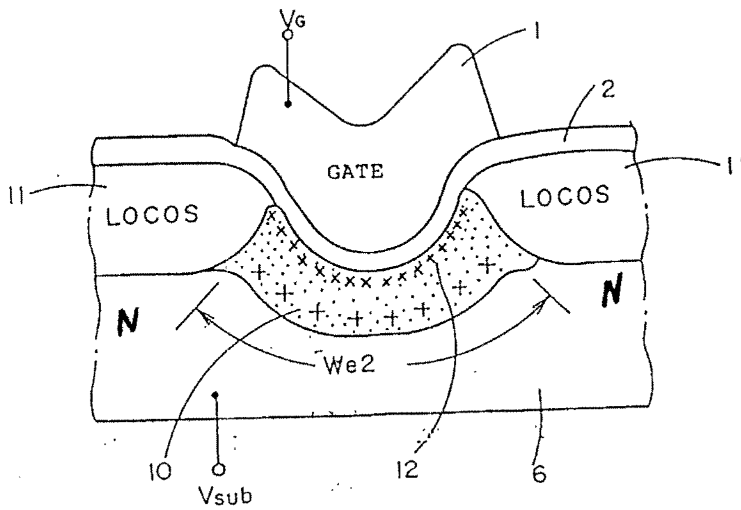

FIG. 4

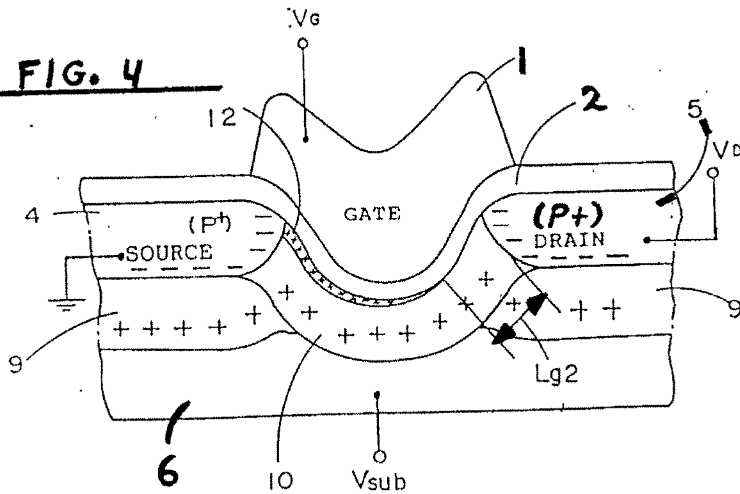

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FIG. 5A

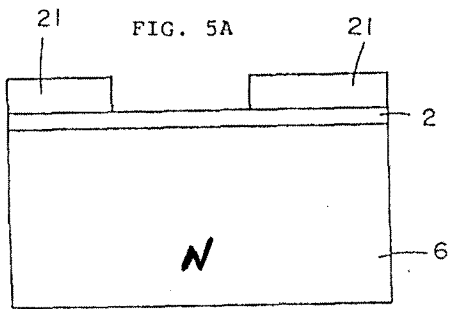


FIG. 5B

PLASMA ETCHING OR EB ETCHING

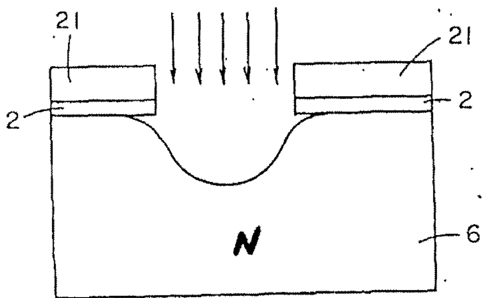


FIG. 5C

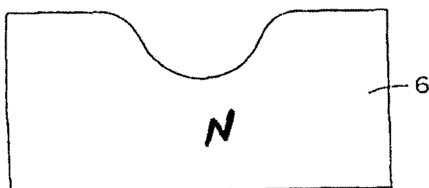


FIG. 5D

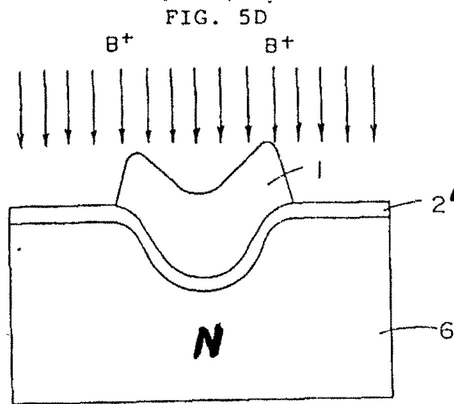
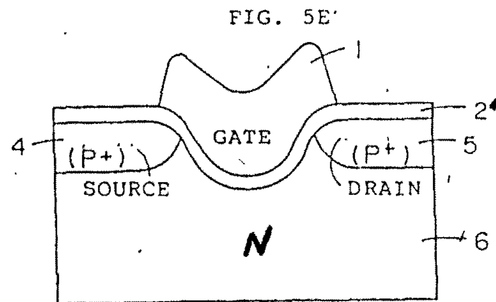


FIG. 5E



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7/14/92

FIG. 6
(PRIOR ART)

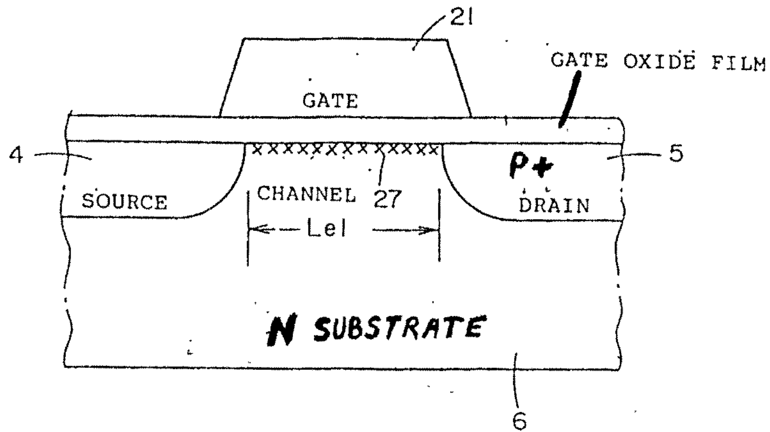
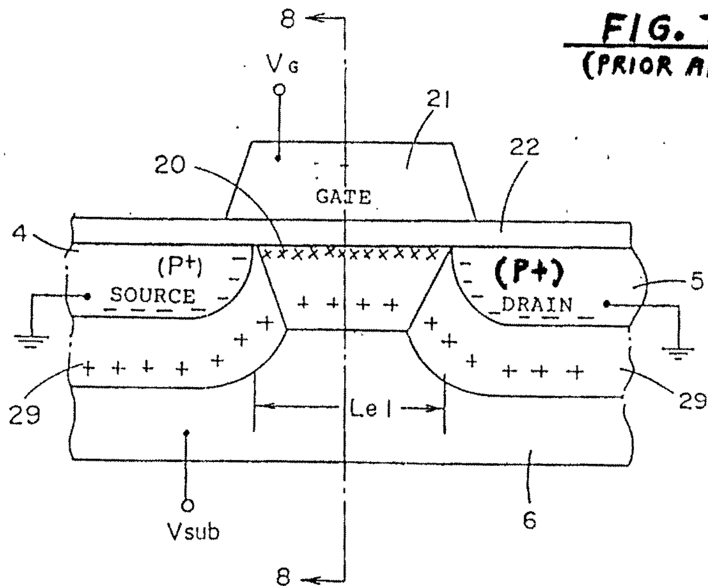


FIG. 7
(PRIOR ART)



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Loke
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FIG. 8
(PRIOR ART)

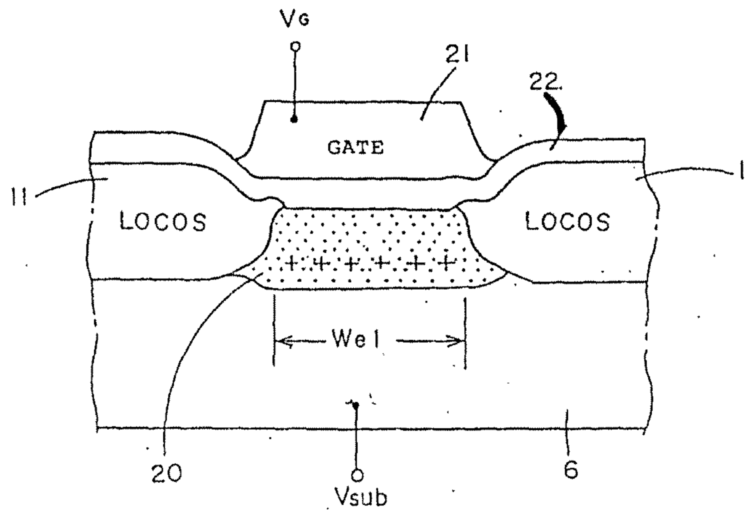
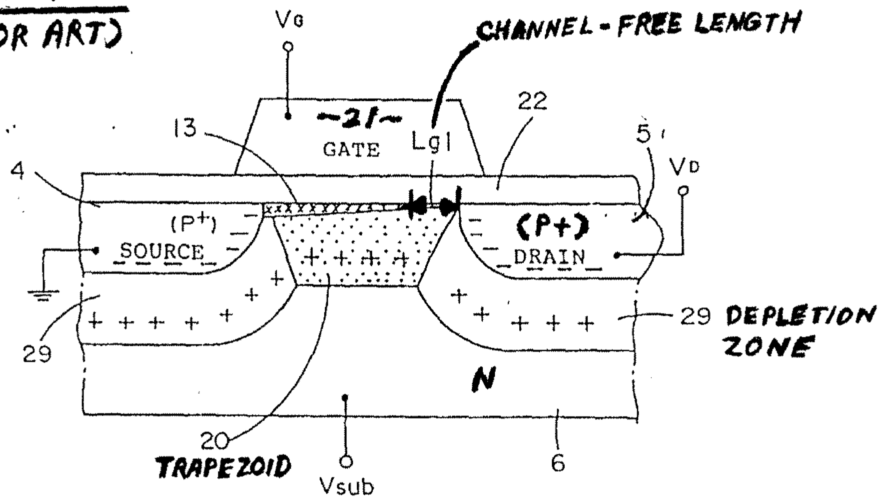


FIG. 9
(PRIOR ART)



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