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EXHIBIT 19

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RESPONSE UNDER 37 C.F.R. §1.116
EXPEDITED PROCEDURE - EXAMINING GROUP [ ]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application	PATENT APPLICATION
Inventor: Shinichi Sakamoto	Art Unit: 2508
SC/Serial No.: 07/660,522	Examiner: S. Loke
Filed: February 25, 1991	
Title: INSULATED GATE FIELD EFFECT DEVICE AND METHOD OF FORMING	

CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8

I hereby certify that this correspondence is being deposited in the United States Postal Service with sufficient postage as first class mail in an envelope addressed to **Commissioner of Patents and Trademarks, Box AF, Washington, D.C. 20231**, on November 10, 1992.

(Attorney Signature)
Gideon Gimlan, Esq., Reg. No. 31,955
Signature Date: November 10, 1992

Please enter amendment D
Loke
11/20/92

RESPONSE UNDER 37 C.F.R. § 1.116

Box AF
Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

This RESPONSE is in reply to the Final Office action dated July 22, 1992.

Amendments

Please amend the above-identified application as follows:

In the Claims.

Claims 1, 2, 4, and 7-15 were pending in the Application at the time of the latest Office action. All next pending Claims,

whether amended or not, are reproduced below for the Examiner's convenience.

Please amend Claims 1 and 13 as indicated below. Also please add Claims 16 and 17 as shown below.

1. (Amended three times) An insulated gate field effect device comprising:

a first ~~main~~ conductivity type semiconductor substrate having a main surface;

said semiconductor substrate having a concave surface formed on said main surface extending to a prespecified depth below the main surface;

an insulating film formed on said concave surface;

a conductive gate electrode formed above said insulating film, overlying the concave surface;

first and second impurity regions of a second conductivity type respectively formed in the substrate, in the vicinity of said main surface, self-aligned to and **positioned** at one side and the other side of said gate electrode respectively; and

a first conductivity type region located in said semiconductor substrate between said first and second impurity regions for defining a channel region and a channel-free region ~~(Lg2)~~ extending conformably under and along said concave surface;

wherein the depth of said concave surface is set to a value which ranges between one and two times the depth of said first and second impurity regions, and

wherein the concave surface is continuously curved in the vicinity of at least one of the first and second impurity regions to produce smooth merger of a conforming first depletion region formed around the at least one impurity region and a conforming second depletion region formed in the vicinity of the gate electrode so that excessive field concentration will not develop in the vicinity where the first and second depletion regions meet.--

Claims 2, 4 and 7-12 continue to read as:

2. (Amended once) An insulated gate ~~film~~ field effect device according to Claim 1, wherein one of said first and second impurity regions constitutes a drain region of said insulated gate field effect device, the other of said first and second impurity regions constitutes a source region and wherein the concave surface is continuously curved at least in the vicinity of the drain region, where the channel-free region ~~(Lg2)~~ develops during an off state of the device, to produce smooth merger of the conforming first depletion region which develops in the vicinity of the channel-free region ~~(Lg2)~~ and the drain region and the conforming second depletion region formed in the vicinity of the gate electrode so that excessive field concentration will not develop in the vicinity of the channel-free region ~~(Lg2)~~.

(Claim 3 was cancelled previously.)

3. An insulated gate field effect device according to claim 1, which comprises a metal oxide semiconductor (MOS) transistor, and wherein said insulating film comprises an oxide film.

(Claims 5 and 6 were cancelled previously.)

4. An insulated-gate field effect transistor comprising:

a substrate having a substantially planar main surface and a concave surface portion extending continuously from the main surface to a predetermined depth below the main surface;

an insulating layer conformably disposed on the main surface and the concave surface portion;

a gate conformably disposed on the insulating layer, overlying the concave surface portion, the gate having opposed first and second sides;

implanted source and drain regions disposed within the substrate and self-aligned to the respective first and second opposed sides of the gate; and

a channel-region formed between the source and drain regions, for defining a channel that conducts current between the source and drain regions when the transistor is in a turned-on state;

wherein a channel-free zone develops in the substrate, under the gate and between the source and drain regions, when the transistor is in a turned-off state; and

wherein the gate and concave surface portion are curved at least in the vicinity of the channel-free zone such that a

smoothly curved depletion zone boundary will develop in the vicinity of the channel-free zone when the transistor is in the turned-off state.

6 ~~8~~. An insulated-gate field effect transistor according to Claim 4 ~~7~~ wherein the concave surface portion is curved in a transverse cross-sectional plane extending through the transistor between but not intersecting the first and second sides of the gate so as to provide an effective channel width greater than a ~~the~~ width of the channel as projected onto the plane of the main substrate surface.

6 ~~9~~. An insulated-gate field effect transistor according to Claim 5 ~~8~~ wherein the concave surface portion is curved both in the transverse cross-sectional plane and in a non-transverse cross-sectional plane, extending between and joining the first and second sides of the gate, so as to provide an effective channel surface area greater than an ~~the~~ area of the channel as projected onto the plane of the main substrate surface.

7 ~~10~~. An insulated-gate field effect transistor according to Claim 6 ~~9~~ wherein the concave surface portion is equally curved both in the transverse cross-sectional plane and in the non-transverse cross-sectional plane, so as to provide a sheet-like depletion region having a uniform thickness and a smooth bottom boundary underlying the channel region and the source and drain regions, when the transistor is in a turned-off state.

11. An insulated-gate field effect transistor according to claim 7 wherein the concave surface portion is continuously curved from the point where it descends below and away from the main surface of the substrate to the point where it ascends to re-join the main surface of the substrate.

12. An insulated-gate field effect transistor according to claim 7 wherein the gate fills the void created by the concave surface portion and insulating layer at least from the level where the concave surface portion and insulating layer descend below the level of the main surface of the substrate.

--12. ["second" 12]. (Amended once) An insulated-gate field effect transistor according to claim 7 wherein the concave surface portion is defined by isotropic plasma etching **[or focal ion beam etching]**.--

Claims which were erroneously numbered as 13 and 14 in the previous amendment are renumbered as shown below to correct the numbering error.

11 ~~14~~ [13]. An insulated-gate field effect transistor according to Claim 4 ~~7~~ wherein the depth of the concave surface portion is set to a value which ranges between one and two times the depth of the source and drain regions.

12 ~~15~~ [14]. An insulated-gate field effect transistor according to Claim 4 ~~7~~ wherein the depth of the drain region is 0.5 to 0.6 microns and the depth of the concave surface portion is set to approximately one micron.

-- 13 ~~16~~. (New) An insulated-gate field effect transistor according to Claim 4 ~~7~~ wherein the concave surface portion is defined by focal ion beam etching.--

-- 14 ~~17~~. (New) An insulated-gate field effect transistor comprising:

a substrate having a substantially planar main surface and a concave surface portion extending continuously from the main surface to a predetermined depth below the main surface;

an insulating layer conformably disposed on the main surface and the concave surface portion;

a gate conformably disposed on the insulating layer, overlying the concave surface portion, the gate having opposed first and second sides;

implanted source and drain regions disposed within the substrate **respectively at** the first and second opposed sides of the gate, **the drain region having a bottom surface which curves upwardly toward the top surface of the substrate**; and

a channel-region formed between the source and drain regions, for defining a channel that conducts current between the source and drain regions when the transistor is in a turned-on state;

wherein a channel-free zone develops in the substrate, under the gate and between the source **region** and **the upwardly curved bottom surface of the** drain region, when the transistor is in a turned-off state; and

wherein the gate and concave surface portion are curved at least in the vicinity of the channel-free zone, **and the upwardly curved bottom surface of the drain region is also ~~so~~ curved,** such that a smoothly curved depletion zone boundary will develop in the vicinity of the channel-free zone when the transistor is in the turned-off state.

Remarks

The above Amendments and these Remarks are in reply to the Office action dated July 22, 1992. Claims 1, 2, 4, 7-15 were pending in this case.

Due to a numbering error, two Claims 12 were presented in the last amendment. The second Claim 12 is renumbered above as Claim 13 and Claims 13 and 14 are subsequently renumbered as Claims 14 and 15. It is assumed the Examiner has done the same in his records. We apologize for the confusion.

Claims 7 and 11-13 stand rejected under 35 U.S.C. §103 as being obvious Takeda, et al. No art is applied against remaining Claims 1, 2, 4, 8-10, 14 and 15.

Claims 1, 2, 4, 8-10, 12 and 13 are rejected under 35 U.S.C. §112 for indefiniteness. Claims 1, 14 and 15 are indicated to be allowable if rewritten to overcome the indefiniteness rejection.

Claim 1 is amended above to recite "self-aligned to and positioned at one side and the other side of said gate electrode respectively; and ...". This correction is believed to overcome the indefiniteness rejection and to place Claim 1 in condition for allowance. Entry of the amendment is requested pursuant to 37 C.F.R. §1.116. The error results from an oversight in the previous response and was thus not earlier presented.

Dependent Claims 2 and 4 should be found in condition for allowance for the same reason.

Claims 8-10 and 12 depend from Claim 7 rather than from Claim 1. As such, rejection of Claims 8-10 and 12 on the basis of an indefiniteness found in Claim 1 is improper. Withdrawal of the final rejection of Claims 8-10 and 12 is requested.

Independent consideration of Claims 8-10 and 12 on the merit of specific limitations found therein is also requested. Note that Claim 8 is directed to the "transverse" cross section. See application Fig. 3. No prior art has been applied against the subject matter of Claims 8-10 or the subject matter of Claim 12. As such, these claims should be deemed in condition for allowance.

Claims 7, 11-13 stand rejected under 35 U.S.C. §103 as being obvious over Takeda.

Takeda fails to teach or suggest that portion of Claim 7 which recites:

> wherein the gate and concave surface portion are curved at least in the vicinity of the channel-free zone such that a smoothly curved depletion zone boundary will develop in the vicinity of the channel-free zone when the transistor is in the turned-off state.
> [Underline added for emphasis.]

The gate, channel and drain of the Takeda structure are not curved to produce the recited function.

Takeda also fails to teach or suggest that portion of Claim 7 which recites:

> implanted source and drain regions disposed within the substrate and self-aligned to the respective first and second opposed sides of the gate; and
> [Underline added for emphasis.]

In rejecting Claim 7, the Examiner contends:

> Since Takeda et al teaches a transistor structure similar to the claimed invention, it would have been obvious to one of ordinary skill in the art to have a channel-free zone in Takeda et al because Takeda et al has a grooved-gate MOSFET similar to the claimed invention.

Applicant respectfully submits that the focus of the above grounds for rejection is misdirected. Referring to Fig. 9 (admitted prior art) of the present application, it is seen that a "channel-free" zone (which is the region labeled Lg1) develops even in a non-grooved transistor.

The point of attention is not on whether a channel-free zone (e.g., the region labeled Lg1 in Fig. 9) develops in a

grooved or ungrooved transistor, but rather what the shape of the depletion zone (see elements 20 and 29 of Fig. 9) will be in the vicinity of the channel-free zone.

Takeda fabrication diagrams 2(e)-(j) clearly indicate that the gate and the gate groove are intended to be trapezoidal in shape rather than smoothly curved. The bottom of the drain (n+) is flat and it terminates abruptly against the groove side in Takeda Fig. 2(e).

In Takeda Fig. 1, it is again seen that the drain bottom surface is flat and terminates abruptly at the groove sidewall. The curvature of the gate breaks away from that of the groove in the vicinity of the drain/channel junction. Such a structure tends to produce a nonuniform distribution of doping impurities at the substrate surface. This and the flat structure of the drain's bottom surface tends to produce the undesired fringing effect. There is no teaching to suggest that a smoothly curved depletion zone boundary will develop in Takeda in the vicinity of its channel-free zone when the transistor is in the turned-off state.

In contra-distinction, Fig. 2 of the present application shows a curved drain bottom joining a curved channel groove such that a depletion zone composed of merged depletion subregions 9 and 10 forms. Fig. 4 of the present application shows a smoothly curved depletion boundary forming in the vicinity of "channel-free" zone Lg2.

If the Takeda reference is considered in whole, for what it fairly teaches one of ordinary skill in the art; it is seen that Takeda proposes a completely different solution to breakdown in

the drain/channel region.

In Takeda, the lightly-doped channel region (P-) separates the moderately doped (P) channel from the heavily doped (N+) drain region to provide increased breakdown voltages. Takeda focuses on the length of the lightly doped channel as the reason for improved breakdown characteristics. (See Takeda, Page 683, second column, last paragraph.) This is very different from focusing on the shape of the gate and channel regions and the shape of the resultant depletion region. Reconsideration and allowance of Claim 7 is requested.

Claim 13 (which was previously the second Claim 12) is rejected in part because of the use of the expression "or". Applicant proposes to delete "or focal ion beam etching" thereby overcoming this ground of rejection. Newly introduced claim 16 separately recites "focal ion beam etching". Entry and reconsideration are respectfully requested.

Claim 13 (which was previously the second Claim 12) is further rejected because the Examiner contends that product-by-process steps such as "isotropic plasma etching" and "focal ion beam etching" are non-limiting (the latter by-process language has been moved to claim 16). In re Hirao 190 USPQ 15, and its progeny are cited in support of this position.

Interestingly enough, a similar issue lies at the heart of an inter-panel dispute currently ongoing within the CAFC. See Atlantic Thermoplastics Co. v. Faytex Corp., 23 USPQ.2d 1801 (CAFC 1992) [In banc reheating denied, Nies, Rich, Newman, Lourie dissenting] (But see also the concurring opinion of J. Rader at 24 USPQ.2d 1138).

The questions implicitly raised and answered by the Examiner in the present case, as far as Applicant understands it, are these:

> Given a first claim (7) which recites a novel product (but which product is argued by the Examiner to be obvious); is any weight to be accorded to a further recitation in a dependent claim (13 and 16), that the product is made by "isotropic plasma etching" or "focal ion beam etching"? Does the by-process language make the dependent claim (13 or 16) different in ANY patentably recognizable way from the base claim (7)? The Examiner appears to have responded with an unequivocal NO to both questions.

Applicant respectfully disagrees.

The above questions are not the same as asking whether the subject matter of a single "by-process" product claim distinguishes over a non-novel prior art structure where the only difference is the process of making. In the latter case, the burden is rightfully placed on the Applicant to show that the "by-process" product is novel relative to the prior-art product. No amount of artful dodging should allow the Applicant to remove from the public domain, a product that was already in the public domain.

In re Hirao 190 USPQ 15, and its progeny start off with this public policy as their underpinning. (Hirao, incidentally, was not a product-by-process case but rather a case involving a claim for "A process for preparing foods and drinks sweetened mildly ..." by a 3-step process, the first 2 steps of which produced high purity maltose, a known sweetener.)

The present case is different at its start, however, because the Examiner implicitly admits that the thing being claimed, even without the process limitation, is novel. The implicit admission comes from the application of only a §103 obviousness rejection and not a §102 anticipation rejection to base claim 7.

The question then becomes whether the Examiner can rightfully maintain that for the case of claim 13, "the process limitation of how the concave surface portion is formed <u>has NO patentable weight</u> in [a] claim drawn to structure." (Underlining and capitalization added for emphasis. Bracketed text added for clarity.)

Applicant respectfully urges the Examiner to re-read <u>In re Hirao</u> 190 USPQ at 17-18. The holding in that case does not say one should ignore the process limitations, but rather:

> The obviousness of the invention <u>as a whole</u> must be determined, and the unobvious first two [elements/] steps are clearly part of the invention as a whole.
>
> 190 USPQ at 17. [Emphasis is in the original. Bracketed text is added.]

In light of this, it is respectfully submitted that final rejection of claim 13 without giving its limitations any weight whatsoever is improper and the finality of the rejection should be removed.

Notwithstanding the above, Applicant submits that the "by-process" product of Claim 13 is patentably different from the product of Claim 7 at the microscopic level even though the products may appear to be the same at the macroscopic level.

Those skilled in the art recognize that different results

can be obtained in semiconductor devices by choosing anisotropic etching as opposed to isotropic etching and vice versa.

In the present instance, it is a goal of the invention to provide a "smoothly" curved depletion zone boundary, as is recited in Claim 7. Isotropic etching proceeds uniformly in all directions as opposed to anisotropic etching which does not have uniform etch properties in all directions. As such, isotropic plasma etching tends to provide a surface polishing action that leaves behind a desired, relatively "smooth" surface. Anisotropic etching, on the other hand, has a tendency to create overhangs and sharp sidewalls. The latter results are not helpful to the goal of the present invention.

Focal ion beam etching (Claim 16) is a relatively new etching technology which is expected to provide smooth surface textures in the submicron regime. As such, a submicron device produced by focal ion beam etching should be found patentably distinguishable over one made by anisotropic etching.

Given that surface smoothness is affected by production process, and given that surface smoothness is relevant to the operation of the claimed subject matter, it is respectfully submitted that the by-process limitations of Claims 13 and 16 deserve to be given full consideration when determining the patentability of these claims.

The art of record fails to teach or suggest the subject matter of claims 13 and 16. Accordingly they should be found allowable on their own merit.

Newly submitted Claim 17 distinguishes over Takeda in that Takeda does not have a drain with an upwardly curved bottom

surface. Entry and allowance are respectfully requested.

In view of the above Amendments and Remarks, reconsideration of pending Claims 1, 2, 4, and 7-15 is requested and entry plus consideration of newly added Claims 16 and 17 is requested.

Enclosed is a PETITION FOR EXTENSION OF TIME UNDER 37 C.F.R. § 1.136 for extending the time to respond up to and including November 23, 1992.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 06-1325 for any matter in connection with this response, including any fee for extension of time, which may be required.

Respectfully submitted,

Date: Nov. 10, 1992 By: ______________________
Gideon Gimlan, Esq.
Reg. No. 31,955

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application	PATENT APPLICATION
Inventor: Shinichi Sakamoto	Art Unit: 2508
SC/Serial No.: 07/660,522	Examiner: S. Loke
Filed: February 25, 1991	
Title: INSULATED GATE FIELD EFFECT DEVICE AND METHOD OF FORMING	

CERTIFICATE OF MAILING UNDER 37 C.F.R. § 1.8

I hereby certify that this correspondence is being deposited in the United States Postal Service with sufficient postage as first class mail in an envelope addressed to **Commissioner of Patents and Trademarks, Box AF, Washington, D.C. 20231**, on November 10, 1992.

_______________ (Attorney Signature)
Gideon Gimlan, Esq., Reg. No. 31,955
Signature Date: November 10, 1992

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RESPONSE TRANSMITTAL LETTER

Box AF
Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

Transmitted with this communication in connection with the above-identified application are the following:

___ A Response under 37 C.F.R. § 1.111 to the Office Action dated _____.

X A Response under 37 C.F.R. § 1.116 to the Office Action dated July 22, 1992.

X A Petition for an Extension of Time under 37 C.F.R. §1.136.

___ A Verified Statement pursuant to 37 C.F.R. §1.27 to establish small entity status under 37 C.F.R. §1.9(f).

The fee associated with this communication has been calculated as shown below:

___ No fee is required with this communication.

___ Small entity status of this application under 37 C.F.R. §1.9 and §1.27 has been established.

_X_ A fee for extension of time for response under 37 C.F.R. §1.136 filed within _1_ month after the original time for response of $110.00 is due.

___ A fee for addition of claims under 37 C.F.R. § 1.17 is due as follows:

Claims Remaining After Amendment		Highest Previously Paid For		Number Extra		Rate Small entity/ Other Than Small Entity
Total Claims 14	-	[20 or more]	=	0 *	X	$ 11.00 $ 22.00 = $ 0.00
Independent Claims 3	-	3	=	0 *	X	$ 37.00 $ 74.00 = $ 0.00
First Presentation of Multiple Dependent Claim(s) ____						$115.00 $230.00 = $ 0.00

*If the difference is less than zero, enter "0".

Additional Fee $ 0.00

The total fee required with this communication is $110.00 and is to be paid as follows:

___ Please charge Deposit Account No. 06-1325 in the amount of $________. A duplicate copy of this authorization is enclosed.

_X_ A check in the amount of $110.00 is enclosed.

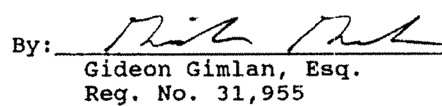
X The Commissioner is hereby authorized to charge underpayment of any fees, including the following fees, associated with this communication or credit any overpayment to Deposit Account No. 06-1325. A duplicate copy of this authorization is enclosed.

X Any filing fees under 37 C.F.R. §1.16 for the presentation of additional claims.

X Any patent application processing fees under 37 C.F.R. §1.17 including any applicable fee for extension of time.

Respectfully submitted,

Date: 11/10/92

By: 
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