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ROBERT T. HASLAM (Bar No. 71134)
RHaslam@cov.com
MICHAEL K. PLIMACK (Bar No. 133869)
MPlimack@cov.com
CHRISTINE SAUNDERS HASKETT (Bar No. 188053)
CHaskett@cov.com
COVINGTON & BURLING LLP
1 Front Street, 35th Floor
San Francisco, California 94111
Telephone: (415) 591-6000
Facsimile: (415) 591-6091

ALAN H. BLANKENHEIMER (Bar No. 218713)
ABlankenheimer@cov.com
LAURA E. MUSCHAMP (Bar No. 228717)
LMuschamp@cov.com
JO DALE CAROTHERS (Bar No. 228703)
JCarothers@cov.com
COVINGTON & BURLING LLP
9191 Towne Centre Drive, 6th Floor
San Diego, California 92122
Telephone: (858) 678-1800
Facsimile: (850) 678-1600

Attorneys for Defendants and Counterclaimants
SAMSUNG ELECTRONICS CO., LTD., et al.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

ADVANCED MICRO DEVICES, INC., et al.,

Plaintiffs and Counterdefendants,

v.

SAMSUNG ELECTRONICS CO., LTD., et al.,

Defendants and Counterclaimants.

Case No. 3:08-CV-0986-SI

DECLARATION OF RICHARD PASHLEY IN SUPPORT OF SAMSUNG'S RESPONSIVE CLAIM CONSTRUCTION BRIEF

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I, Richard Pashley, declare as follows:

1. I have been retained as an expert in this case by the Defendant-Counterclaimant Samsung entities ("Samsung"). No part of my compensation is dependent upon the particular outcome of this case or any issue in it.

2. I submit this Declaration in support of Samsung's responsive claim construction brief.

3. I am over eighteen years of age and I am competent to testify as to the matters set forth herein if I am called upon to do so. If called as a witness, I could and would competently testify about the facts and opinions set forth herein.

4. I have been retained to investigate certain issues related to U.S. Patent No. 5,559,990 (the '990 patent) asserted by Plaintiff AMD against Samsung. Based on my analysis and investigation, I have reached certain conclusions and developed certain opinions that I discuss in this declaration. These statements are made of my own personal knowledge and in accordance with 28 U.S.C § 1746.

5. The opinions expressed in this declaration are based on the information currently available to me. I reserve the right to continue my investigation and study, which may include a review of documents and information that may be produced, as well as deposition testimony from depositions for which transcripts are not yet available or that may not yet have been taken in this case. Therefore, I expressly reserve the right to expand or modify my opinions as my investigation and study continue, and to supplement my opinions in response to any additional information that becomes available to me, any matters raised by the Plaintiff and/or other opinions provided by the Plaintiff's expert(s), or in light of any relevant orders from the Court or other authoritative body.

6. In making the statements in this declaration, I rely on my personal knowledge, education, and professional experience. Attached as Exhibit A is a true and correct copy of my curriculum vitae, which summarizes my education and professional qualifications.

Qualifications and Professional Experience

7. Most of my career was spent at Intel Corporation working on memory products. I personally designed or managed the design of over 60 commercial memory products, including

SRAM, NVRAM, EPROM, EEPROM, Flash, and memory cards, in my 25 years at Intel. During my stay at Intel, I worked in a wide range of technical positions,serving as an integrated circuit design engineer, a device physicist, a process engineer, a project manager, a product design manager, and a director of technology development. In the second half of my career at Intel, I was fortunate enough to have the opportunity to do a business startup using one of the memory technologies, namely flash, that my team developed while I was in the technology development side of Intel. I summarize my educational and professional background below.

Educational Background

8. I received my bachelors degree in physics from the University of Colorado in 1969, and my M.S. and Ph.D. degrees in electrical engineering from the California Institute of Technology in 1970 and 1974, respectively. My Doctorial thesis investigated the electrical properties of ion implantation in silicon and Gallium Arsenide. I pioneered the development of the ion implanted GaAs MOS transistor resulting in a ground breaking patent on the fabrication of the GaAs Mosfet. During my stay at Caltech, I successfully petitioned the Graduate School of Electrical Engineering to create a class in integrated circuit design. In this class and in a subsequent research project under Dr. Carver Meade, I designed two memory integrated circuits that were fabricated at Intel Corporation. Both integrated circuits worked on first silicon. The work on the second Caltech integrated circuit resulted in a publication in the IEEE JSSC entitled a "128-Bit Multicomparator."

Professional Experience

9. I was employed by the Intel Corporation from 1973 through 1998. From 1973 to 1976, I worked as an engineer managing a small technology development team where I personally designed an EPROM and many SRAM memory devices. My duties in this period included silicon process development, transistor level device physics analysis, creation of transistor simulation tools, memory circuit design, initial memory device debugging/testing, and reliability data analysis. During this time period, I developed Intel's High Performance MOS technology (HMOS) and the use of on chip back-bias. The combination of the HMOS technology and the utilization of on chip back-bias doubled the speed of Intel's SRAM products. I presented a landmark ISSCC paper on a

4K bit 70ns SRAM in 1977 that broke the bipolar memory speed barrier. I also drove Intel's "optical chip shrink" strategy for SRAM and microprocessor products.

10. From 1977 through 1980, I was Intel's Manager of the Static Logic Technology Development Department where I was responsible for developing Intel's static random access memory (SRAM) products and the associated silicon manufacturing processes for SRAM memory, microcontroller, and microprocessor products. In this position, I pioneered the development of redundancy to improve memory wafer yields and lower unit costs by over 50%. My team developed and put into production the second generation HMOS fabrication process and several SRAM products. In addition, we developed an ECL 4K SRAM and a Silicon on Sapphire 1K SRAM that were functional but did not go into production.

11. From 1980 through 1982, I became Intel's Manager of Non-Volatile Technology Development Department where I was responsible for Intel's non-volatile memory technology/product development and Intel's basic technology development (photolithography, etching, deposition, etc). In this position, I developed and transferred into production four EPROM & EEPROM silicon technologies and their associated memory products ranging in density from 4K to 256K bits. Noteworthy was the design and successful transfer to production of the world's first 5V only electrically erasable programmable memory (EEPROM) design and developing and transferring Intel's first CMOS EPROM technology into production.

12. From 1983 through 1986, I served as Director of California Technology Development (combination of Microprocessor/SRAM and Non-Volatile Memory Directorships). Under my guidance, a multitude of new SRAM, EPROM, EEPROM, and microprocessor silicon fabrication technologies and their associated products were developed and transferred into production. In this timeframe, the highest volume writeable nonvolatile memory, the EPROM, was under extreme price pressure due to a maturing market with over 20 competitors. In addition, customers were growing weary of the ultraviolet light erase required to reprogram an EPROM. They wanted the electrically erase capability of the new high priced EEPROM technology at EPROM prices. This spurred me to search for the "holy grail of nonvolatile memory," the single transistor electrically erasable memory. In 1985, Toshiba was the first to announce a single

transistor electrically erasable memory and coined the name "Flash Memory" as the new device erased in a "flash". Unfortunately, Toshiba's initial Flash product was unmanufacturable and difficult to use and, as a result, a market failure. Meanwhile, I negotiated a joint development partnership with Xicor Corporation to develop a single transistor EEPROM technology. While the single transistor EEPROM looked good on paper, the reality was the cell operating window was nonexistent and the partnership was dissolved. Fortunately for Intel, I had initiated a parallel internal Intel development on an EPROM based Flash memory technology as a "skunkworks project." By 1985, I had a working 64Kb Flash memory in the lab. But to my surprise, the Intel EPROM business unit was not interested in commercializing Flash, claiming that the market would not accept it based on Toshiba's lack of success and a fear of Flash cannibalizing Intel's own EPROM business. I approached Gordon Moore, CEO of Intel, and expressed my frustration with this decision. Gordon recognized that Flash was a "disruptive" new technology that could open new markets for Intel. As a result of this discussion with Gordon, I was offered the unique position of becoming the general manager of a flash memory startup business unit inside Intel.

13. In 1986, I left the pure R&D side of Intel and started up Intel's Flash memory business unit. As the General Manager of the Flash Memory Business, I directed all aspects of the business, including engineering, manufacturing, marketing and financial. Early in 1988, we began selling our first Flash memory product, the 256Kb.With over 95% of its manufacturing steps the same as an EPROM, the Intel Flash technology was able to quickly ramp up in volume using existing EPROM manufacturing plants. By 1990, Intel's Flash business revenue had grown to $25 million capturing 90% of the total Flash market. My Flash Memory Business's technological accomplishments include the development and the successful transfer to production of the 1st and 2nd Generation Flash Silicon Technologies (1.2μ and 1μ Lithography), incorporating these technologies into Intel's 2864 (64 Kb), 28256(256 Kb), 28512 (512 Kb) and the 28010 (1 Mb) Flash memory products. This success drove the creation of new Flash memory markets, such as digital camera "film", cell phone code store, PC Bios store, automotive engine control, and EPROM replacement. The first real time demonstration of a digital camera using a Flash "film card" was in April of 1988 during the Intel 256Kb Flash product introduction at the Eiffel Tower in

Paris. During my presentation, I took a picture of a journalist in the audience; and then, electronically, we placed the journalist on a beach in Tahiti.

14. By 1990, Intel's Flash Memory Business was so successful that Intel rewarded my Flash efforts by giving me the additional responsibility of Intel's EPROM Business, with the merged entity becoming Intel's Memory Component Division. Under my business and engineering leadership, Intel's Flash business grew from $25 million in 1990 and to $500 million in 1994. During this period, the Division achieved a number of technological accomplishments under my leadership, including:

- Developing and transferring into production Intel's 3rd, 4th, and 5th generation Flash technologies (0.8 μ, 0.6 μ, and 0.4 μ lithography, respectively) and the associated Flash file memories, boot Bios memories, automotive sectored products ranging in density from 256K to 8M bit;
- Initiated the development of Intel's multi-level cell Flash technology, resulting in the world's first commercially viable memory product implementing this new technology;
- Developed and transferred into production Intel's 10M byte flash ATA equivalent of a magnetic hard drive;
- Developed and transferred into production several generations of Intel Flash memory cards ranging in density from 1M to 40M bytes;
- Successfully negotiated a flash joint development/manufacturing agreement with Sharp Corporation to increase our flash manufacturing capacity beyond what Intel was capable of providing for our rapidly growing flash business;
- Developed 5V-only Flash circuits with on-chip voltage pumps for high voltage generation and on-chip programming/erase control circuits;

In recognition for these accomplishments, I was appointed Vice President of Intel in 1993.

15. I returned to my engineering roots in 1994 and became the Engineering Manager of Intel's Memory Component Division where I was responsible for finishing the development and transferring into production the world's first multi-level cell Flash devices, developing and transferring into production Intel's 5th generation Flash technology and developed Intel's 1st generation Compact Flash memory card products. I retired from Intel in 1998.

16. Since 1999, I have served as an adjunct professor in the Graduate School of Engineering at the University of California Davis, teaching a course on technology management. From 1998 to 2001, I also served as an adjunct professor at U.C. Davis's Graduate School of

Management, offering a class on technology management based on my years of industry experience.

17. During my professional career, I have been a member of the *Phi Beta Kappa* Society (national honor society), the *Sigma Pi Sigma* Society (National Physics Honor Society), the *Sigma Xi* Society (the oldest and largest scientific organizations in the world, dedicated to scientific research), the *Institute of Electrical and Electronics Engineers* ("IEEE," the world's leading professional association for the advancement of technology), and the *Bohmische Physikalische Gesellschaft*.

18. My services to various professional industry groups include serving on the program committee of the IEEE International Solid-State Circuits Conference (ISSCC) in 1980-1985 and from 1988-1990, and acting as the guest editor for the October 1982 *IEEE Journal of Solid-State Circuits*' special issue on logic and memory.

19. I have authored or co-authored over 40 publications in this field of technology, and I am named as the inventor or a co-inventor on 17 U.S. patents covering ion implantation, metal oxide semiconductor (MOS) processing and design, SRAM, EPROM devices and Flash EEPROM devices among other inventions. I have included a complete list my publications and patents in Exhibit B of this Declaration.

Basis for Opinions

20. In preparing this declaration, I have reviewed the '990 patent and the prosecution history for the '990 patent. I have reviewed the references cited on the face of the '990 patent. I also relied on my personal expertise of over 25 years in the field of memory devices, during which I designed or supervised the design over 60 memory devices. I have also reviewed literature in my possession that shows the state of the art of memory devices at the time the patent was filed.

Overview of Technology Disclosed in '990 Patent

21. The '990 patent discloses a memory with boundaryless burst mode access. The boundaryless burst mode access is alleged to be an improvement over prior art memories having burst modes that read four consecutive locations in response to a single address. ['990 Patent, Col.

1:36-40] The boundaryless burst mode access allows for any number of consecutive locations to be read in response to a single address. ['990 Patent, Col. 1:58-64]

22. The '990 Patent discloses multiple subarrays, each with its own dedicated circuitry, to implement the boundaryless burst mode operation by interleaving and alternating accesses among the subarrays. The patent further discloses multiple column groups in each subarray to implement the boundaryless burst mode operation by interleaving and alternating accesses among the subarrays/column groups. In the '990 Patent, the standard read access is broken into two parts; the portion from the memory cell row/column access to the sense amplifier inputs and the portion from the sense amplifier transfer to the memory output (output buffer). In a simplified view, the boundaryless burst is achieved by interleaving these two portions of the standard memory read access to improve read access time performance. This interleaving is accomplished by transferring data associated with the start address in one subarray or column group from this subarray's sense amplifiers to the memory output; while at the same time accessing data associated with the next consecutive address in another subarray or column group and placing this data on the inputs of the its subarray's sense amplifiers. By alternating this interleaving process, the claimed boundaryless burst is achieved.

Level of Skill in the Art

23. The claimed technology involves relatively sophisticated memory technology. Thus, a person of skill in the art would have a relatively high level of skill in designing electrical circuits, at least some of which involved the design of memory products. More specifically, a person of skill in the art would have a Bachelor's degree in electrical engineering with 4-5 years experience designing electrical circuits or a Master's degree in electrical engineering with 2-3 years experience designing electrical circuits, with at least one year of this experience involving the design of memory products.

"Integrated Memory"

24. The '990 patent discloses a memory device. The patented invention is depicted at the block diagram level and shows known circuits such as registers, decoders, sense amplifiers and memory cells which are arranged and operated in an allegedly novel manner.

25. The '990 patent specifically provides that the invention is independent of whether the memory device is integrated as a integrated circuit or is part of an integrated memory system. ['990 Patent, Co. 7:9-10 ("Memory 810 is fabricated in an integrated circuit in some embodiments."); Col. 13:8-9 ("Further, some embodiments are not integrated into one integrated circuit.")]

26. Dr. Wolfe interprets the Pinkham patent to teach that the term "integrated memory" is the same as the term "integrated circuit". I have reviewed the Pinkham reference, U.S. Patent No. 4,636,986 ("the '986 Patent"), and disagree with Dr. Wolfe's conclusions. Pinkham does not use integrated memory interchangeably with the term integrated circuit. Rather, Pinkham teaches a method of manufacturing multiple integrated memories on a single integrated circuit. ['986 Patent, Col. 2:9-39] Using Dr. Wolfe's interpretation of the term "integrated memory," one would expect a single integrated circuit for each of the integrated memories discussed in the '986 Patent. But this is simply not true, as the citation that Dr Wolfe provides in the '986 Patent states: "...each of the integrated memories must maintain some degree of independence relative to the other memories on the same chip...." The term "integrated memory" in the '986 Patent simply means that each of these integrated memories contain a memory array, and all the necessary associated circuitry such as the row/column decoders and sense amplifiers, as shown in Figure 1 of the '986 Patent.

27. I agree that an "integrated circuit" is an electronic device consisting of all its circuit elements formed on a single silicon chip. However, an "integrated memory" is a memory system that has all its components integrated in a single apparatus (e.g. a memory card with multiple integrated circuit memories), but is not necessarily formed on a single piece of silicon. The word "integrated" in "integrated memory" means that the memory apparatus must contain all the necessary support components inside the apparatus (e.g. a self-contained apparatus and not a memory with components distributed throughout a computer system). Examples of an "integrated memory" are a memory card, a USB jump drive, an add-on memory printed circuit board, and a solid state flash disk drive. All of these integrated memory devices contain memory control circuitry as well as one or more memory array chips. These "integrated memories" typically contain multiple integrated circuits (e.g. multiple silicon chips including several memory chips and one or

more controller chips), but in rare some cases may only contain one chip. Both integrated circuit memories and integrated memory systems were well known in 1992 when the application to which the '990 patent claims priority was filed, and I personally worked on the development of both integrated circuit memories and integrated memory systems.

28. Only dependent claims 6 and 14 include an "integrated circuit" limitation. None of the claims associated with independent claim 20 recite an integrated circuit. Rather, claim 20 refers to an "integrated memory." The use of the term "integrated memory" at the beginning of claim 20 does not add structure to the claimed memory. The term "integrated memory" is simply a description of what is formed by the combination of the elements (e.g. the registers and decoders) recited in the body of the claim.

29. The term "integrated memory" had a well-known meaning to persons involved in the design and implementation of memory circuits at the time the patent was filed. Integrated memories commonly consisted of a memory controller chip(s) which controlled multiple memory circuits. For example, in the 1990s, Intel developed integrated circuit flash memory devices such as the 28F010 (a flash 1M bit single chip memory) but also developed integrated memory products which incorporated multiple integrated circuits. One example of such an integrated memory is the Intel iMC001FLKA Flash Memory Card, a 1M byte flash memory system contained in a memory card. This card includes eight 28F010 integrated circuits memories along with two support integrated circuits as can be seen below in Figure 2 of the iMC001FLKA datasheet. Attached to my declaration are the 28F010 datasheet (Exhibit C), the iMC001FLKA datasheet (Exhibit E), and an Octoboer 1990 press release (Exhibit D).

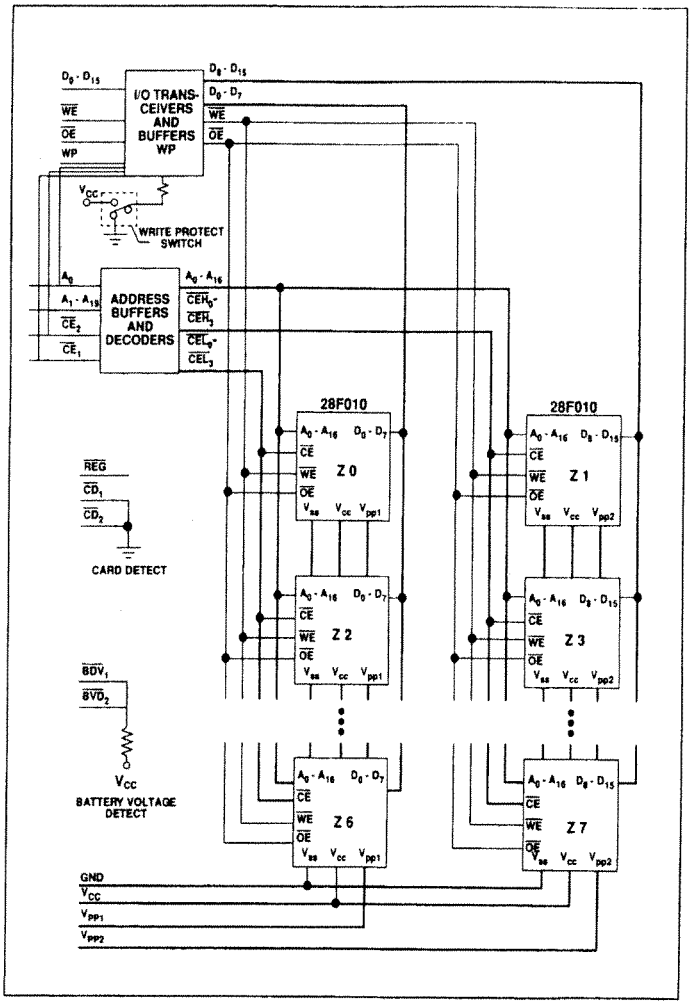
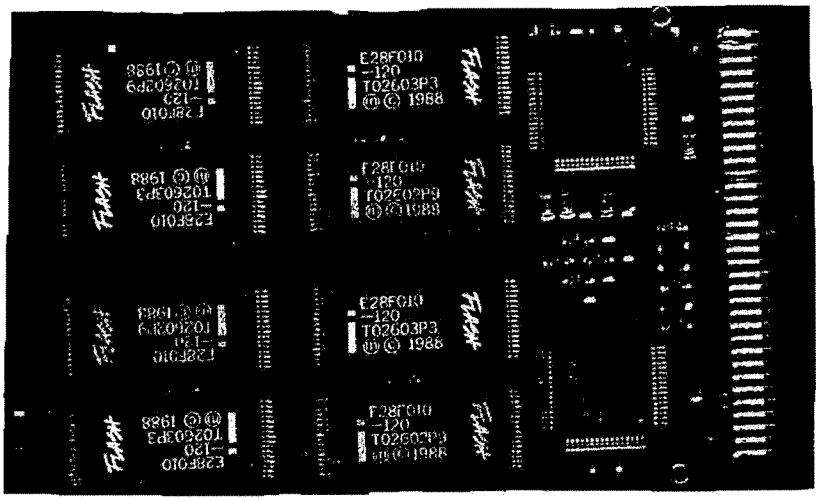


Figure 2. iMC001FLKA Block Diagram

30. In addition, these multiple integrated circuits can clearly be distinguished in the photograph of the printed circuit board contained inside the iMC001FLKA memory card shown below and attached as Exhibit F.



31. In the opening line of the Intel iMC001FLKA datasheet it clearly states that "Intel's Flash Memory Card is the integrated memory solution for portable PCs." As I have shown, this memory card contains more than one integrated circuit, so the term "integrated memory" cannot mean that this memory card is composed of a single integrated circuit as Dr. Wolfe attests.

32. In addition, page 30 of an article entitled "Card Physical" in the May/June issue of the Memory Card Systems & Design magazine refers to a memory card as "the JEIDA IC memory card." JEIDA is the Japanese Electronics Industry Development Association that is responsible for establishing standards for the memory card. *See* Exhibit H. On page 31 of this article, it clearly discusses multiple IC memory devices fitting into the memory card. So in this case, the use of the term IC memory card does not mean that a memory card contains only a single integrated circuit. Also on pages 32 and 33 of this article, there is an Intel advertisement for the Intel 4M byte memory card (iMC004FLKA), that clearly shows the benefits of an "integrated memory" containing all the components of a distributed memory system in a single apparatus. The iMC004FLKA was a 4-megabyte "integrated memory" consisting of 16 integrated circuit memories along with support integrated memories. *See* Exhibit G.

33. Patents filed contemporaneously with the '990 Patent, including U.S. Patent No. 5,502,667, also evidence the prevalence of multi-chip integrated circuits in the early 1990s. *See* Exhibit I.

34. In summary, the term "integrated memory" simply refers to a single memory apparatus that incorporates one or more integrated circuits. The iMC001FLKA memory card is an example of an integrated memory that contains multiple integrated circuits. An integrated memory as understood by a person of ordinary skill in the art at the time the patent was filed was a memory apparatus containing one or more integrated circuits.

"the locations L1 and L2 in the sequence of consecutive addresses," "consecutively addressed memory locations L1, ... Ln," and "the memory locations ... have consecutive addresses"

35. Each of the asserted claims of the '990 patent associate an address with a memory location. The claims require that the memory locations have consecutive addresses. Consecutive addresses are addresses that follow one after the other in order.

36. The '990 patent uses the term memory location synonymously with memory cell. ['990 patent, Col. 1:10-11 (describing "1-bit memory locations (or 'cells'))"]. Hence, in the '990 patent, a memory cell is the physical object that holds one bit of memory. I agree with Dr. Wolfe that "[i]n the context of this patent, a cell is only one bit of memory." [Wolfe Decl. ¶ 36] Thus, the relationship between the consecutive addresses and the memory locations can be described as a set of addresses following one after the other in order from L1 to Ln wherein each memory location represents a memory cell that is associated with a single address.

37. AMD disagrees with this description based on the embodiment of Figure 5 showing multiple memory cells that form part of the same memory location. The above description is not intended to eliminate the possibility of multiple memory cells associated with the same address forming a single memory location as would occur in a byte or word-wide memory device. The claim construction can be modified slightly to alleviate AMD's concern to state "a set of addresses following one after the other in order from L1 to Ln where each memory location represents a memory cell or cells associated with a single address." But even with this modification, a memory cell would still only contain a single bit of data.

"the sense amplifiers from which the contents of said location L1 are being transferred are enabled and the sense amplifiers to which the contents of said location L2 are disabled" (claim 3)

"a control circuit for selectively enabling said sense amplifier circuits so that said control circuit enables a sense amplifier circuit whose output signals are being transferred to the output of said memory but said control circuit does not enable all said sense amplifier circuits at the same time" (claim 8)

"the control circuit enables the sense amplifier circuit selected to provide data to the memory output and at the same time disables one or more sense amplifier circuits not selected to provide data to the memory output" (claim 23)

38. Sense amplifiers are well-known circuits in the art of memory design. A sense amplifier is commonly used in memory circuits to receive a signal representing information from selected memory cell and amplify that information. In the '990 patent, the amplified signal from the sense amplifier is provided to the memory output.

39. The '990 patent discloses a power-saving technique achieved by enabling only certain sense amplifiers. Enabling a sense amplifier turns on the sense amplifier and allows the input signal to be amplified and placed on the sense amplifier output. When a sense amplifier is disabled it is turned off (saving power) and the input signal is not amplified and placed on the output of the sense amplifier. The '990 Patent discloses a control circuit to enable and disable the sense amplifiers as follows:

> Control-multiplexer circuit 334 of memory 310 provides enable signals to sense amplifier circuits 330.L-0 through 330.L-3 and 330.R-0 through 330.R-3 on busses 350.L and 350.R to enable only the sense amplifier circuit being read and thus to reduce power consumption. In some embodiments, control-multiplexer circuit 334 enables, in addition to the sense amplifier circuit being read, a certain number of sense amplifier circuits to be read immediately after, so as to allow those sense amplifier circuits sufficient time to develop their output signals. ['990 patent, Col. 5:45-54]

40. Dr. Wolfe expresses his opinion that "[n]either claims 3, 8 nor 23 indicate that each sense amplifier must be disabled when data is being transferred from a memory location to the sense amplifier." [Wolfe Decl. at paragraph 40] The passage he cites from the April 27, 1995 Amendment, however, contradicts his opinion:

> Claim 4 [issued claim 3] dependent from Claim 2 further distinguishes from Pinkham and Rao, taken singularly or together, by reciting that when the contents of a location L1 are being transferred in burst mode from one or more sense amplifiers

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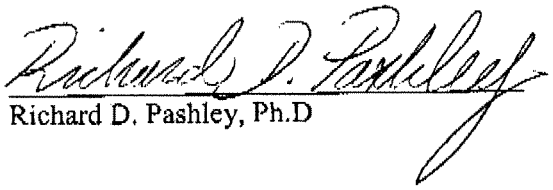
> to the memory output and the contents of another location L2 are being transferred from L2 to one or more sense amplifiers, *the sense amplifiers **from which** the contents of L1 are being transferred **are enabled*** and *the sense amplifiers **to which** the contents of L2 are being transferred **are disabled***, but these latter sense amplifiers become enabled subsequently for amplifying the contents of L2. [04/27/1995 Amendment at 5 (emphasis added)]

41. Dr. Wolfe also opines that the normal operation of a sense amplifier is that it need not be enabled to develop a signal on its output for the entire duration of time when data is being transferred from the sense amplifier output to the memory output. Contrary to Dr. Wolfe's opinion, in the context of the '990 patent, the sense amplifier must be enabled for the entire duration of time when data is being transferred from the sense amplifier output to the memory output. If the sense amplifier was disabled (e.g. allowed to have its output signals go to an indeterminate state), the memory output would also go to an indeterminate state. Since there is only a simple MUX pass transistor ('990 Col. 7, Lines 33-36) between the sense amplifier and the memory output that selects the desired sense amplifier to transfer its output signal to the memory output, any change in the sense amplifier's output state would immediately be passed through to the memory output. In other words, if the sense amplifier is disabled during this transfer, inaccurate data may be provided to the output. Hence, the sense amplifier would have to be enabled during the entire time that the sense amplifier is transferring data to the memory output.

I declare under penalty of perjury that the foregoing is true and correct. Executed this 30th day of March, 2009, in Granite Bay, California.



Richard D. Pashley, Ph.D