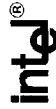


EXHIBIT G



ADVANCE INFORMATION

IMC004FLKA 4-MEGABYTE FLASH MEMORY CARD



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- Inherent Nonvolatility (Zero Retention Power)
 - No Batteries Required for Back-up
 - Over 1,000,000 Hours MTBF
 - More Reliable than Disk
- High-Performance Read
 - 250 ns Maximum Access Time
 - CMOS Low Power Consumption
 - 40 mA Typical Active Current (X8)
 - 800 μ A Typical Standby Current
- Flash Electrical Zone-Erase
 - 2 Seconds Typical per 256 K-Byte Zone
 - Multiple Zone-Erase
- Random Writes to Erased Zones
 - 10 μ s Typical Byte Write
- Write Protect Switch to Prevent Accidental Data Loss
- Command Register Architecture for Microprocessor/Microcontroller Compatible Write Interface
- ETOX™ II Flash Memory Technology
 - 5V Read, 12V Erase/Write
 - High-Volume Manufacturing Experience
- PCMCIA/JEIDA 68-Pin Standard
 - Byte- or Word-wide Selectable
- Independent Software & Hardware Vendor Support
 - Integrated System Solution Using Flash Filing Systems

Intel's Flash Memory Card is the integrated memory solution for portable PCs. The IMC004FLKA enables OEM system manufacturers to design portable PCs that no longer require rotating electro-mechanical media to store application code and data files. This allows the design and manufacture of PCs that are higher performance, more rugged, consume less battery power, and weigh much less than traditional disk-based portable PCs. The flash memory card supports the emerging "Mobile Office" by allowing the user to transport both application code and data files between desktop PCs and portables.

The IMC004FLKA conforms to the PCMCIA/JEIDA international standard, providing standardization at the hardware and data interchange level. OEMs may opt to write the Card Information Structure (CIS) at the memory card's address 00000H with a format utility. This information provides data interchange functional capability. The 250 nanosecond access time allows for "execute-in-place" capability, for popular low-power microprocessors. Intel's 4-Megabyte Flash Memory Card operates in a byte-wide and word-wide configuration providing performance/power options for different systems.

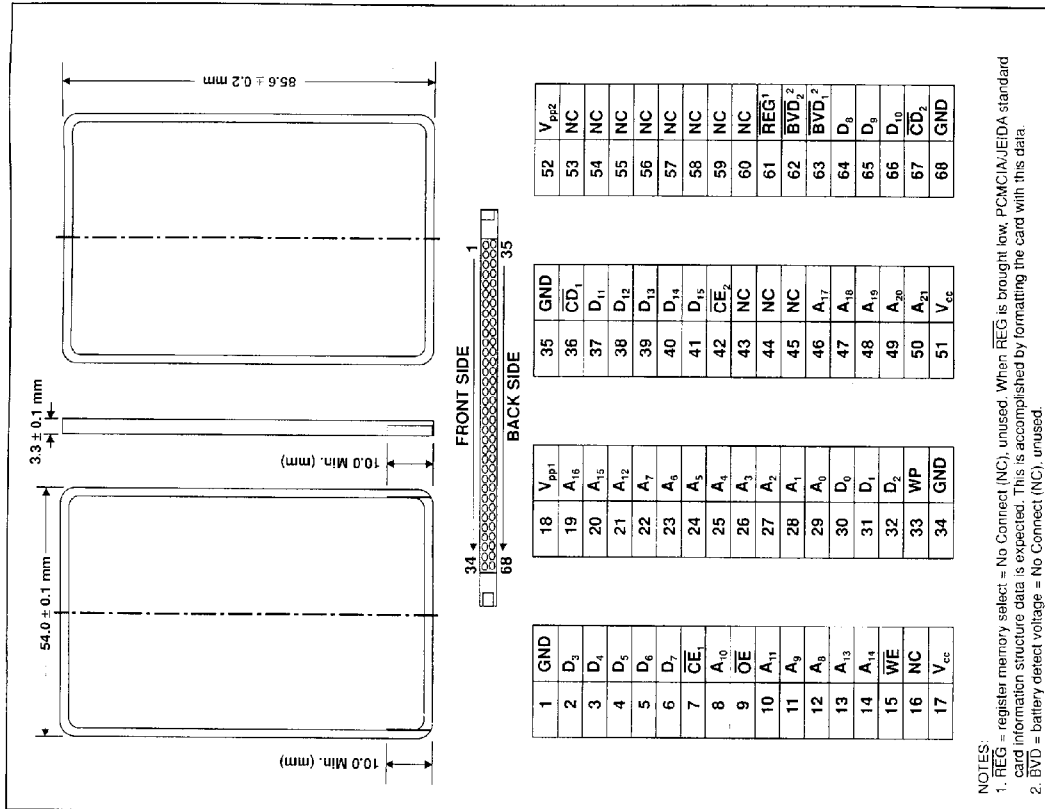
Intel's Flash Memory card employs Intel's ETOX II Flash Memories. Filing systems, such as Microsoft's Flash File System (FFS), facilitate sequential data file storage and card erasure using a purely nonvolatile medium. Flash filing systems, coupled with the Intel Flash Memory Card, effectively create an all-silicon nonvolatile read/write random access memory system that is more reliable and higher performance than disk-based memory systems.

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Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel product. No other circuit patent licenses are implied. Information contained herein supersedes previously published specifications on these devices from Intel. October, 1990
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MEMORY PRODUCTS

SAMAMD0325696



NOTES:
 1. REG = register memory select = No Connect (NC), unused. When \overline{REG} is brought low, PCMCIA/JEIDA standard card information structure data is expected. This is accomplished by formatting the card with this data.
 2. \overline{BVD} = battery detect voltage = No Connect (NC), unused.

Figure 1. iMC004FLKA Pin Configurations

Table 1. Pin Description

Symbol	Type	Name and Function
A ₀ -A ₂₁	INPUT	ADDRESS INPUTS for memory locations. Addresses are internally latched during a write cycle.
D ₀ -D ₁₅	INPUT/ OUTPUT	DATA INPUT/OUTPUT: inputs data during memory write cycles; outputs data during memory read cycles. The data pins are active high and float to tri-state OFF when the card is deselected or the outputs are disabled. Data is internally latched during a write cycle.
\overline{CE}_1 , \overline{CE}_2	INPUT	CARD ENABLE: activates the card's high and low byte control logic, input buffers, zone decoders, and associated memory devices. \overline{CE} is active low; \overline{CE} high deselects the memory card and reduces power consumption to standby levels.
\overline{OE}	INPUT	OUTPUT ENABLE: gates the cards output through the data buffers during a read cycle. \overline{OE} is active low.
WE	INPUT	WRITE ENABLE controls writes to the control register and the array. Write enable is active low. Addresses are latched on the falling edge and data is latched on the rising edge of the \overline{WE} pulse. Note: With V _{pp} ≤ 6.5V, memory contents cannot be altered.
V _{pp1} , V _{pp2}		ERASE/WRITE POWER SUPPLY for writing the command register, erasing the entire array, or writing bytes in the array.
V _{CC}		DEVICE POWER SUPPLY (5V ± 5%).
GND		GROUND
\overline{CD}_1 , \overline{CD}_2	OUTPUT	CARD DETECT. The card is detected at $\overline{CD}_{1,2}$ = ground.
WP	OUTPUT	WRITE PROTECT. All write operations are disabled with WP = active high.
NC		NO INTERNAL CONNECTION to device. Pin may be driven or left floating.
\overline{BVD}_1 , \overline{BVD}_2	OUTPUT	BATTERY VOLTAGE DETECT. NOT REQUIRED.

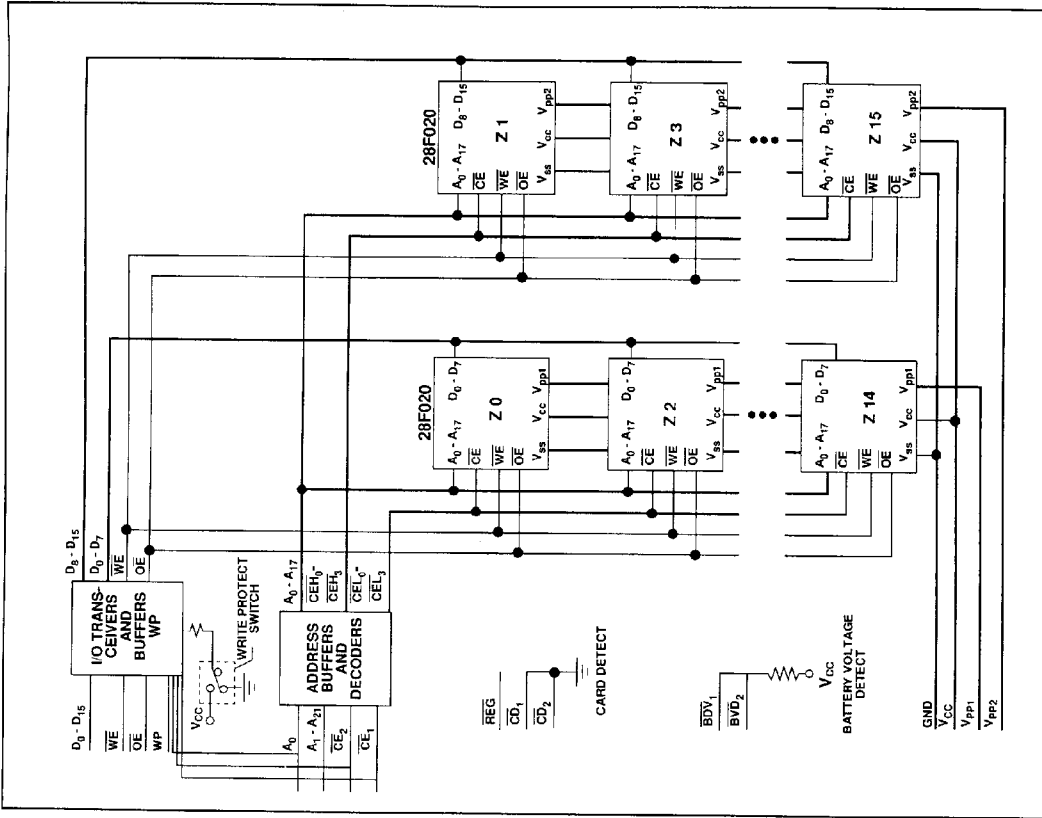


Figure 2. IMC004FLKA Block Diagram

APPLICATIONS

The IMC004FLKA Flash Memory Card allows for the storage of data files and application programs on a purely solid-state removable medium. System resident flash filing systems, such as Microsoft's Flash File System, allow Intel's ETOS II highly reliable Flash Memory Card to effectively function as a physical disk drive. The Intel Flash Memory Card in conjunction with flash filing systems provides an innovative alternative to both fixed hard disks and floppy disks in DOS-compatible portable PCs.

User application software stored on the flash memory card substantially reduces the slow disk-DRAM download process. Replacing the disk results in a dramatic enhancement of read performance and substantial reduction of active power consumption, size, and weight — considerations particularly important in portable PCs and equipment. The IMC004FLKA's high performance read access time and command register microprocessor write interface allows for use of the flash memory system in an "execute-in-place" architecture. This configuration eliminates the need for the redundancy associated with DRAM and Disk memory system architectures. ROM based operating systems, such as Microsoft's MS-DOS ROM Version allow for "instant-on" capability. This enables the design of PCs that boot, operate, store data files, and execute application code from/to purely nonvolatile memory.

Flash write performance is often 50% higher than hard disks for typical user file storage. This equates to ten times more performance when compared to "spun-down" disks, the common practice for portable machines.

Flash filing systems enable the storage and modification of data files by allocating flash memory space intelligently, thus minimizing the number of rewrite cycles. This management function allows the user to rewrite reliably to the flash memory card many more times than a fixed or floppy disk which concentrate rewrite operations into small fixed portions of the medium.

Flash filing systems implement Intel's Flash Memory Card as a redirected disk drive; similar to structures used in local area networks. This enables the end user to interact with the flash memory card in precisely the same way as a magnetic disk. Filing systems that run under popular operating systems, such as MS-DOS, can use the installed base of application software.

The Microsoft Flash File System enables the storage and modification of data files by utilizing a linked list directory structure that is evenly distributed along with the data across the memory card. The linked list approach minimizes file fragmentation losses by using variable-sized data structures rather than the standard sector/cluster method of disk-based systems.

The integration of the PCMCIA/JEIDA 68-pin interface with flash filing systems enables the end-user to transport user files and application code between portable PCs and desktop PCs with memory card Reader/Writers. Intel Flash PC cards provide durable nonvolatile memory storage for Notebook PCs on the road, facilitating simple transfer back into the desktop environment.

For systems currently using a static RAM; battery configuration for data acquisition, the IMC004FLKA's inherent nonvolatility eliminates the need for battery backup. The concern for battery failure no longer exists, an important consideration for portable computers and medical instruments, both requiring continuous operation. The IMC004FLKA consumes no power when the system is off. In addition, the IMC004FLKA offers a considerable cost and density advantage over memory cards based on static RAM with battery backup.

The flash memory card's electrical zone-erase, byte writability, and complete nonvolatility fit well with data accumulation and recording needs. Electrical zone-erase gives the designer the flexibility to selectively rewrite zones of data while saving other zones for infrequently updated look-up tables.

PRINCIPLES OF OPERATION

Intel's Flash Memory Card combines the functionality of two mainstream memory technologies: the rewritability of RAM and the nonvolatility of EPROM. The flash memory card consists of an array of individual memory devices, each of which defines a physical zone. The IMC004FLKA's memory devices erase as individual blocks, equivalent in size to the 256 K-Byte zone. Multiple zones can be erased simultaneously provided sufficient current for the appropriate number of zones (memory devices). Note, multiple zone erasure requires higher current from both the V_{PP} and V_{CC} power supplies. Erased zones can then be written in bit- or byte-at-a-time fashion and read randomly like RAM. Bit level write capability also supports disk emulation.

In the absence of high voltage on the $V_{PP1,2}$ pins, the IMC004FLKA remains in the read-only mode. Manipulation of the external memory card-control pins yields the standard read, standby, and output disable operations.

The same read, standby, and output disable operations are available when high voltage is applied to the $V_{PP1,2}$ pins. In addition, high voltage on $V_{PP1,2}$ enables erasure and rewriting of the accessed zone(s). All functions associated with altering zone contents — erase, erase verify, write, and write verify — are accessed via the command register.

Commands are written to the internal memory register(s), decoded by zone size, using standard microprocessor write timings. Register contents for a given zone serve as input to that zone's internal state-machine which controls the erase and rewrite circuitry. Write cycles also internally latch addresses and data needed for write and erase operations. With the appropriate command written to the register(s), standard microprocessor read timings output zone data, or output data for erase and write verification.

Byte-wide or Word-wide Selection

The flash memory card can be read, erased, and written in a byte-wide or word-wide mode. In the word-wide configuration V_{PP1} and/or CE_1 control the LO-Byte (with $A_0 = 0$) while V_{PP2} and CE_2 control the HI-Byte ($A_0 = \text{don't care}$).

Read, Write, and Verify operations are byte- or word-oriented, thus zone independent. Erase Setup and Begin Erase Commands are zone dependent such that commands written to any address within a 256 K-Byte zone boundary initiate the erase

operation in that zone for two 256 K-Byte zones under word-wide operation).

Conventional x8 operation uses \overline{CE} , active-low, with CE_2 high, to read or write data through the D_7 , D_0 , only. "Even bytes" are accessed when A_0 is low, corresponding to the low byte of the complete x16 word. When A_0 is high, the "odd byte" is accessed by transposing the high byte of the complete x16 word onto the D_0 - D_7 outputs. This odd byte corresponds to data presented on D_8 - D_{15} pins in x16 mode.

Note that two zones logically adjacent in x16 mode are multiplexed through D_0 - D_7 in x8 mode and are toggled by the A_0 address. Thus, zone specific erase operations must be kept discrete in x8 mode by addressing even bytes only for one-half of the zone pair, then addressing odd bytes only for the other half.

Card Detection

The flash memory card features two card detect pins ($CD_{1,2}$) that allow the host system to determine if the card is properly loaded. Note that the two pins are located at opposite ends of the card. Each CD output should be read through a port bit. Should only one of the two bits show the card to be present, then the system should instruct the user to re-insert the card squarely into the socket. Card detection can also tell the system whether or not to redirect drives in the case of system booting. $CD_{1,2}$ is active low, internally tied to ground.

Write Protection

The flash memory card features three types of write protection. The first type features a mechanical Write Protect Switch that disables the circuitry that control Write Enable to the flash devices. When the switch is activated, \overline{WE} is forced high, which disables any writes to the Command Register. The second type of write protection is based on the PCMCIA/JEIDA socket. Unique pin length assignments provide protective power supply sequencing during hot insertion and removal. The third type operates via software control through the Command Register when the card resides in its connector. The Command Register of each zone is only active when $V_{PP1,2}$ is at high voltage. Depending upon the application, the system designer may choose to make $V_{PP1,2}$ power supply switchable — available only when writes are desired. When $V_{PP1,2} = V_{PPn}$, the contents of the register default to the read command, making the IMC004FLKA a read-only memory card. In this mode, the memory contents cannot be altered.

Intelligent Identifier™ Command

The manufacturer and device codes can be read via the Command Register for instances where the IMC004FLKA is erased and rewritten in a universal reader/writer. Following a write of 90H to a zone's Command Register, a read from address location 00000H on any zone outputs the manufacturer code (89H). A read from address 00020H outputs the memory device code (BDH).

Write

Zone erasure and rewriting are accomplished via the Command Register, when high voltage is applied to $V_{PP1,2}$. The contents of the register serve as input to that zone's internal state-machine. The state-machine outputs dictate the function of the targeted zone.

The Command Register itself does not occupy an addressable memory location. The register is a latch used to store the command, along with address and data information needed to execute the command.

The Command Register is written by bringing Write Enable to a logic-low level (V_{IL}), while Card Enable(s) is/are low. Addresses are latched on the falling edge of Write Enable, while data is latched on the rising edge of the Write Enable pulse. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Write Waveforms for specific timing parameters.

COMMAND DEFINITIONS

When low voltage is applied to the V_{PP} pin(s), the contents of the zone Command Register(s) default to 00H, enabling read-only operations.

Placing high voltage on the V_{PP} pin(s) enable(s) read/write operations. Zone operations are selected by writing specific data patterns into the Command Register. Tables 3 and 4 define these IMC004FLKA register commands for both byte-wide and word-wide configurations.

The system designer may choose to leave $V_{PP1,2} = V_{PPn}$, making the high voltage supply constantly available. In this case, all Command Register functions are inhibited whenever V_{CC} is below the write lockout voltage, V_{LKO} . (See the section on Power Up/Down Protection.) The IMC004FLKA is designed to accommodate either design practice, and to encourage optimization of the processor-memory card interface.

BUS OPERATIONS

Read

The IMC004FLKA has two control functions, both of which must be logically active, to obtain data at the outputs: Card Enable (\overline{CE}) is the power control and should be used for high and/or low zone(s) selection. Output Enable (\overline{OE}) is the output control and should be used to gate data from the output pins, independent of accessed zone selection. In the byte-wide configuration, only one \overline{CE} is required. The word-wide configuration requires both \overline{CE} s active low.

When $V_{PP1,2}$ is high (V_{PH}), the read operations can be used to access zone data and to access data for write/erase verification. When $V_{PP1,2}$ is low (V_{PL}), only read accesses to the zone data are allowed.

Output Disable

With Output Enable at a logic-high level (V_{IH}), output from the card is disabled. Output pins are placed in a high-impedance state.

Standby

With one Card Enable at a logic-high level, the standby operation disables one-half of the x16 output's read/write buffer. Further, only the zone corresponding to the selected address within the upper or lower \overline{CE}_n bank is active at a time. (NOTE: A_0 must be low to select the low half of the x16 word when $\overline{CE}_2 = 1$ and $\overline{CE}_1 = 0$.) All other zones are deselected, substantially reducing card power consumption. For deselected banks, the outputs are placed in a high-impedance state, independent of the Output Enable signal. If the IMC004FLKA is deselected during erasure, writing, or write/erase verification, the accessed zone draws active current until the operation is terminated.

Table 2. Bus Operations

Pins	Notes	[1, 7]		A0	CE ₂	CE ₁	OE	WE	D ₀ -D ₁₅	D ₀ -D ₇
		V _{PP2}	V _{PP1}							
Read (x8)	8	V _{PPL}	V _{PH}	V _L	V _H	V _L	V _L	V _H	Tri-state	Data Out-Even
Read (x8)	9	V _{PPL}	V _{PH}	V _L	V _H	V _L	V _L	V _H	Tri-state	Data Out-Odd
Read (x8)	10	V _{PPL}	V _{PH}	X	V _L	V _H	V _L	V _H	Data Out	Tri-state
Read (x16)	11	V _{PPL}	V _{PH}	X	V _L	V _L	V _L	V _H	Data Out	Data Out
Output Disable		V _{PP}	V _{PH}	X	X	X	V _H	V _H	Tri-state	Tri-state
Standby		V _{PPL}	V _{PH}	X	V _H	V _H	X	X	Tri-state	Tri-state
Read (x8)	3, 8	V _{PPX}	V _{PH}	V _L	V _H	V _L	V _L	V _H	Tri-state	Data Out-Even
Read (x8)	3, 9	V _{PPX}	V _{PH}	V _H	V _L	V _L	V _L	V _H	Tri-state	Data Out-Odd
Read (x8)	10	V _{PPH}	V _{PH}	X	V _L	V _H	V _L	V _H	Data Out	Tri-state
Read (x16)	3, 11	V _{PPH}	V _{PH}	X	V _L	V _L	V _L	V _H	Data Out	Data Out
Write (x8)	5, 8	V _{PPX}	V _{PH}	V _L	V _H	V _L	V _H	V _L	Tri-state	Data In-Even
Write (x8)	9	V _{PPH}	V _{PH}	V _H	V _L	V _L	V _H	V _L	Tri-state	Data In-Odd
Write (x8)	10	V _{PPH}	V _{PH}	X	V _L	V _H	V _H	V _L	Data In	Tri-state
Write (x16)	11	V _{PPH}	V _{PH}	X	V _L	V _L	V _L	V _H	Data In	Data In
Standby	4	V _{PPH}	V _{PH}	X	V _H	V _H	X	X	Tri-state	Tri-state
Output Disable		V _{PPH}	V _{PH}	X	X	X	V _H	V _L	Tri-state	Tri-state

Notes:

1. Refer to DC Characteristics. When V_{PP1/2} = V_{PPX}, memory contents can be read but not written or erased.
2. Manufacturer and device codes may be accessed via a command register write sequence. Refer to Table 3. All other addresses low.
3. Read operations with V_{PP1/2} = V_{PPX} may access array data or the intelligent identifier codes.
4. With V_{PP1/2} at high voltage, the standby current equals I_{CC} + I_{PP} (standby).
5. Refer to Table 3 for valid Data-In during a write operation.
6. X can be V_L or V_H.
7. V_{PPX} = V_{PPH} or V_{PPL}.
8. This x8 operation reads or writes the low byte of the x16 word on DQ_{0,7}, i.e., A₀ low reads "even" byte in x8 mode, "odd" byte in x8 mode.
9. This x8 operation reads or writes the high byte of the x16 word on DQ_{8,15} (transposed from DQ_{0,7}), i.e., A₀ high reads "odd" byte in x8 mode.
10. This x8 operation reads or writes the high byte of the x16 on DQ_{8,15}. A₀ is "don't care."
11. A₂ is "don't care", unused in x16 mode. High and low bytes are presented simultaneously.

Table 3. Command Definitions byte-wide mode

Command	Notes	Bus Cycles Req'd			First Bus Cycle			Second Bus Cycle		
		Operation ⁽¹⁾	Address ⁽²⁾	Data ⁽³⁾	Operation ⁽¹⁾	Address ⁽²⁾	Data ⁽³⁾	Operation ⁽¹⁾	Address ⁽²⁾	Data ⁽³⁾
Read Memory		1	Write	X	00H					
Read Intelligent ID Codes	4	3	Write	IA	90H		Read			
Set-up Erase/Erase	5	2	Write	ZA	20H		Write	ZA	EA	20H
Erase Verify	5	2	Write	EA	A0H		Read	EA	EA	EVD
Set-up Write/Write	6	2	Write	WA	40H		Write	WA	WA	WD
Write Verify	6	2	Write	WA	C0H		Read	WA	WA	WVD
Reset	7	2	Write	X	FFH		Write	X	X	FFFH

Table 4. Command Definitions word-wide mode

Command	Notes	Bus Cycles Req'd			First Bus Cycle			Second Bus Cycle		
		Operation ⁽¹⁾	Address ⁽²⁾	Data ⁽³⁾	Operation ⁽¹⁾	Address ⁽²⁾	Data ⁽³⁾	Operation ⁽¹⁾	Address ⁽²⁾	Data ⁽³⁾
Read Memory		1	Write	X	0000H					
Read Intelligent ID Codes	4	3	Write	IA	9090H		Read			
Set-up Erase/Erase	5	2	Write	ZA	2020H		Write	ZA	ZA	2020H
Erase Verify	5	2	Write	EA	A0A0H		Read	EA	EA	EVD
Set-up Write/Write	6	2	Write	WA	4040H		Write	WA	WA	WD
Write Verify	6	2	Write	WA	C0C0H		Read	WA	WA	WVD
Reset	7	2	Write	X	FFFFH		Write	X	X	FFFFH

Notes:

1. Bus operations are defined in Table 2.
2. IA = Identifier address: 00H for manufacturer code, 01H for device code.
EA = Address of memory location to be read during erase verify.
ZA = Address of memory location to be written.
EA = Address of 256 K-Byte zones involved in erase operation.
Addresses are latched on the falling edge of the Write Enable pulse.
3. ID = Data read from location IA during device identification. (Mfr = 88H, Device = BDH).
EVD = Data read from location EA during erase verify.
WD = Data to be written at location WA. Data is latched on the rising edge of Write Enable.
WVD = Data read from location WA during write verify. WA is latched on the Write command.
4. Following the Read Intelligent ID command, two read operations access manufacturer and device codes.
5. Figure 5 illustrates the Erase Algorithm.
6. Figure 6 illustrates the Write Algorithm.
7. The second bus cycle must be followed by the desired command register write.

Read Command

While $V_{PP1,2}$ is high, for erasure and writing, zone memory contents can be accessed via the read command. The read operation is initiated by writing 00H (0000H for word-wide configuration) into the zone Command Register(s). Microprocessor read cycles retrieve zone data. The accessed zone remains enabled for reads until the Command Register(s) contents are altered.

The default contents of each zone's register(s) upon $V_{PP1,2}$ power-up is 00H (00000H for word-wide). This default value ensures that no spurious alteration of memory card contents occurs during the $V_{PP1,2}$ power transition. Where the $V_{PP1,2}$ supply is left at V_{PPH} , the memory card powers-up and remains enabled for reads until the command Register contents of targeted zones are changed. Refer to the AC Read Characteristics and Waveforms for specific timing parameters.

Intelligent Identifier Command

Each zone of the IMC004FLKA contains an intelligent identifier to identify memory card device characteristics. The operation is initiated by writing 90H (9090H for word-wide) into the Command Register(s). Following the command write, a read cycle from address 00000H retrieves the manufacturer code 89H (8989H for word-wide). A read cycle from address 0002H returns the device code BDH (BD0DH for word-wide). To terminate the operation, it is necessary to write another valid command into the register(s).

Set-up Erase/Erasure Commands

Set-up Erase is a command-only operation that stages the targeted zone(s) for electrical erasure of all bytes in the zone. The set-up erase operation is performed by writing 20H to the Command Register (2020H for word-wide).

To commence zone-erasure, the erase command (20H or 2020H) must again be written to the register(s). The erase operation begins with the rising edge of the Write-Enable pulse and terminates with the rising edge of the next Write-Enable pulse (i.e., Erase-Verify Command).

This two-step sequence of set-up followed by execution ensures that zone memory contents are not accidentally erased. Also, zone-erasure can only occur when high voltage is applied to the $V_{PP1,2}$ pins. In the absence of this high voltage, zone memory contents are protected against erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Erase-Verify Command

The erase command erases all of the bytes of the zone in parallel. After each erase operation, all bytes in the zone must be individually verified. In byte-mode operations, zones are segregated by A_0 in odd and even banks; erase and erase verify operations must be done in complete passes of even-bytes-only then odd-bytes-only. See the Erase Algorithm for byte-wide mode. The erase verify operation is initiated by writing A0H (A0A0H for word-wide) into the Command Register(s). The address for the byte(s) to be verified must be supplied as it is latched on the falling edge of the Write Enable pulse. The register write terminates the erase operation with the rising edge of its Write Enable pulse.

The enabled zone applies an internally-generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are erased. Similarly, reading FFFFH from the addressed word indicates that all bits in the word are erased.

The erase-verify command must be written to the Command Register prior to each byte (word) verification to latch its address. The process continues for each byte (word) in the zone(s) until a byte (word) does not return FFH (FFFFH) data, or the last address is accessed.

In the case where the data read is not FFH (FFFFH), another erase operation is performed. (Refer to Set-up Erase/Erasure.) Verification then resumes from the address of the last-verified byte (word). Once all bytes (words) in the zone(s) have been verified, the erase step is complete. The accessed zone can now be written. At this point, the verify operation is terminated by writing a valid command (e.g., Write Set-up to the Command Register). The Erase algorithms for byte-wide and word-wide configurations illustrate how commands and bus operations are combined to perform electrical erasure of the IMC004FLKA. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Set-up Write/Write Commands

Set-up write is a command-only operation that stages the targeted zone for byte writing. Writing 40H (4040H) into the Command Register(s) performs the set-up operation.

Once the write set-up operation is performed, the next Write Enable pulse causes a transition to an active write operation. Addresses are internally latched on the falling edge of the Write Enable pulse. Data is internally latched on the rising edge of the Write Enable pulse. The rising edge of Write Enable also begins the write operation. The write operation terminates with the next rising edge of Write Enable, which is used to write the verify command. Refer to AC Write Characteristics and Waveforms for specific timing parameters.

Write Verify Command

The IMC004FLKA is written on a byte-by-byte or word-by-word basis. Byte or word writing may occur sequentially or at random. Following each write operation, the byte or word just written must be verified.

The write-verify operation is initiated by writing C0H (C0C0) into the Command Register(s). The register write(s) terminates the write operation with the rising edge of its Write Enable pulse. The write-verify operation stages the accessed zone(s) for verification of the byte or word last written. No new address information is latched. The zone(s) apply(ies) an internally-generated margin voltage to the byte

or word. A microprocessor read cycle outputs the data. A successful comparison between the written byte or word and true data means that the byte or word is successfully written. The write operation then proceeds to the next desired byte or word location. The Write algorithms for byte-wide and word-wide configurations illustrate how commands are combined with bus operations to perform byte and word writes. Refer to AC Write Characteristics and Waveforms for specific timing parameters.

Reset Command

A reset command is provided as a means to safely abort the erase- or write-command sequences. Following either set-up command (erase or write) with two consecutive writes of FFH (FFFFH for word-wide) will safely abort the operation. Zone memory contents will not be altered. A valid command must then be written to place the accessed zone in the desired state.

EXTENDED ERASE/WRITE CYCLING

Intel has designed extended cycling capability into its ETOX II flash memory technology enabling a flash memory card with a MTBF that is approximately 20 times more reliable than rotating disk technology. Resulting improvements in cycling reliability come without increasing memory cell size or complexity. First, an advanced tunnel oxide increases the charge carrying ability ten-fold. Second, the oxide area per cell subjected to the tunneling electric field minimizes the probability of oxide defects in the region. The lower electric field greatly reduces oxide stress and the probability of failure.

WRITE ALGORITHMS

The write algorithm(s) use write operations of 10 μ s duration. Each operation is followed by a byte or word verification to determine when the addressed byte or word has been successfully written. The algorithm(s) allows for up to 25 write operations per byte or word, although most bytes and words verify on the first or second operation. The entire sequence of writing and byte/word verification is performed with V_{PP} at high voltage.

ERASE ALGORITHM

The Erase algorithm(s) yield(s) fast and reliable electrical erasure of memory contents. The algorithm employs a closed-loop flow, similar to the write algorithm, to simultaneously remove charge from all bits in the accessed zone(s).

Erase begins with a read of memory zone contents. Reading FFH (FFFFH) data from the accessed zone(s) can be immediately followed by writing to the desired zone(s).

For zones being erased and rewritten, uniform and reliable erasure is ensured by first writing all bits in the accessed zone to their charged state (data = 00H by byte-wide, 00000H word-wide). This is accomplished, using the write algorithm, in approximately four seconds per zone.

Erase execution then continues with an initial erase operation. Erase verification (data = FFH byte-wide, FFFFH word-wide) begins at address 00000H and continues through the zone to the last address, or until data other than FFH (FFFFH) is encountered. (Note: byte-wide erase operation requires separate even- and odd-address passes to handle the individual 256 K-Byte zones.) With each erase operation, an increasing number of bytes or words verify to the erased state. Erase efficiency may be improved by storing the address of the last byte or word verified in a register(s). Following the next erase operation, verification starts at that stored address location. Follow this procedure until all bytes in the zone are erased. Then, re-start the procedure for the next zone or word-wide zone pair. Erasure typically occurs in two seconds per zone.

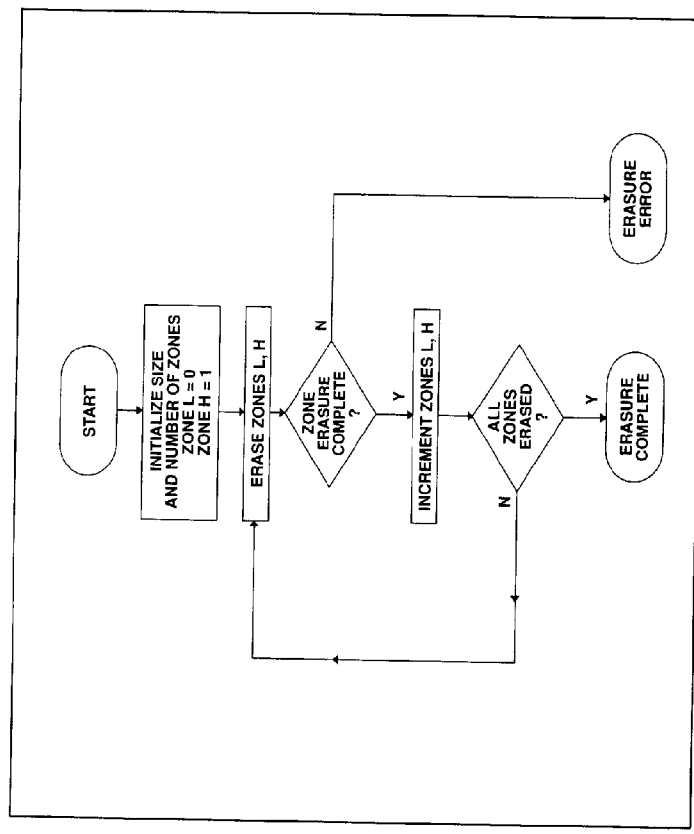


Figure 3. Full Card Erase Flow

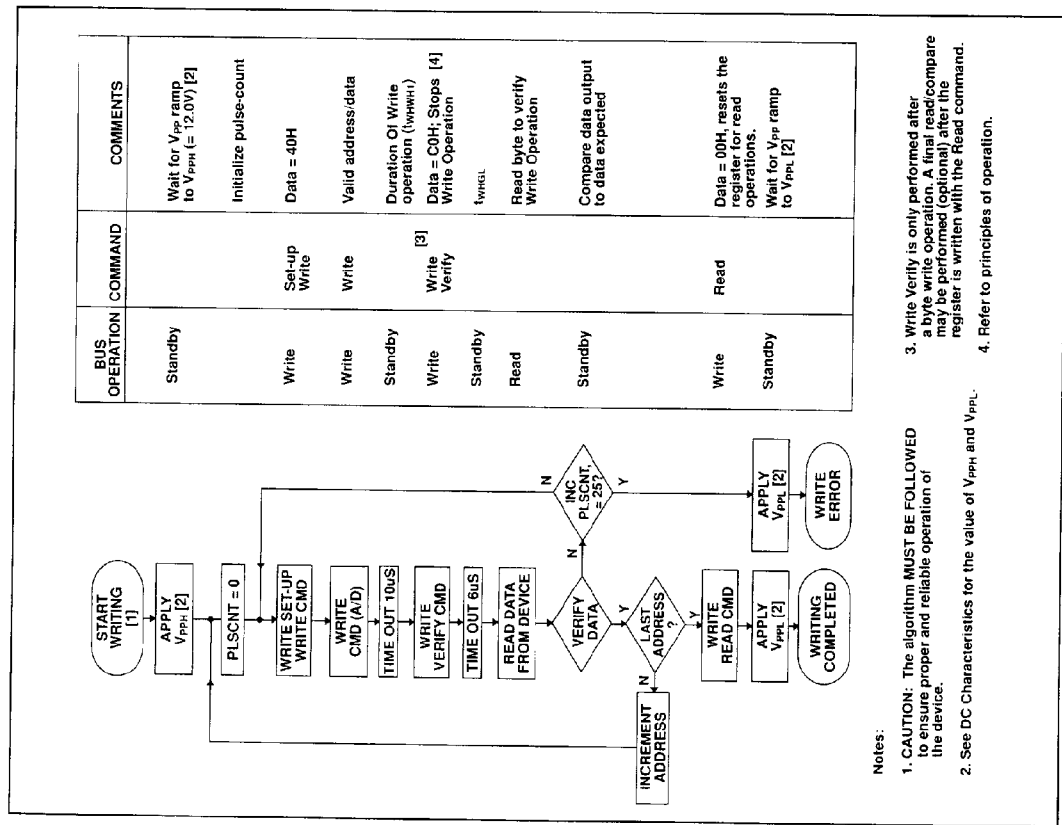


Figure 4. Write Algorithm for byte-wide mode

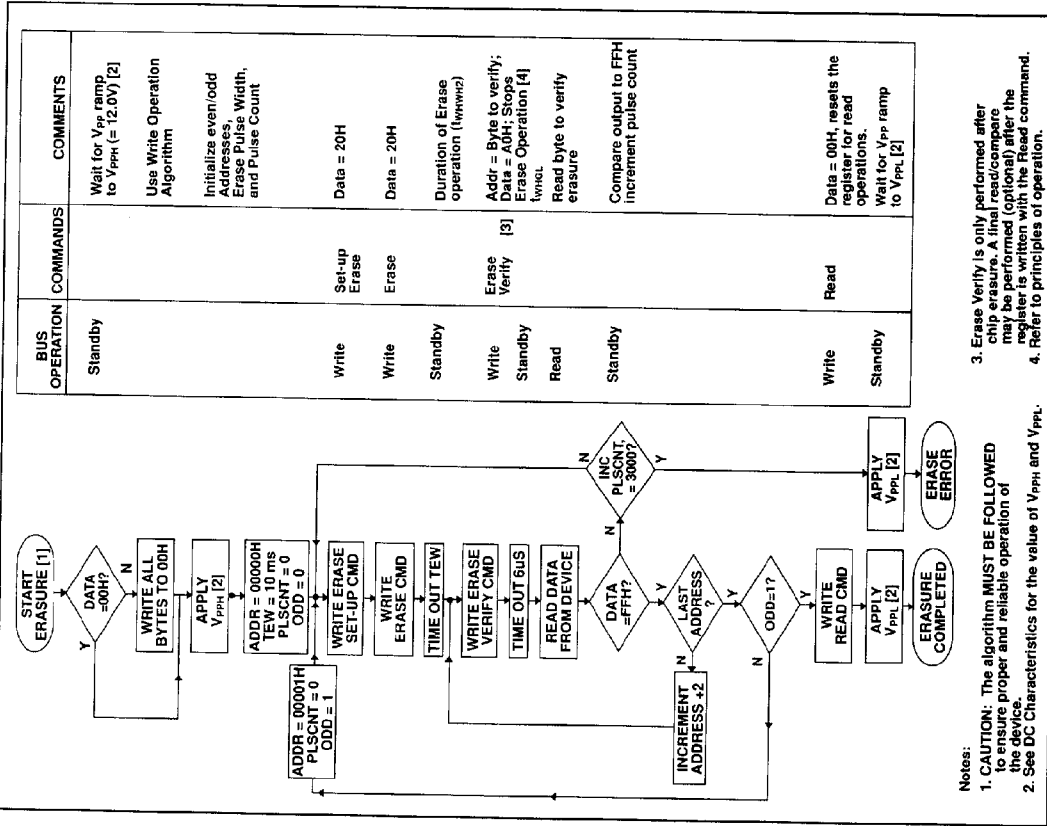


Figure 5. Erase Algorithm for byte-wide mode

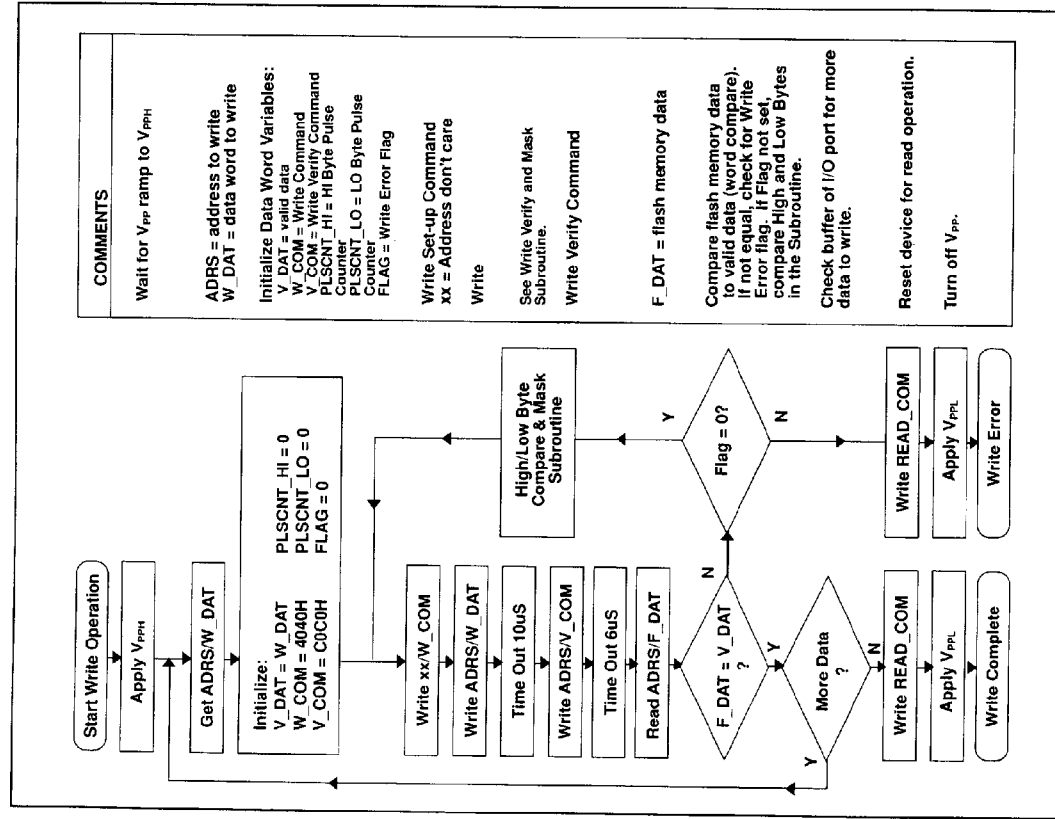


Figure 6. Write Algorithm for word-wide mode

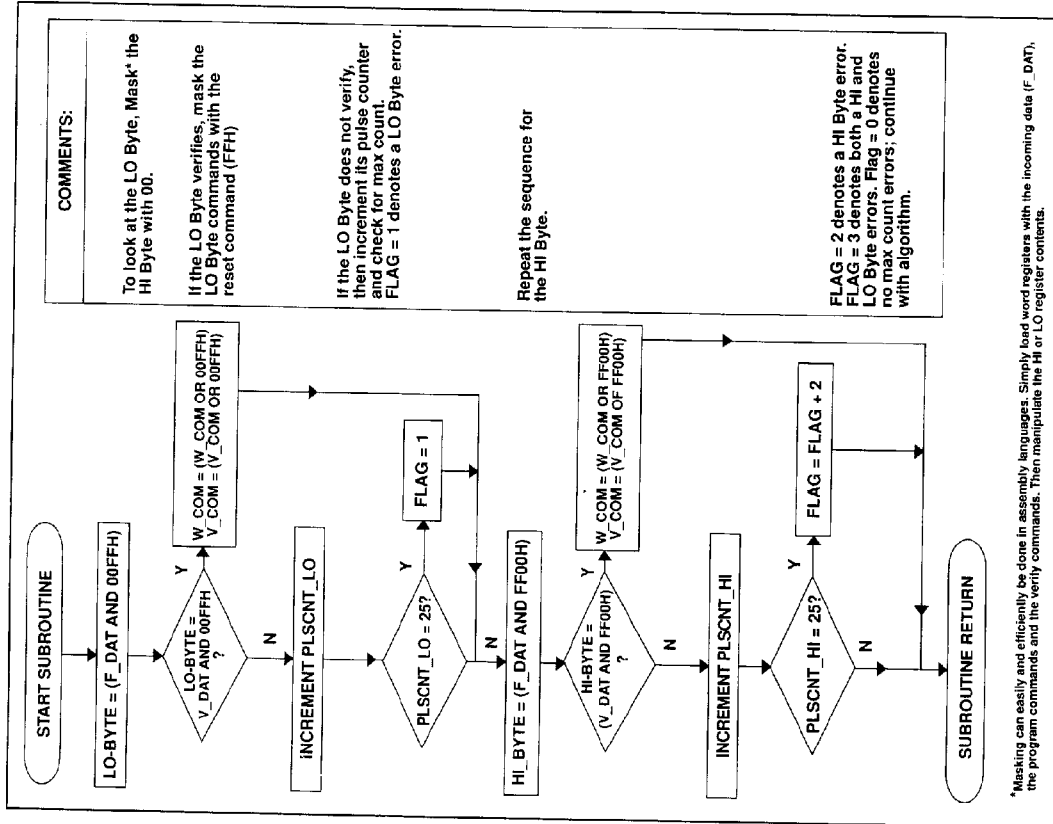


Figure 7. Write Verify and Mask Subroutine for word-wide mode

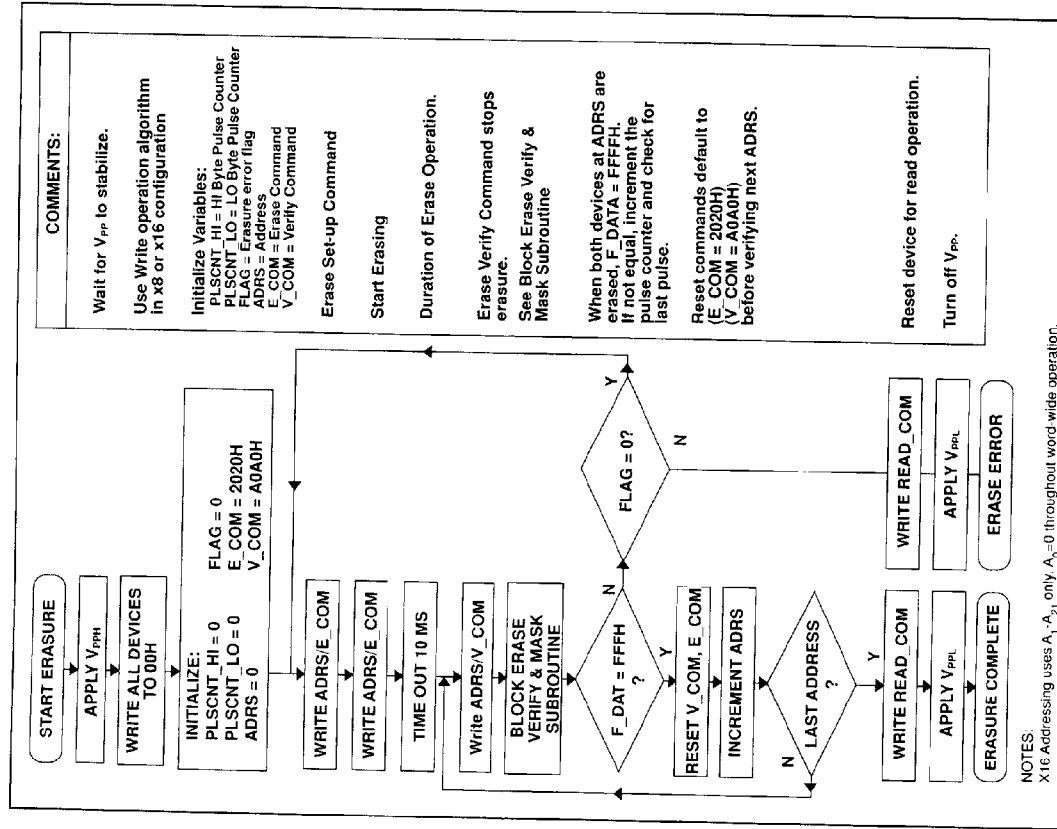
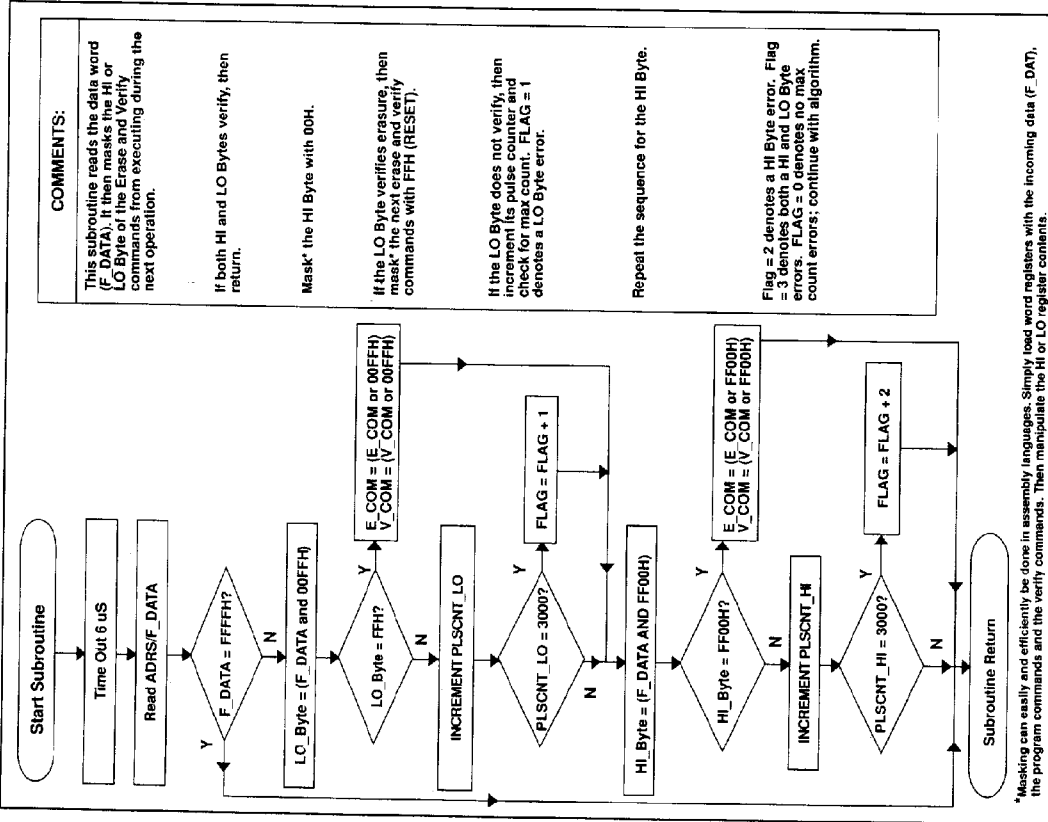


Figure 8. Erase Algorithm for word-wide mode



*Masking can easily and efficiently be done in assembly languages. Simply load word registers with the incoming data (F_DATA), the program commands and the verify commands. Then manipulate the HI or LO register contents.

Figure 9. Erase Verify and Mask Subroutine for word-wide mode.

SYSTEM DESIGN CONSIDERATIONS

Three-Line Control

Three-line control provides for:

- a. the lowest possible power dissipation and,
- b. complete assurance that output bus contention will not occur.

To efficiently use these three control inputs, an address-decoder output should drive CE₁ while the system's Read signal controls the card OE signal, and other parallel zones. This, coupled with the internal zone decoder, assures that only enabled memory zones have active outputs, while deselected zones maintain the low power standby condition.

Power-Supply Decoupling

Flash memory power-switching characteristics require careful device decoupling. System designers are interested in three supply current issues — standby, active and transient current peaks, produced by falling and rising edges of CE_{1/2}. The capacitive and inductive loads on the card and internal flash memory zones determine the magnitudes of these peaks.

Three-line control and proper decoupling capacitor selection will suppress transient voltage peaks. The IMC004FLKA features on-card ceramic decoupling capacitors connected between V_{CC} and V_{SS}, and between V_{PP1}/V_{PP2} and V_{SS}.

The card connector should also have a 4.7µF electrolytic capacitor between V_{CC} and V_{SS}, as well as between V_{PP1}/V_{PP2} and V_{SS}. The bulk capacitors will overcome voltage slumps caused by printed-circuit-board trace inductance, and will supply charge to the smaller capacitors as needed.

Power Up/Down Protection

The PCMCIA/JEIDA socket is specified, via unique pin lengths, to properly sequence the power supplies to the flash memory card. This assures that hot insertion and removal will not result in card damage or data loss.

Each zone in the IMC004FLKA is designed to offer protection against accidental erasure or writing, caused by spurious system-level signals that may exist during power transitions. The card will power-up into the read state.

A system designer must guard against active writes for V_{CC} voltages above V_{LKO} when V_{PP} is active. Since both WE and CE_{1/2} must be low for a command write, driving either to V_{HI} will inhibit writes. With its control register architecture, alteration of zone contents only occurs after successful completion of the two-step command sequences.

While these precautions are sufficient for most applications, it is recommended that V_{CC} reach its steady state value before raising V_{PP1/2} above V_{CC} + 2.0V. In addition, upon powering-down, V_{PP1/2} should be below V_{CC} + 2.0V, before lowering V_{CC}.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to + 60°C ⁽¹⁾
During Read	0°C to + 60°C
During Erase/Write	- 10°C to + 70°C
Temperature Under Bias	- 30°C to + 70°C
Storage Temperature	- 55°C to + 125°C
Voltage on Any Pin with Respect to Ground	- 2.0V to + 7.0V ⁽²⁾
V _{PP} , V _{PP1} , V _{PP2} Supply Voltage with Respect to Ground	- 2.0V to + 14.0V ^(2,3)
V _{CC} Supply Voltage with Respect to Ground	- 2.0V to + 7.0V ⁽²⁾

Notes:

1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC input voltage is -0.5V. During transitions, inputs may undershoot to -2.0V for periods less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5V, which may overshoot to V_{CC} + 2.0V for periods less than 20 ns.
3. Maximum DC input voltage on V_{PP1}/V_{PP2} may overshoot to +14.0V for periods less than 20 ns.

DC CHARACTERISTICS — Byte Wide Mode

Symbol	Parameter	Notes	Limits		Unit	Test Condition
			Min	Max		
I _I	Input Leakage Current	1	± 1.0	± 20	µA	V _{CC} = V _{CC} max V _{IN} = V _{CC} or V _{SS}
I _O	Output Leakage Current	1	± 1.0	± 20	µA	V _{CC} = V _{CC} max V _{OUT} = V _{CC} or V _{SS}
I _{CCS}	V _{CC} Standby Current	1	0.8	1.6	mA	V _{CC} = V _{CC} max CE = V _{PP}
I _{CC1}	V _{CC} Active Read Current	1,2	40	70	mA	V _{CC} = V _{CC} max CE = V _L f = 6MHz, I _{OUT} = 0mA
I _{CC2}	V _{CC} Write Current	1,2	1.0	12.0	mA	Writing in progress
I _{CC3}	V _{CC} Erase Current	1,2	6.0	17	mA	Erase in progress
I _{CC4}	V _{CC} Write Verify Current	1,2	6.0	17	mA	V _{PP} = V _{PPH} Write Verify in progress
I _{CC5}	V _{CC} Erase Verify Current	1,2	6.0	17	mA	V _{PP} = V _{PPH} Erase Verify in progress
I _{PPS}	V _{PP} Leakage Current	1	± 80		µA	V _{PP} ≤ V _{CC}
I _{PP1}	V _{PP} Read Current or Standby Current	1,3	0.7	1.6	mA	V _{PP} > V _{CC} V _{PP} ≤ V _{CC}
I _{PP2}	V _{PP} Write Current	1,3	8.0	30	mA	V _{PP} = V _{PPH} Write in progress
I _{PP3}	V _{PP} Erase Current	1,3	10	30	mA	V _{PP} = V _{PPH} Erase in progress
I _{PP4}	V _{PP} Write Verify Current	1,3	3.0	6.0	mA	V _{PP} = V _{PPH} Write Verify in progress
I _{PP5}	V _{PP} Erase Verify Current	1,3	3.0	6.0	mA	V _{PP} = V _{PPH} Erase Verify in progress
V _{IL}	Input Low Voltage		-0.5	0.8	V	
V _{IH}	Input High Voltage		2.4	V _{CC} + 0.3	V	
V _{OL}	Output Low Voltage			0.40	V	I _{OL} = 3.2mA V _{CC} = V _{CC} min
V _{OHI}	Output High Voltage		3.8		V	I _{OH} = -2.0mA V _{CC} = V _{CC} min
V _{PPL}	V _{PP} During Read-Only Operations		0.00	6.5	V	Note: Erase/Write are inhibited when V _{PP} = V _{PPL}
V _{PPH}	V _{PP} During Read/Write Operations		11.40	12.60	V	
V _{LKO}	V _{CC} Erase/Write lock voltage		2.5		V	

Notes:

1. All currents are in RMS unless otherwise noted. Typical values at V_{CC} = 5.0V, V_{PP} = 12.0V, T = 25°C.
2. 1 chip active and 15 in standby for byte-wide mode.
3. Assumes 1 V_{PP} is active.

OPERATING CONDITIONS

Symbol	Parameter	Limits		Unit	Comments
		Min	Max		
T _A	Operating Temperature	0	60	°C	For Read-Only and Read/Write Operations
V _{CC}	V _{CC} Supply Voltage	4.75	5.25	V	
V _{PPH}	Active V _{PP1} , V _{PP2} Supply Voltages	11.40	12.60	V	
V _{PPL}	V _{PP} During Read Only Operations	0.00	6.50	V	

DC CHARACTERISTICS — Word Wide Mode

Symbol	Parameter	Notes	Limits		Test Condition
			Min	Max	
I_{LI}	Input Leakage Current	1	± 1.0	± 20	$V_{CC} = V_{CC\ max}$ $V_{IN} = V_{CC}$ or V_{SS}
I_{LO}	Output Leakage Current	1	± 1.0	± 20	$V_{CC} = V_{CC\ max}$ $V_{OUT} = V_{CC}$ or V_{SS}
I_{CCS}	V_{CC} Standby Current	1	0.8	1.6	$V_{CC} = V_{CC\ max}$ $CE = V_{IH}$
I_{CC1}	V_{CC} Active Read Current	1,2	50	100	$V_{CC} = V_{CC\ max}$ $CE = V_{IL}$ $f = 6\text{MHz}$, $t_{OUT} = 0\text{ms}$
I_{CC2}	V_{CC} Write Current	1,2	2.0	20	Writing in progress
I_{CC3}	V_{CC} Erase Current	1,2	10	30	Erase in progress
I_{CC4}	V_{CC} Write Verify Current	1,2	10	30	$V_{PP} = V_{PPH}$ Write Verify in progress
I_{CC5}	V_{CC} Erase Verify Current	1,2	10	30	$V_{PP} = V_{PPH}$ Erase Verify in progress
I_{PPS}	V_{PP} Leakage Current	1	± 160		$V_{PP} \leq V_{CC}$
I_{PP1}	V_{PP} Read Current or Standby Current	1,3	1.5	3.0	$V_{PP} > V_{CC}$
I_{PP2}	V_{PP} Write Current	1,3	± 16		$V_{PP} \leq V_{CC}$
I_{PP3}	V_{PP} Erase Current	1,3	17	63	$V_{PP} = V_{PPH}$ Write in progress
I_{PP4}	V_{PP} Write Verify Current	1,3	20	60	$V_{PP} = V_{PPH}$ Erase in progress
I_{PP5}	V_{PP} Erase Verify Current	1,3	5.0	12	$V_{PP} = V_{PPH}$ Write Verify in progress
V_{IL}	Input Low Voltage		-0.5	0.8	Erase Verify in progress
V_{IH}	Input High Voltage		2.4	$V_{CC} \pm 0.3$	
V_{OL}	Output Low Voltage			0.40	$I_{OL} = 3.2\text{mA}$ $V_{CC} = V_{CC\ min}$
V_{OH1}	Output High Voltage		3.8		$I_{OH} = -2.0\text{mA}$ $V_{CC} = V_{CC\ min}$
V_{PPL}	V_{PP} During Read-Only Operations		0.00	6.5	Note: Erase/Write are inhibited when $V_{PP} = V_{PPL}$
V_{PPH}	V_{PP} During Read/Write Operations		11.40	12.60	
V_{LKO}	V_{CC} Erase/Write lock voltage		2.5		

Notes:
 1. All currents are in RMS unless otherwise noted. Typical values at $V_{CC} = 5.0\text{V}$, $V_{PP} = 12.0\text{V}$, $T = 25^\circ\text{C}$.
 2. Chips active and 14 in standby for word-wide mode.
 3. Assumes 2 V_{PPS} are active.

CAPACITANCE $T = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$

Symbol	Parameter	Notes	Limits		Conditions
			Min	Max	
C_{IN}	Address Capacitance			8	$V_{IN} = 0\text{V}$
C_{INZ}	Control Capacitance			16	$V_{IN} = 0\text{V}$
C_{OUT}	Output Capacitance			21	$V_{OUT} = 0\text{V}$
$C_{I/O}$	I/O Capacitance			16	$V_{IO} = 0\text{V}$

AC TEST CONDITIONS

Input Rise and Fall Times (10% to 90%) 10 ns
 Input Pulse Levels Vol and Voh1
 Input Timing Reference Level Vol and Vih
 Output Timing Reference Level Vll and Vlh

AC CHARACTERISTICS — Read-Only Operations

Symbol	Characteristic	Notes	Min	Max	Unit
t_{WCY}/t_{RC}	Read Cycle Time	2	250		ns
t_{ELOW}/t_{CE}	Chip Enable Access Time	2		250	ns
t_{A0V}/t_{ACC}	Address Access Time	2		250	ns
t_{A0V}/t_{OE}	Output Enable Access Time	2		120	ns
t_{ELOW}/t_{1Z}	Chip Enable to Output in Low Z	2	5		ns
t_{EHOZ}	Chip Disable to Output in High Z	2		60	ns
t_{A0V}/t_{O1Z}	Output Enable to Output in Low Z	2	5		ns
t_{GHOZ}/t_{BF}	Output Disable to Output in High Z	2		60	ns
t_{OH}	Output Hold from Address, CE, or OE Change	1,2	5		ns
t_{WHCL}	Write Recovery Time Before Read	2	6		us

Notes:
 1. Whichever occurs first.
 2. Rise/Fall time $\leq 10\text{ns}$.

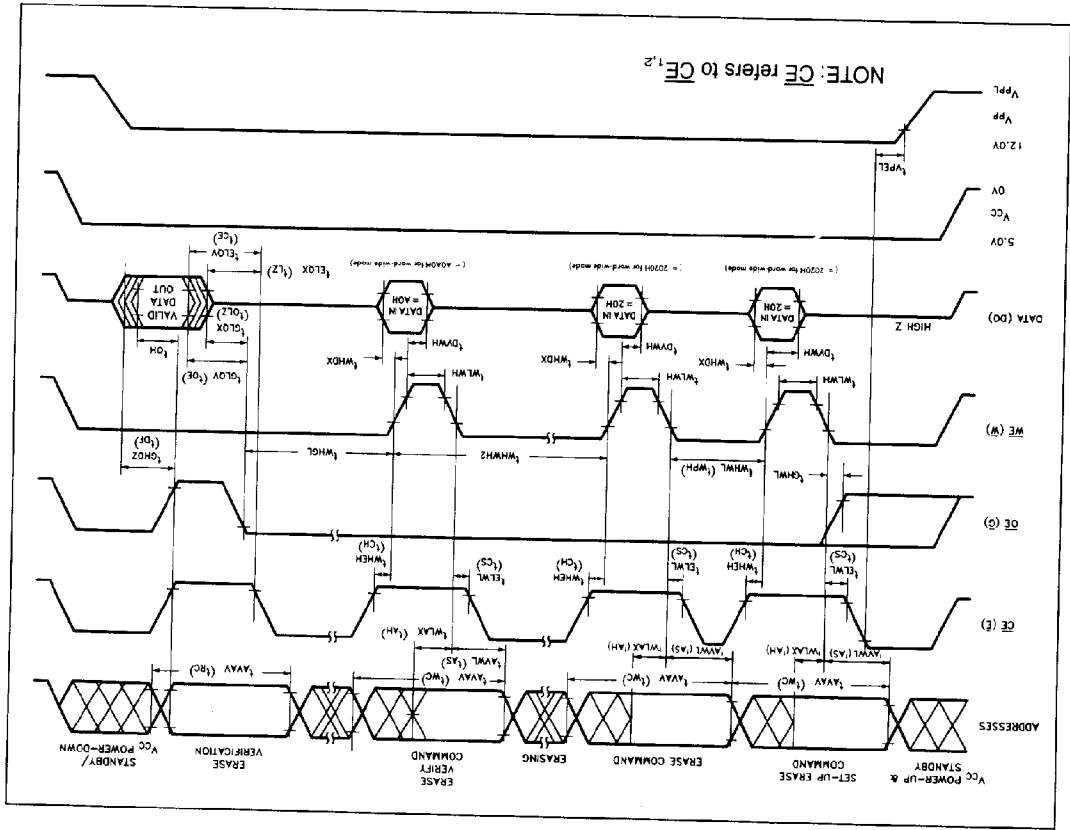


Figure 12. AC Waveforms for Erase Operations

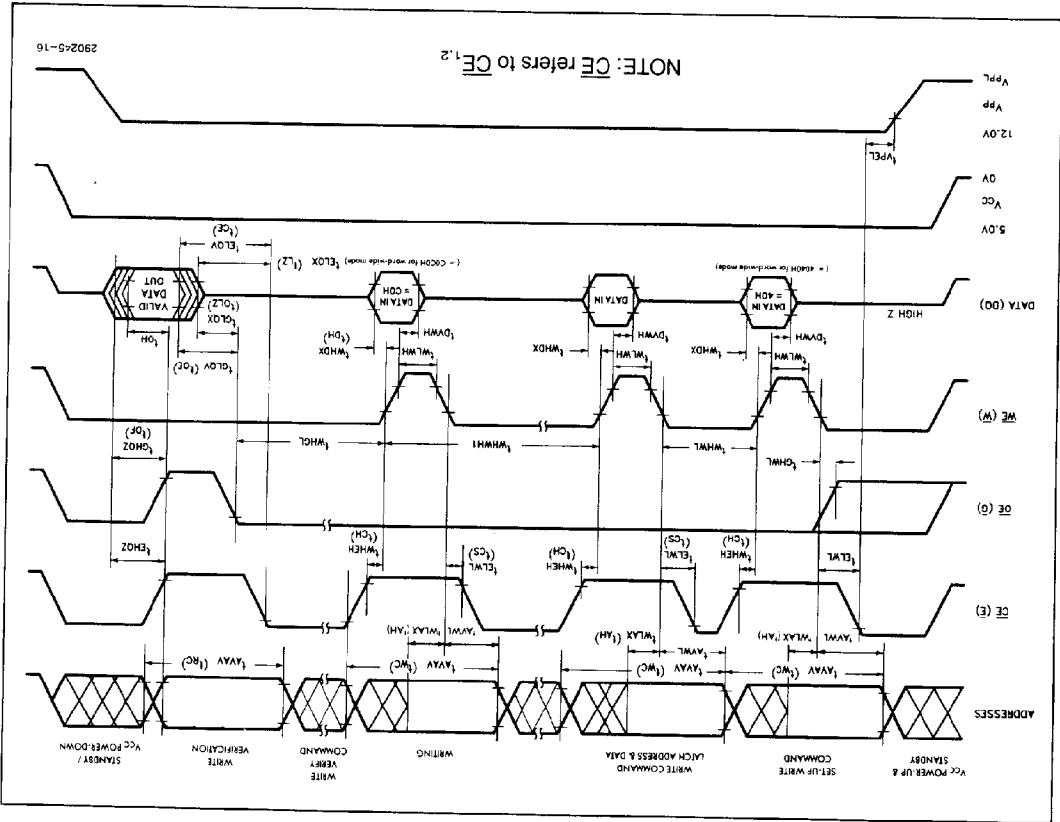


Figure 11. AC Waveforms for Write Operations

ALTERNATIVE \overline{CE} -CONTROLLED WRITES

Symbol	Characteristic	Notes	Min	Max	Unit
t_{AVAV}	Write Cycle Time		250		ns
t_{AVEL}	Address Set-up Time		0		ns
t_{ELAX}	Address Hold Time		100		ns
t_{OVEH}	Data Set-up Time		80		ns
t_{EHDX}	Data Hold Time		30		ns
t_{EHGL}	Write Recovery Time Before Read		6		us
t_{EHLL}	Read Recovery Time Before Write		0		us
t_{WLEL}	Write Enable Set-Up Time before Chip-Enable		0		ns
t_{EHWH}	Write Enable Hold Time		0		ns
t_{ELEH}	Write Pulse Width	1	100		ns
t_{EHLE}	Write Pulse Width High		20		ns
t_{PEL}	V_{PP} Set-Up Time to Chip-Enable Low		100		ns

Notes:

- Chip Enable Controlled Writes: Write operations are driven by the valid combination of Chip Enable and Write Enable. In systems where Chip Enable defines the write pulse width (with a longer Write Enable timing waveform) all set-up, hold and inactive Write Enable times should be measured relative to the Chip Enable waveform.

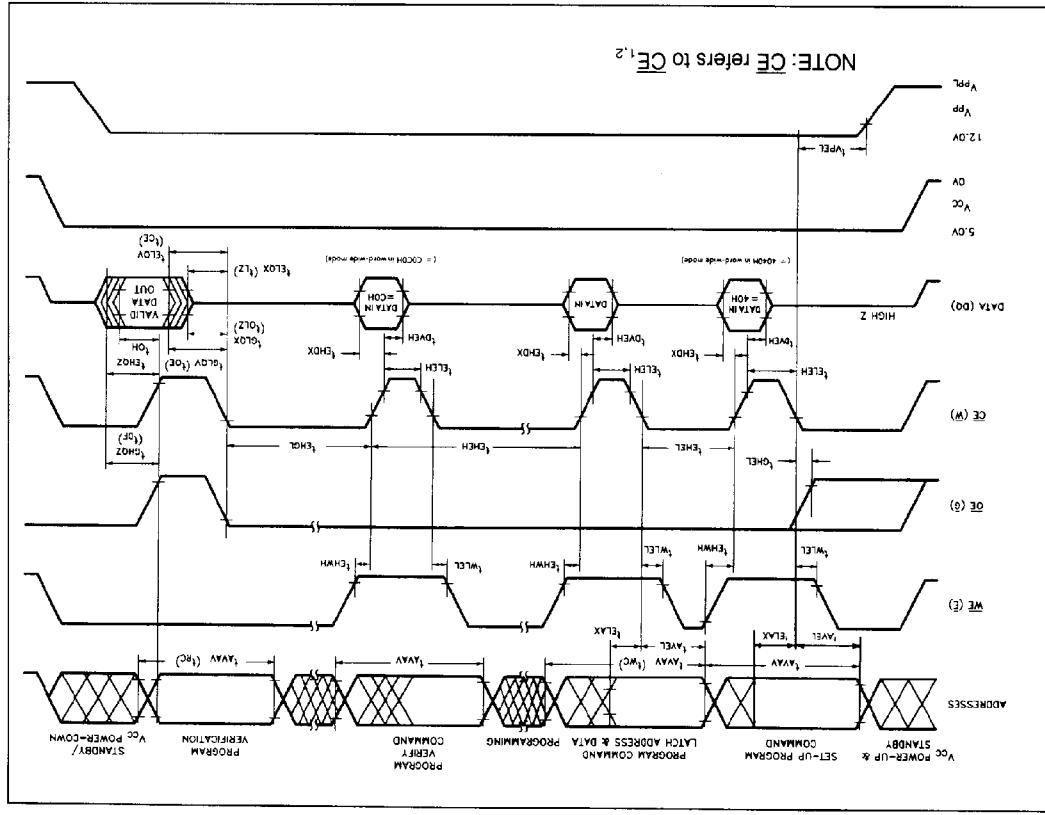


Figure 13. Alternate AC Waveforms for Write Operations



IMC004FLKA

ADVANCE INFORMATION

ORDERING INFORMATION

i M C 0 0 4 F L K A - 2 5 0 , S B X X X X X

CUSTOMER IDENTIFIER
ACCESS SPEED (ns)
A = REVISION
K = WORD-WIDE ARCHITECTURE
FL = FLASH
004 = 4 MEGABYTE DENSITY IN MEGABYTES
MC = MEMORY CARD
I = INTEL

Order Number
294005
293002
292079

ADDITIONAL INFORMATION
ER-20, "ETOX II Flash Memory Technology"
RR-60, "ETOX II Flash Memory Reliability Data Summary"
AP-343, "Solutions for High Density Applications using Flash Memory"

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