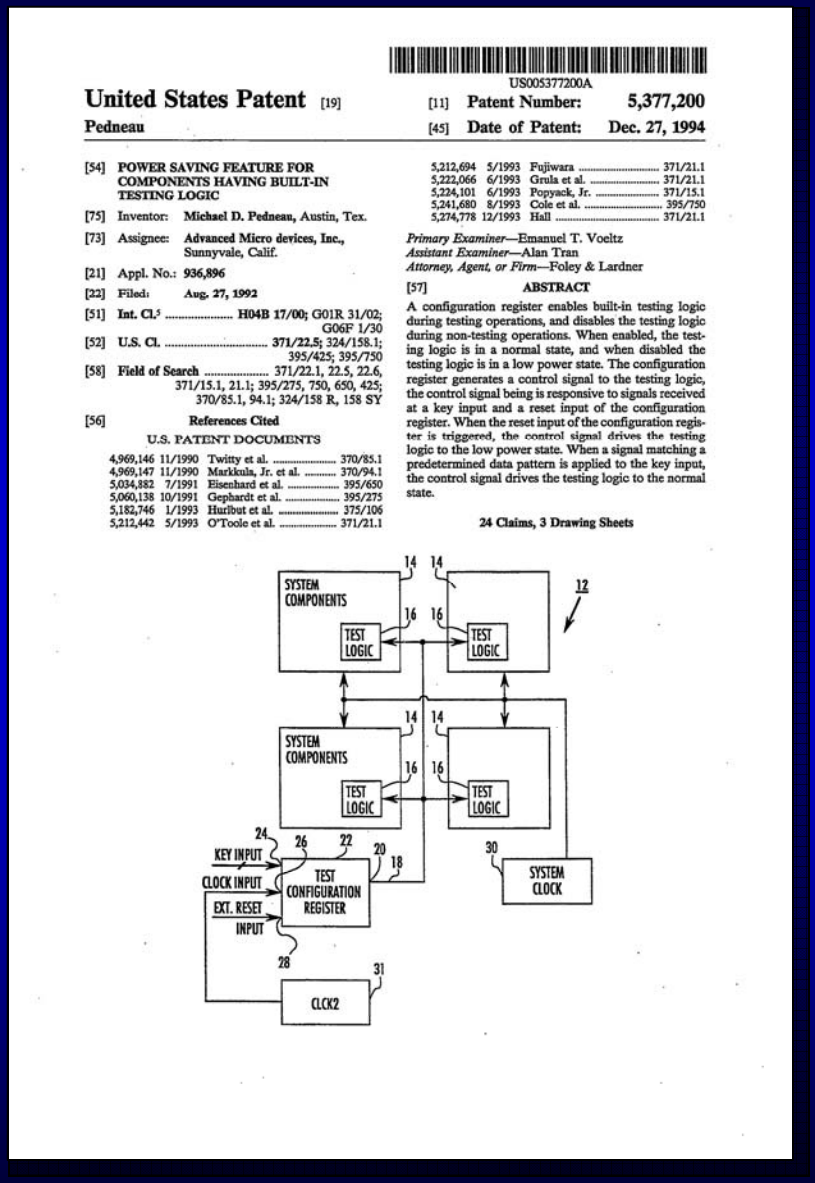
# EXHIBIT K



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**United States Patent** [19]

**Pedneau**

[11] **Patent Number: 5,377,200**

[45] **Date of Patent: Dec. 27, 1994**

[54] **POWER SAVING FEATURE FOR COMPONENTS HAVING BUILT-IN TESTING LOGIC**


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[73] Assignee: **Advanced Micro devices, Inc.**, Sunnyvale, Calif.



[21] Appl. No.: **936,896**

[22] Filed: **Aug. 27, 1992**

[51] **Int. Cl.**[5] ..... **H04B 17/00**; G01R 31/02; G06F 1/30

[52] **U.S. Cl.** ..... **371/22.5**; 324/158.1; 395/425; 395/750

[58] **Field of Search** ..... 371/22.1, 22.5, 22.6, 371/15.1, 21.1; 395/275, 750, 650, 425; 370/85.1, 94.1; 324/158 R, 158 SY



[56] **References Cited**

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[57] **ABSTRACT**

A configuration register enables built-in testing logic during testing operations, and disables the testing logic during non-testing operations. When enabled, the testing logic is in a normal state, and when disabled the testing logic is in a low power state. The configuration register generates a control signal to the testing logic, the control signal being is responsive to signals received at a key input and a reset input of the configuration register. When the reset input of the configuration register is triggered, the control signal drives the testing logic to the low power state. When a signal matching a predetermined data pattern is applied to the key input, the control signal drives the testing logic to the normal state.


**24 Claims, 3 Drawing Sheets**




# Pedneau

## U.S. Patent No. 5,377,200

# Pedneau: '200 Patent
# Technology

## Power-saving feature for processors having testing logic.

- Testing logic is used during product design to work out bugs and streamline the manufacturing process.
- Testing logic is used during the manufacturing process to improve yield (percent of products with no defects).
- Testing logic consumes power.

## Pedneau: '200 Patent

# The Problem the Invention Addresses

- In the prior art, the testing logic was always powered even though it was used only a miniscule percentage of the time. This was a waste of power.

## Pedneau: ’200 Patent

# Statement of the Invention

The invention is a system for controlling the power consumed by testing logic so that it consumes minimal power when not being utilized.

# Pedneau: ’200 Patent

# Pedneau’s Invention

## Key Input Activated – Test Circuitry in Normal Power State

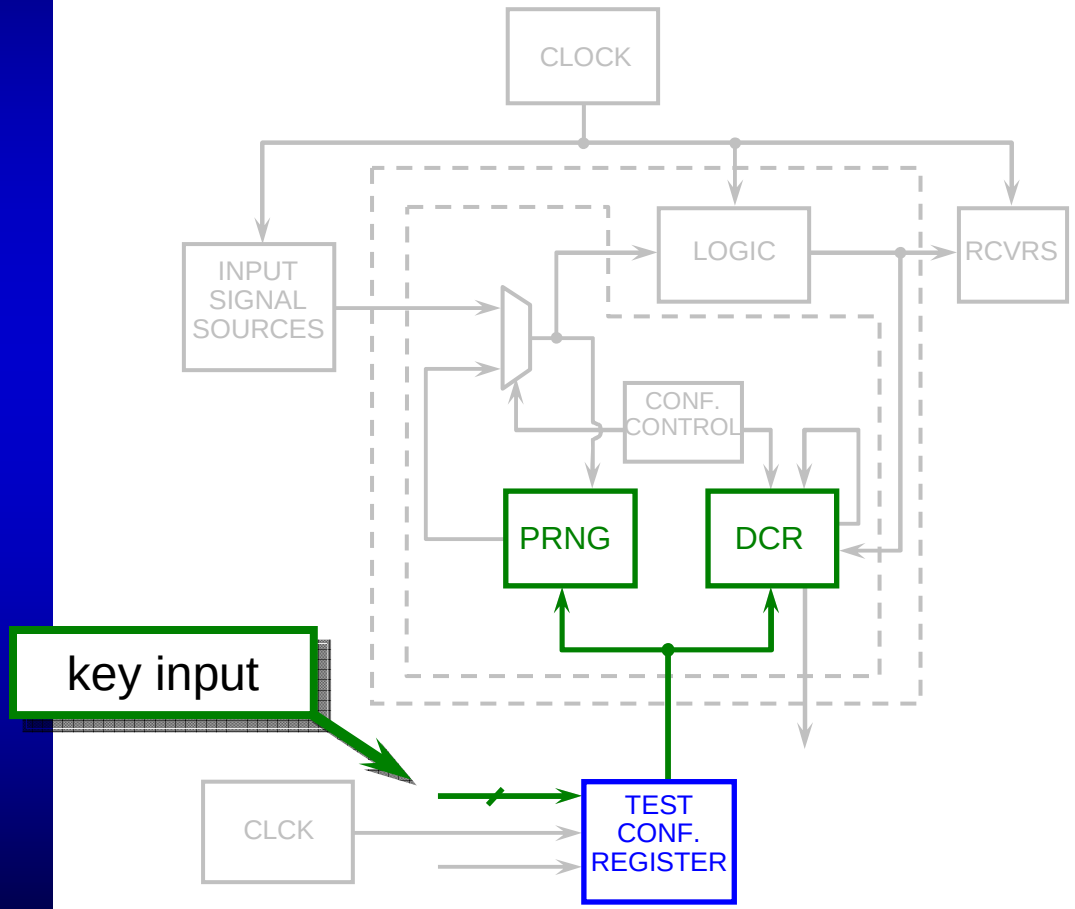


FIG. 2

# Pedneau: ’200 Patent

# Pedneau’s Invention

## Reset Input Activated – Test Circuitry in Low Power State

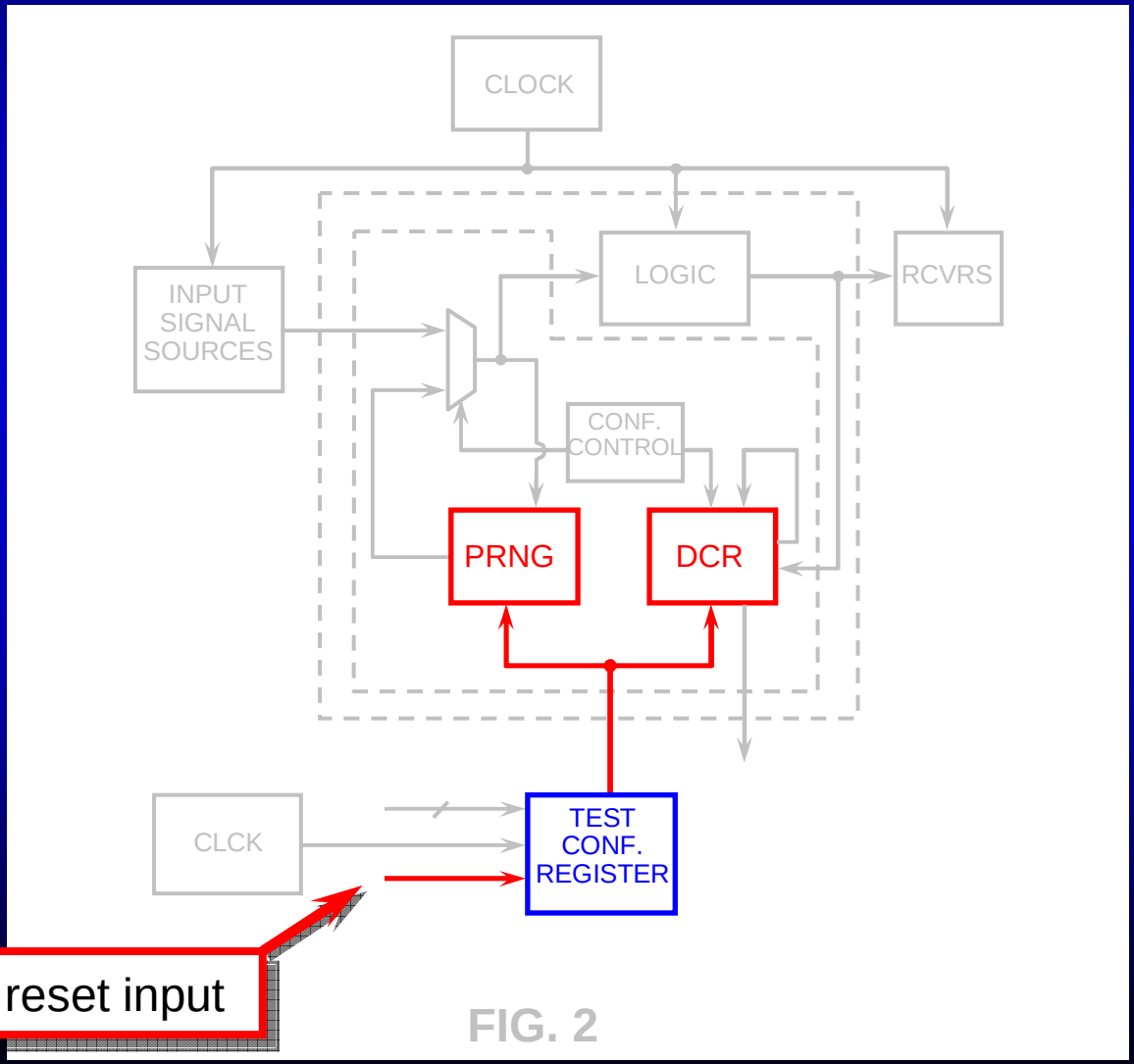


FIG. 2