Goodard v. Google, Inc.
Doc. 73 Att. 4

EXHIBIT D

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The following sets forth the manner in which the Defendants' (collectively referred to as "Samsung") DRAM products infringe U.S. Patent No. 5,248,893. Plaintiffs allege that all elements are present literally, but reserve the right to allege that any particular element is present by equivalents if Samsung establishes that the element is not present literally.

Claim	Claim Element Text	Infringement Support
1	An insulated gate field effect device comprising:	Samsung's DRAMs include insulated gate field effect transistors as set forth below.
1(a)	a first conductivity type semiconductor substrate having a main surface;	Samsung's DRAMs include a semiconductor substrate of a first conductivity type. The substrate has a main surface. This is shown in the figure below, which consists of a TEM image of a cross section of a transistor from an exemplar Samsung DRAM (K4T51083QE).[1] This figure shows the presence of a semiconductor substrate. The area below the dotted line labeled "Junction" has a first conductivity type. The area of the main surface is labeled on the TEM image.

[1] Plaintiffs' contentions are not limited to the exemplar Samsung DRAM chips depicted herein. Those depictions are for illustrative purposes only. Plaintiffs contend that Samsung's DRAM chips generally infringe, but are unable to identify the precise models without further discovery.

Claim	Claim Element Text	Infringement Support
		The TEM set forth above is from a cross section of a Samsung S-RCAT design. AMD's contentions are not limited to Samsung's DRAMs containing S-RCATs. Samsung's DRAMs containing RCATs also meet this claim element. As set forth in the cross-section SEM image depicted below (taken from Kim et al., Technology for sub-50nm DRAM and NAND Flash Memory, (2005)), those products have a substrate with a main surface (see area labeled "main surface"). The area below the dotted line would be of a first conductivity type.

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		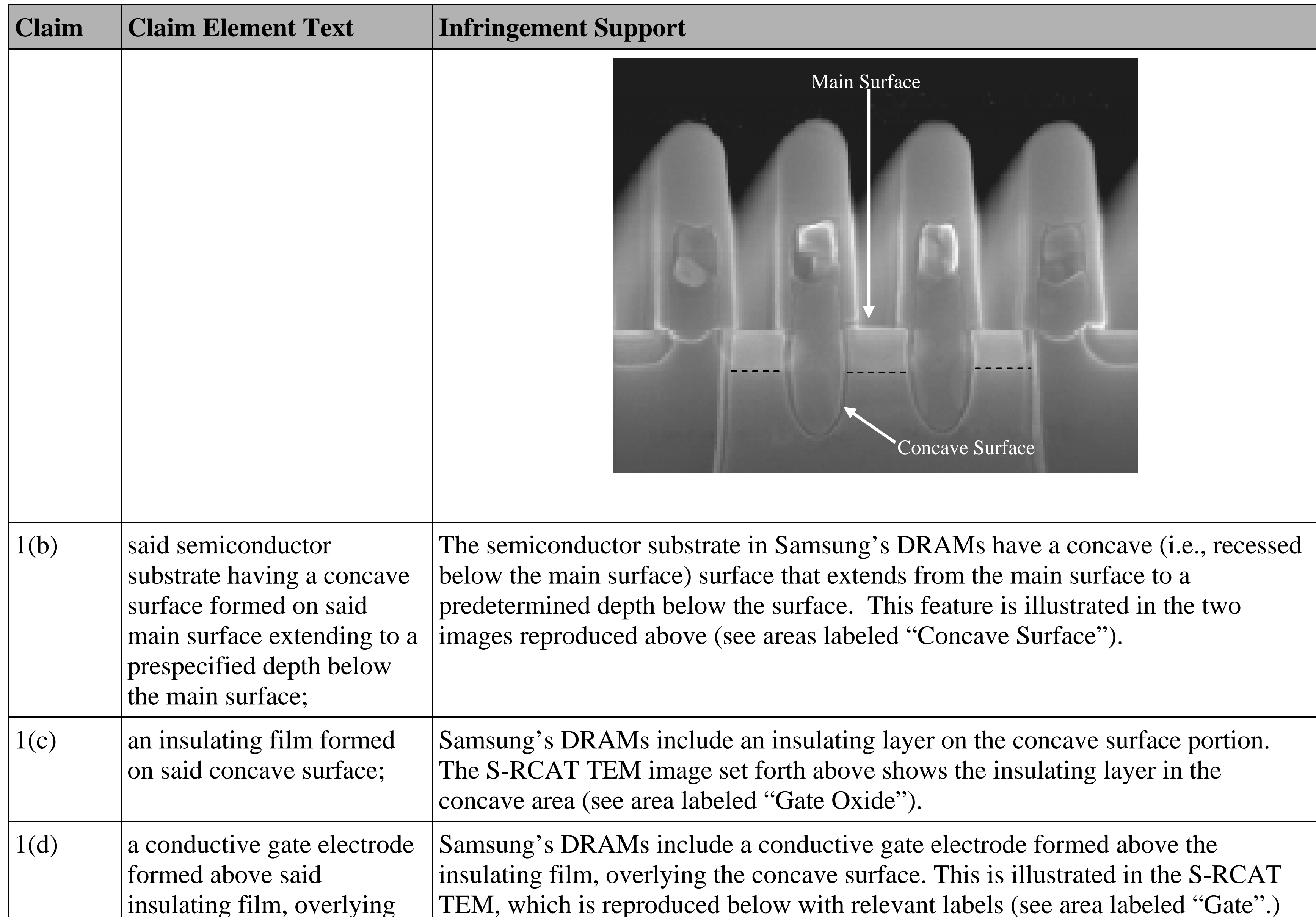
1(b)	said semiconductor substrate having a concave surface formed on said main surface extending to a prespecified depth below the main surface;	The semiconductor substrate in Samsung's DRAMs have a concave (i.e., recessed below the main surface) surface that extends from the main surface to a predetermined depth below the surface. This feature is illustrated in the two images reproduced above (see areas labeled "Concave Surface").
1(c)	an insulating film formed on said concave surface;	Samsung's DRAMs include an insulating layer on the concave surface portion. The S-RCAT TEM image set forth above shows the insulating layer in the concave area (see area labeled "Gate Oxide").
1(d)	a conductive gate electrode formed above said insulating film, overlying	Samsung's DRAMs include a conductive gate electrode formed above the insulating film, overlying the concave surface. This is illustrated in the S-RCAT TEM, which is reproduced below with relevant labels (see area labeled "Gate".)

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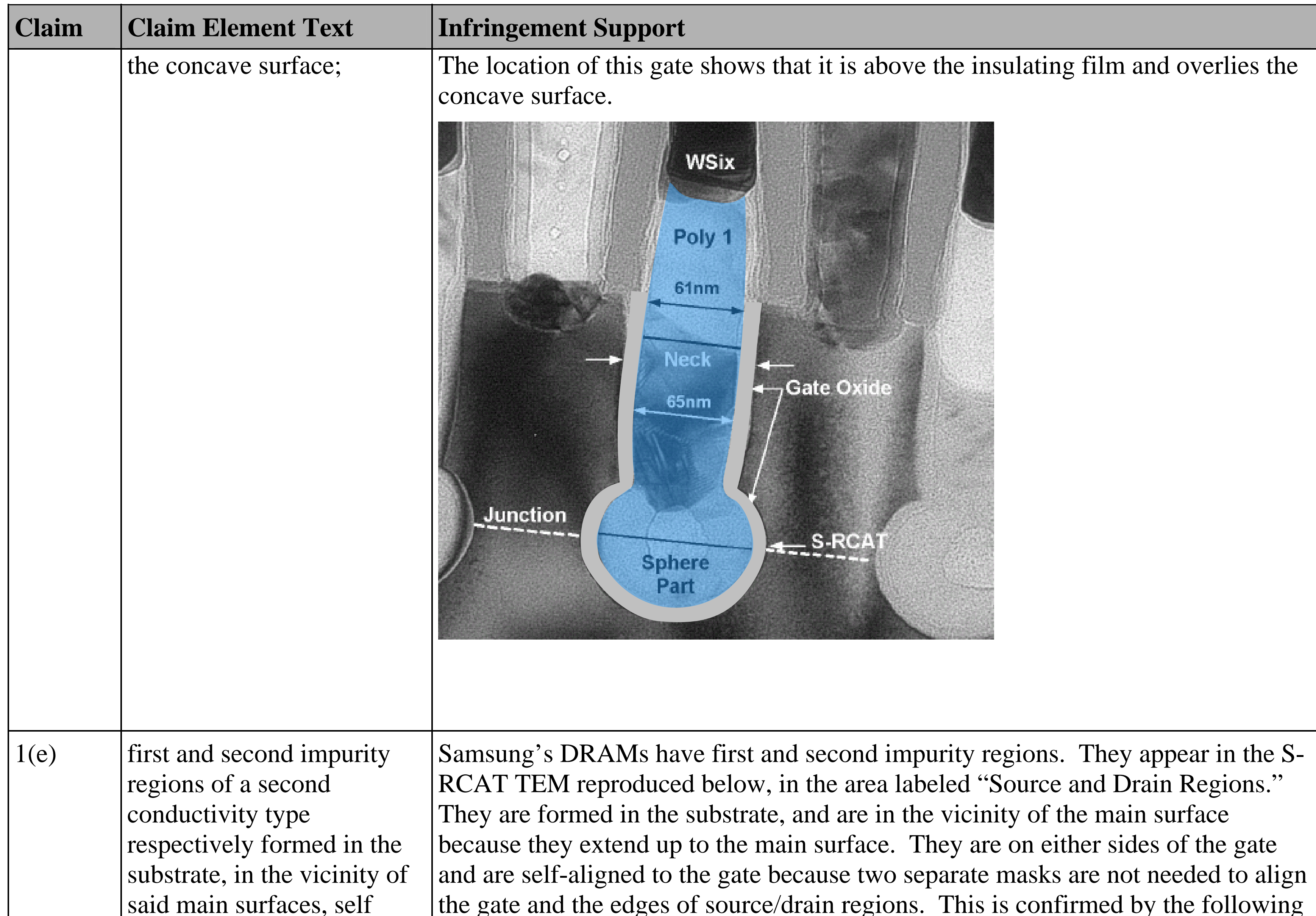
	the concave surface;	The location of this gate shows that it is above the insulating film and overlies the concave surface. 
1(e)	first and second impurity regions of a second conductivity type respectively formed in the substrate, in the vicinity of said main surfaces, self	Samsung's DRAMs have first and second impurity regions. They appear in the S-RCAT TEM reproduced below, in the area labeled "Source and Drain Regions." They are formed in the substrate, and are in the vicinity of the main surface because they extend up to the main surface. They are on either sides of the gate and are self-aligned to the gate because two separate masks are not needed to align the gate and the edges of source/drain regions. This is confirmed by the following

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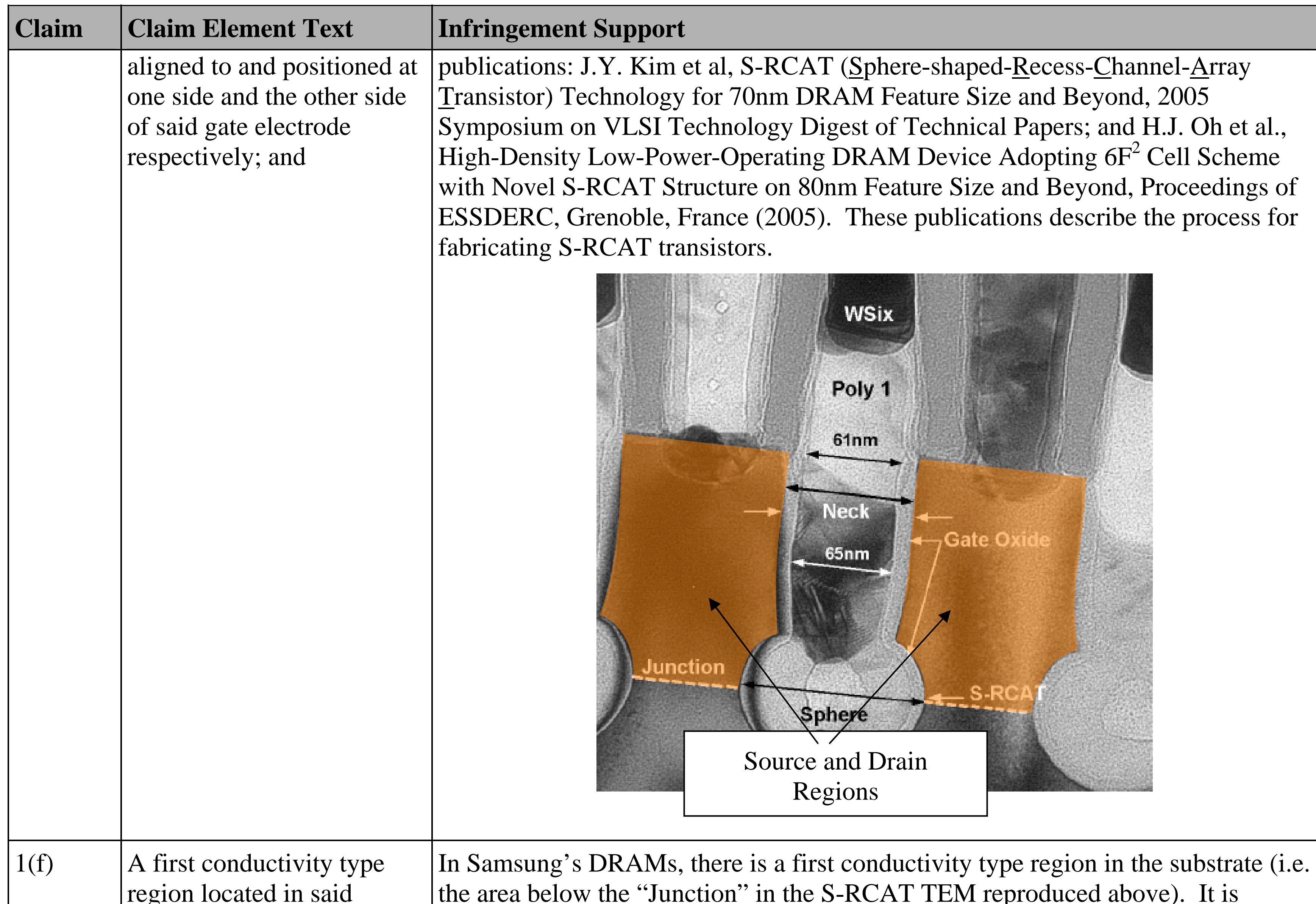
	aligned to and positioned at one side and the other side of said gate electrode respectively; and	publications: J.Y. Kim et al, S-RCAT (Sphere-shaped-Recess-Channel-Array Transistor) Technology for 70nm DRAM Feature Size and Beyond, 2005 Symposium on VLSI Technology Digest of Technical Papers; and H.J. Oh et al., High-Density Low-Power-Operating DRAM Device Adopting $6F^2$ Cell Scheme with Novel S-RCAT Structure on 80nm Feature Size and Beyond, Proceedings of ESSDERC, Grenoble, France (2005). These publications describe the process for fabricating S-RCAT transistors. 
1(f)	A first conductivity type region located in said	In Samsung's DRAMs, there is a first conductivity type region in the substrate (i.e. the area below the "Junction" in the S-RCAT TEM reproduced above). It is

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	semiconductor substrate between said first and second impurity regions for defining a channel region and a channel-free region extending conformably under and along said concave surface	between the source and drain regions because it extends from one to the other. The channel region and the channel free region forms in the first impurity region under and along the gate oxide that extends under the portion of the gate labeled "Sphere Part" in the TEM reproduced above.
1(g)	wherein the depth of said concave surface is set to a value which ranges between one and two times the depth of said first and second impurity regions, and	It is readily apparent in the S-RCAT TEM reproduced above that depth of the concave surface is between one and two times the depth of the source/drain.
1(h)	wherein the concave surface is continuously curved in the vicinity of at least one of the first and second impurity regions to produce smooth merger of a conforming first depletion region formed around the at least one impurity region and a conforming second depletion region formed in the vicinity of the gate electrode so that excessive field concentration will not	In Samsung's DRAMs, the concave surface is continuously curved in the area just below the area labeled "junction" in the S-RCAT TEM depicted above, which is where the first and second impurity regions (i.e. the source/drain regions) exist. By virtue of this shape, the depletion region formed around the gate and the depletion regions formed around the impurity regions would merge together in a smooth way. As a result, excessive field concentration would not develop in the area of merger.

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	develop in the vicinity where the first and second depletion regions meet	
2	An insulated gate field effect device according to claim 1, wherein one of said first and second impurity regions constitutes a drain-region of said insulated gate field effect device, the other of said first and second impurity regions constitutes a source region and wherein the concave surface is continuously curved at least in the vicinity of the drain region, where the channel-free region develops during an off state of the device, to produce smooth merger of the conforming first depletion region which develops in the vicinity of the channel-free region and the drain region and the conforming second depletion region formed in the vicinity of the gate	The source/drain regions are identified in response to section 1(e) above. One of the two functions as the source and the other as the drain. As is evident from the image of the cross section set forth in that section, the lower portion of the concave surface is continuously curved at least in the vicinity of the drain. This is also in the vicinity of the area where the channel free region develops during the off state of the device. A transistor shaped and configured in this fashion would cause depletion regions to develop with a smooth merger of two depletion regions (the one that develops in the vicinity of the channel-free region and drain and the one that forms in the vicinity of the gate electrode). Accordingly, excessive field concentration would not develop in the vicinity of the channel-free region.

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	electrode so that excessive field concentration will not develop in the vicinity of the channel-free region.	
3	An insulated gate field effect device according to claim 1, which comprises a metal oxide semiconductor (MOS) transistor, and wherein said insulting film comprises an oxide film.	The transistors in Samsung's DRAMs are MOS transistors because they are comprised of a conductive electrode (i.e. polysilicon), oxide, and semiconductor. The insulating film (area labeled "gate oxide" in the figure reproduced in Section 1(a) above) is an oxide film.
4	An insulated gate field effect transistor comprising:	Samsung's DRAMs include insulated gate field effect transistors as set forth below.
4(a)	a substrate having a substantially planar main surface and a concave surface portion extending continuously from the main surface to a predetermined depth below the main surface;	Samsung's DRAMS include a semiconductor substrate, a portion of which has a substantially planar (flat) main surface, and another portion of which has a concave (i.e., recessed below the main surface) surface that extends continuously from the main surface to a predetermined depth below the surface. This is shown in the TEM image of the exemplar Samsung S-RCAT reproduced in Section 1(a) above. This figure shows the presence of a semiconductor substrate (see area labeled "Substrate") with a substantially planar main surface (see area labeled "Main Surface"). A portion of the substrate has a concave surface (see area labeled "Concave Surface.") As is illustrated in the figure, the concave surface extends down without interruption into the substrate, to a predetermined depth.

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		Samsung's DRAMS containing RCATs also meet this claim element. The RCAT cross-section SEM image reproduced in Section 1(a) above shows that those products have a substrate with a substantially planar main surface (see area labeled "main surface"), and a concave surface portion extending continuously from the main surface to a predetermined depth below the main surface (see area labeled "concave surface.")
4(b)	an insulating layer conformably disposed on the main surface and the concave surface portion;	Samsung's DRAMs include an insulating layer on the substantially flat main surface, as well as the concave surface portion. The S-RCAT TEM image set forth in Section 1(a) above shows the insulating layer in the concave area (see area labeled "Gate Oxide"). In addition, the SEM image set out below, taken from the same S-RCAT exemplar product, confirms the presence of the insulating layer conformably disposed on the main surface (see area labeled "Gate Oxide.")

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		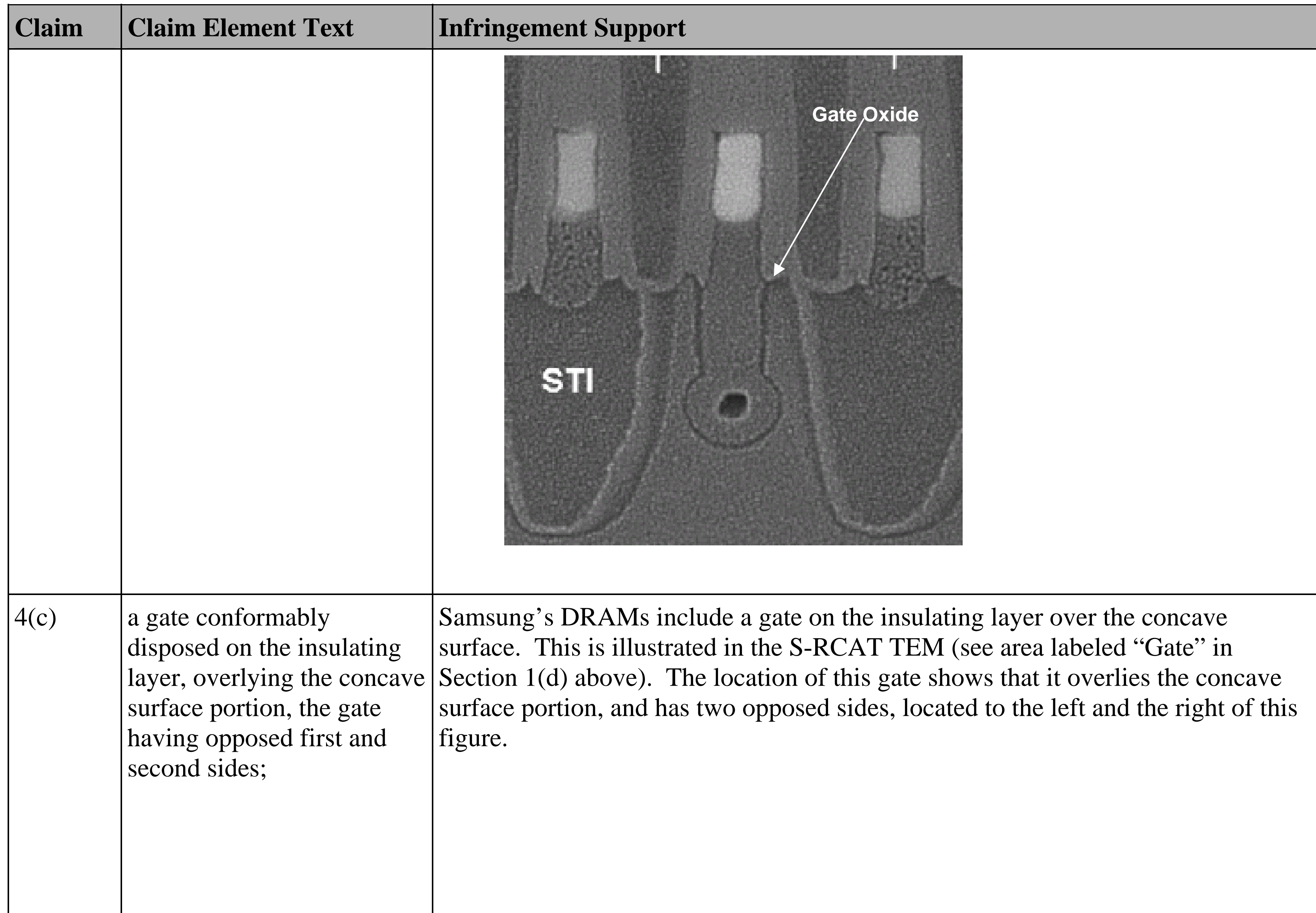
4(c)	a gate conformably disposed on the insulating layer, overlying the concave surface portion, the gate having opposed first and second sides;	Samsung's DRAMs include a gate on the insulating layer over the concave surface. This is illustrated in the S-RCAT TEM (see area labeled "Gate" in Section 1(d) above). The location of this gate shows that it overlies the concave surface portion, and has two opposed sides, located to the left and the right of this figure.

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4(d)	implanted source and drain regions disposed within the substrate and self-aligned to the respective first and second opposed sides of the gate; and	The transistors in Samsung's DRAMs include source and drain regions located within the substrate, adjacent to the opposed sides of the gate. This is illustrated in the S-RCAT TEM reproduced in Section 1(e) above with relevant labeling (see area labeled "Source and Drain Regions)." These source/drain regions are self-aligned because two separate masks are not needed to align the gate and the edges of source/drain regions. This is confirmed by the publications cited in Section 1(e) above, which describe the process for fabricating S-RCAT Transistors.
4(e)	a channel-region formed between the source and drain regions, for defining a channel that conducts current between the source and drain regions when the transistor is in a turned-on state;	The transistors in the Samsung's DRAMs formed in accordance with the elements above will necessarily have a channel-region along the bottom of the area labeled "sphere part" running between the source and drain. This channel-region necessarily conducts current between the source and drain regions when the transistor is in a turned-on state. Otherwise, the transistor could not work.
4(f)	wherein a channel-free zone develops in the substrate, under the gate and between the source and drain regions, when the transistor	The transistors in Samsung's DRAMs formed in accordance with the elements above will necessarily have a channel-free zone that develops in the substrate, at the bottom of the area labeled "sphere part" running between the source and drain, when the transistor is in a turned-off state. Otherwise, the transistor would not work.

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	is in a turned-off state; and	
4(g)	wherein the gate and concave surface portion are curved at least in the vicinity of the channel-free zone such that a smoothly curved depletion zone boundary will develop in the vicinity of the channel-free zone when the transistor is in the turned-off state.	The transistors in Samsung's DRAMs include a gate and concave surface portion that are curved at the bottom, as is illustrated in the TEMS set forth above. This curvature is in the vicinity of the channel-free zone because the channel-free zone is just below the gate and concave surface. As a result of the curved shape of the surface portion at the bottom of the gate, a smoothly-curved depletion zone boundary develops near the channel-free zone when the transistor is in a turned-off state.
5	An insulated-gate field effect transistor according to claim 4 wherein the concave surface portion is curved in a transverse cross-sectional plane extending through the transistor between but not intersecting the first and second sides of the gate so as to provide an effective channel width greater than a width of the channel as projected onto the plane of the main substrate surface.	Because the bottom of the gate in Samsung's S-RCATs is spherical (see area labeled "Sphere Part" in the S-RCAT TEMs depicted above), the concave surface portion is curved in a transverse cross-sectional plane, where such plane extends through the transistor between but not intersecting the first and second sides of the gate. This shape would provide an effective channel width greater than a width of the channel as projected onto the plane of the main substrate surface.

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6	An insulated-gate field effect transistor according to claim 5 wherein the concave surface portion is curved both in the transverse cross-sectional plane and in a non-transverse cross-sectional plane, extending between and joining the first and second sides of the gate, so as to provide an effective channel surface area greater than an area of the channel as projected onto the plane of the main substrate surface.	Because the lower portion of the gate in Samsung's S-RCAT transistors is spherical, it is curved in the relevant portion (i.e. in such a way that it provides an effective channel surface area greater than an area of the channel as projected onto the plane of the main substrate surface.) Further, because it is spherical, the curvature exists both in the transverse cross-sectional plane and in a non-transverse cross-sectional plane. As is plainly evident from the TEM reproduced above, the concave surface portion extends between and joins the first and second sides of the gate.
7	An insulated-gate field effect transistor according to claim 6 wherein the concave surface portion is equally curved both in the transverse cross-sectional plane and in the non-transverse cross-sectional plane, so as to provide a sheet-like depletion region having a uniform thickness	Because the lower portion of the gate in Samsung's S-RCAT transistors is spherical, it is equally curved in two planes (the transverse cross-sectional plane and in the non-transverse cross-sectional plane). This curvature exists in the relevant portion, because it would result in a sheet-like depletion region having a uniform thickness and a smooth bottom boundary underlying the channel region and the source and drain regions, when the transistor is in a turned-off state.

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	and a smooth bottom boundary underlying the channel region and the source and drain regions, when the transistor is in a turned-off state.	
11	An insulated-gate field effect transistor according to claim 4 wherein the depth of the concave surface portion is set to a value which ranges between one and two times the depth of the source and drain regions.	As is plainly evident from the TEMs set forth above, the transistor formed in Samsung's DRAMs infringe dependent Claim 11 because the depth of the concave surface portion (running from the main surface to the bottom of the "Sphere Part") is more than one but less than two times the depth of the source/drain regions. The source/drain regions extend from the main surface level only as deep as the line labeled "Junction" in the S-RCAT TEM images set forth above.