

EXHIBIT F

United States Patent [19]
Cheng et al.



[11] **Patent Number:** 5,559,990
 [45] **Date of Patent:** Sep. 24, 1996

- [54] **MEMORIES WITH BURST MODE ACCESS**
 [75] **Inventors:** Pearl F. Cheng, Cupertino; Michael S. Briner, James C. Yu, both of San Jose, all of Calif.
 [73] **Assignee:** Advanced Micro Devices, Inc., Sunnyvale, Calif.
 [21] **Appl. No.:** 328,337
 [22] **Filed:** Oct. 24, 1994

Related U.S. Application Data

- [63] **Continuation of Ser. No. 836,667, Feb. 14, 1992, abandoned.**
 [51] **Int. Cl.⁶** G06F 12/00
 [52] **U.S. Cl.** 395/484; 395/421.07; 395/405; 364/DIG. 1; 363/230.04; 365/230.08
 [58] **Field of Search:** 395/425, 500, 395/484, 405, 421.07, 401, 481; 365/230, 230.04, 230.08, 238.5

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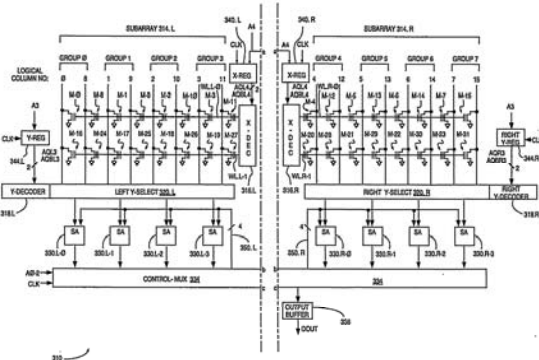
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ABSTRACT

To provide a boundaryless burst mode access, a memory array is divided into two or more subarrays. Each subarray has its own row and column decoders. The columns of each subarray are divided into groups. A sense amplifier circuit is provided for each group of columns. The column decoder of each subarray selects simultaneously one column from each group so that the memory locations in one row in the selected columns have consecutive addresses. The memory locations in the selected row and columns are read by the sense amplifier circuits. While the contents of the sense amplifier circuits of one subarray are transferred one by one to the memory output, consecutive memory locations of another subarray are read to the sense amplifier circuits. In some embodiments, to save power, sense amplifier circuits are disabled when their outputs are not transferred to the memory output.

23 Claims, 37 Drawing Sheets



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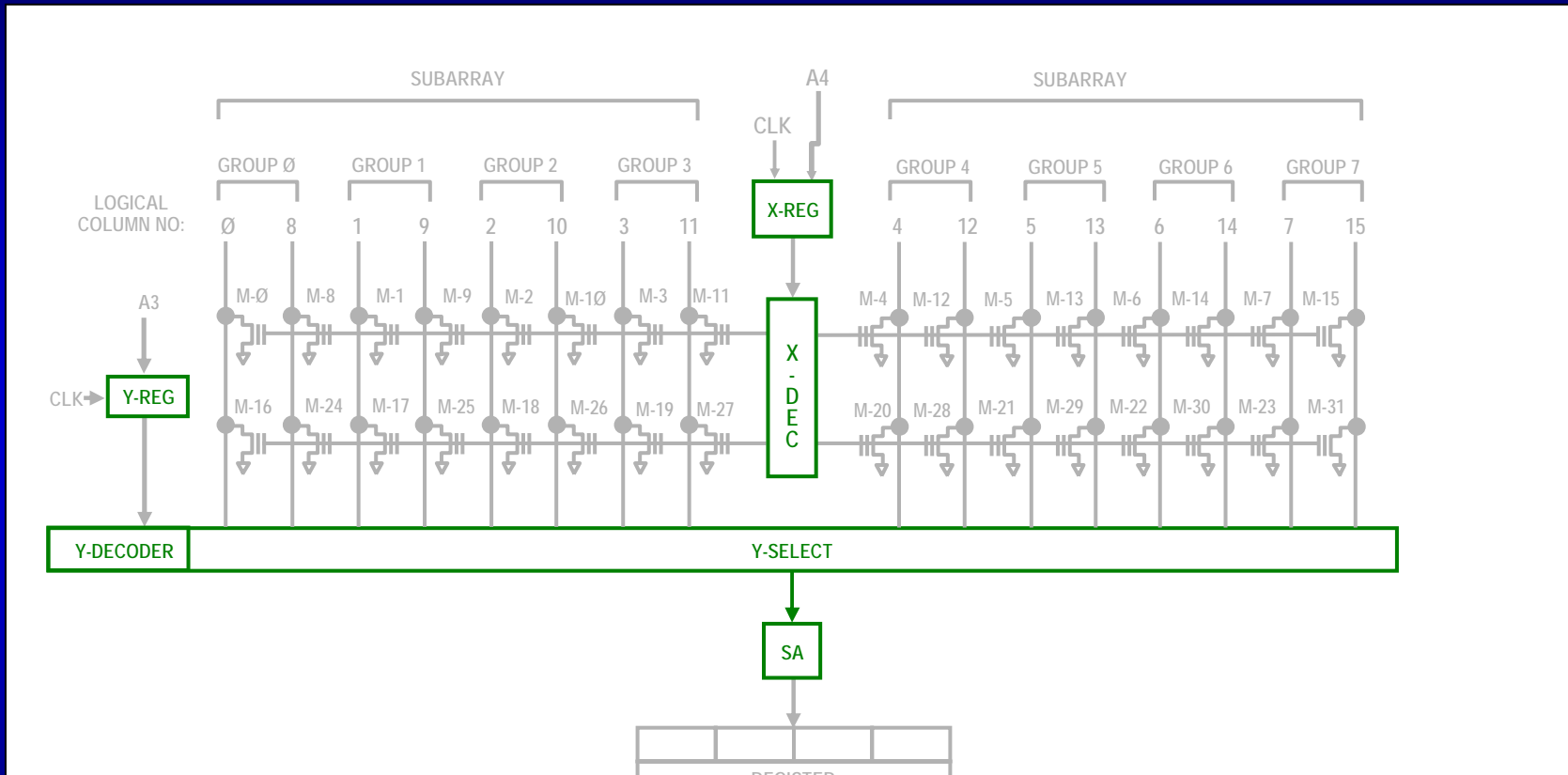
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Statement of the Invention

The invention is a memory with dedicated circuitry for each of its subarrays that maximizes the performance of memory by providing for continuous burst mode reads and selective deactivation of sense amplifiers.

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Prior Art: Shared Circuitry for Subarrays



Only one X-register, X-decoder, Y-register, Y-decoder and sense amplifier for both subarrays.

BUFFER
DOUT

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Dedicated Circuitry for Each Subarray

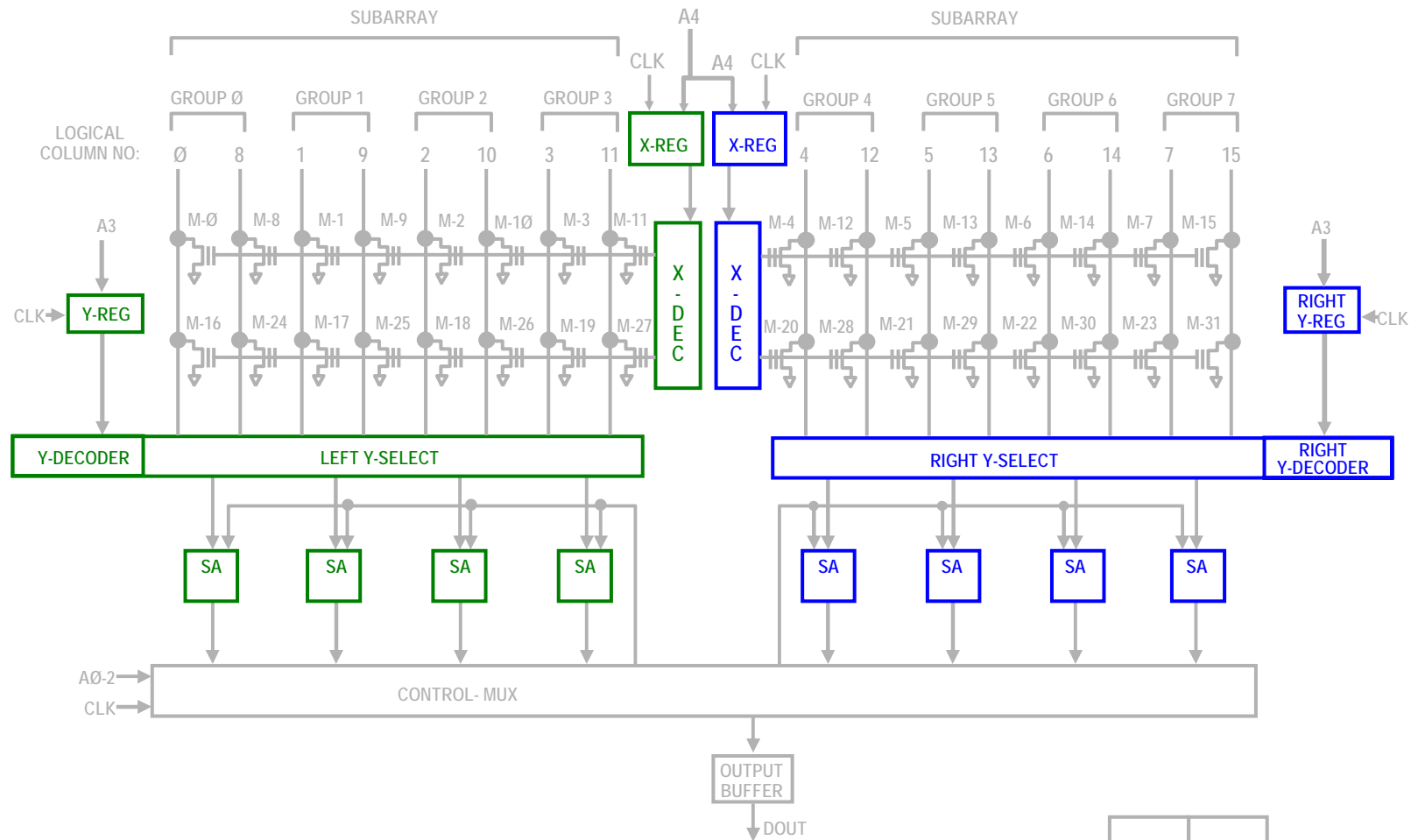
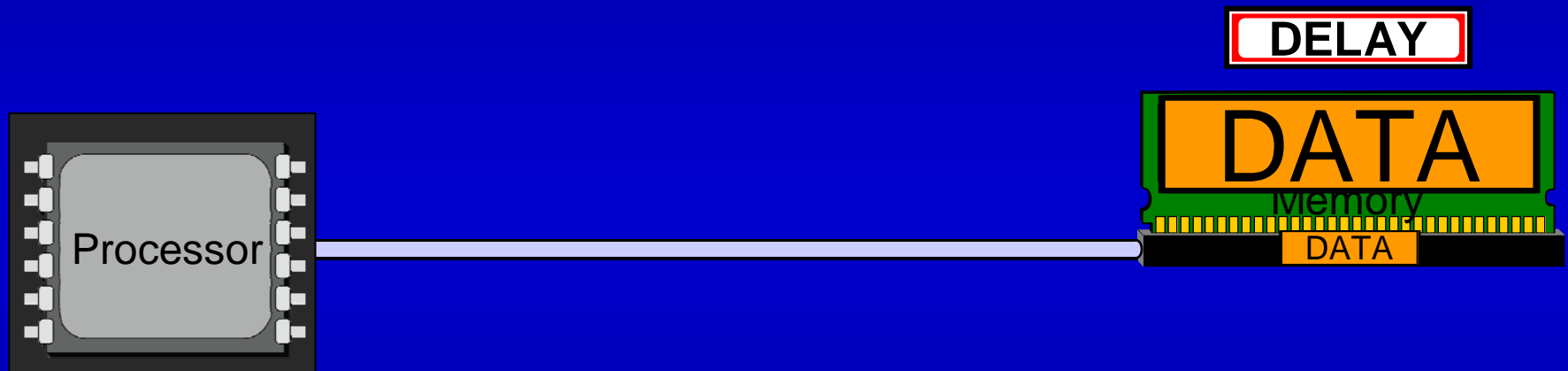


Fig. 3A

Fig. 3B

Fig. 3A	Fig. 3B
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Memory Access: Burst Mode Access



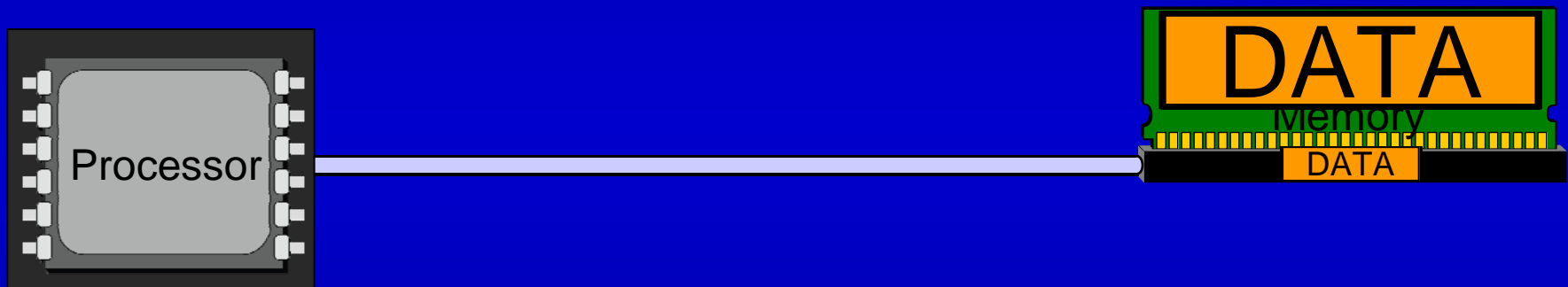
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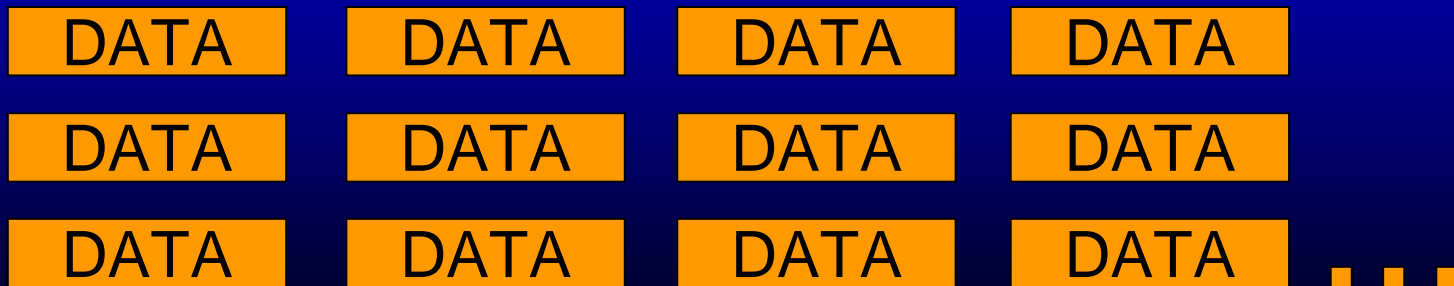
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Continuous Burst Mode



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Cheng: '990 Patent Continuous Burst Mode

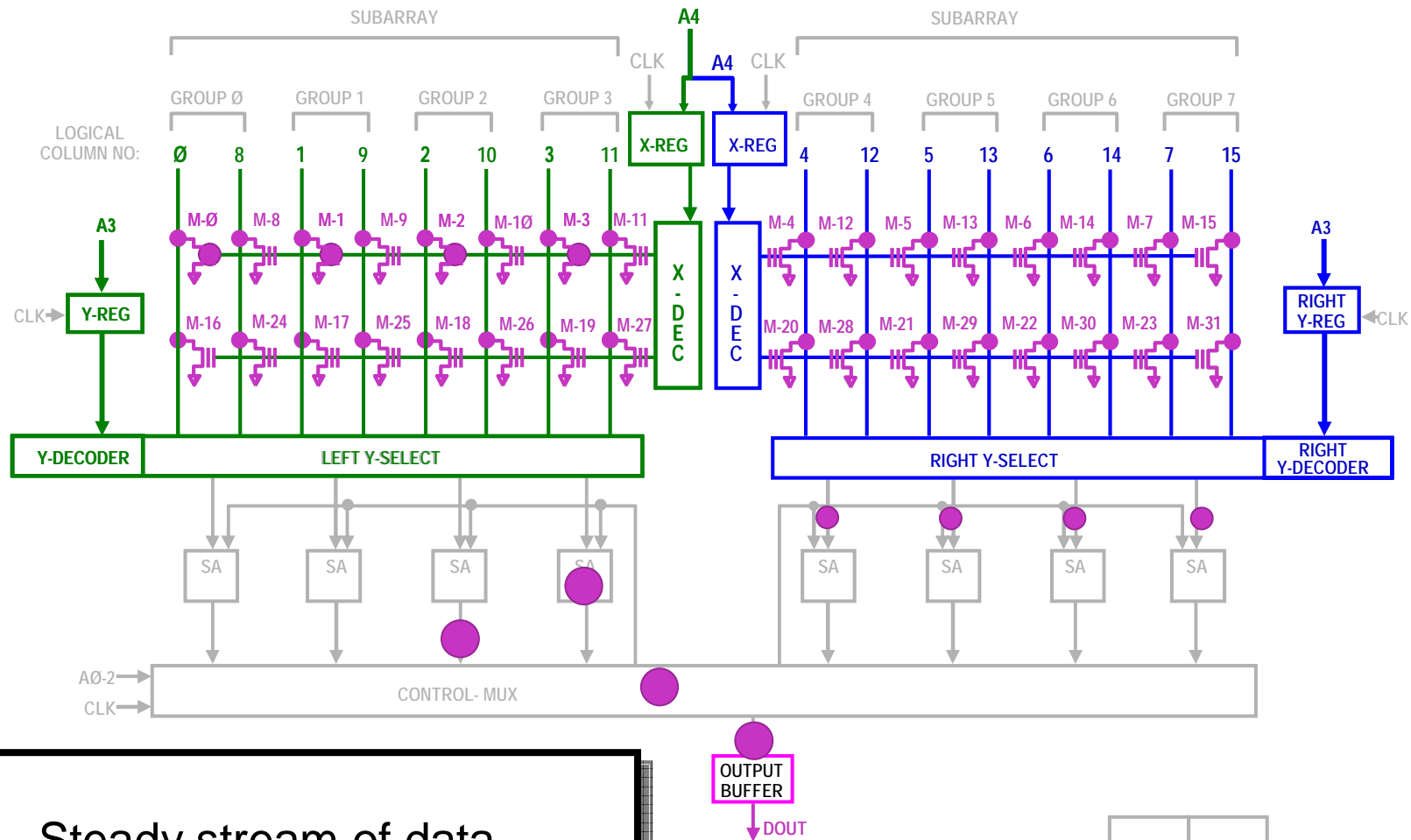
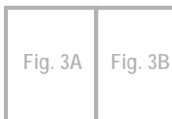


Fig. 3B



Steady stream of data.

Cheng: '990 Patent Sense Amplifier Deactivation

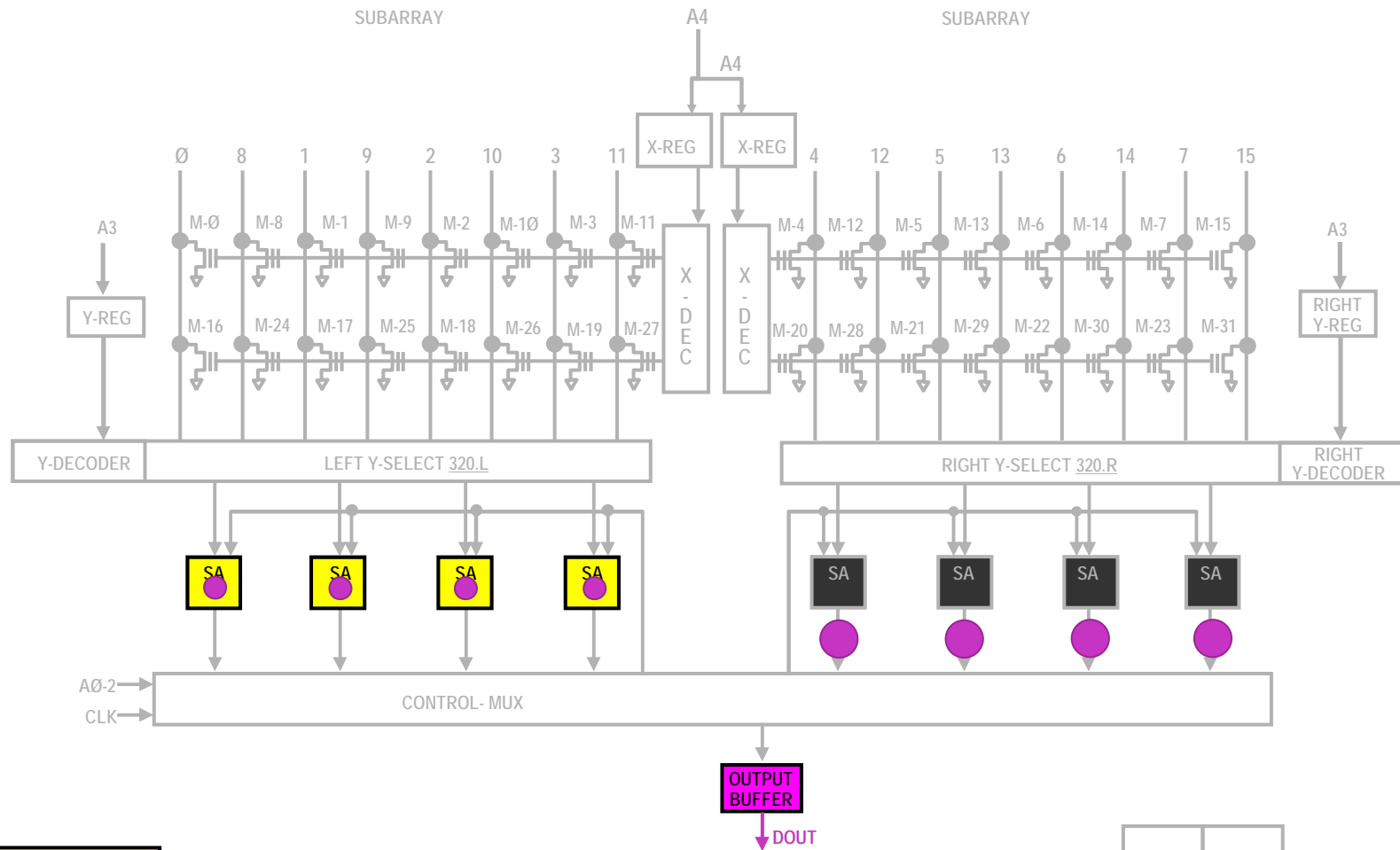


Fig. 3A

Fig. 3B

Fig. 3A	Fig. 3B
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Enabled
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