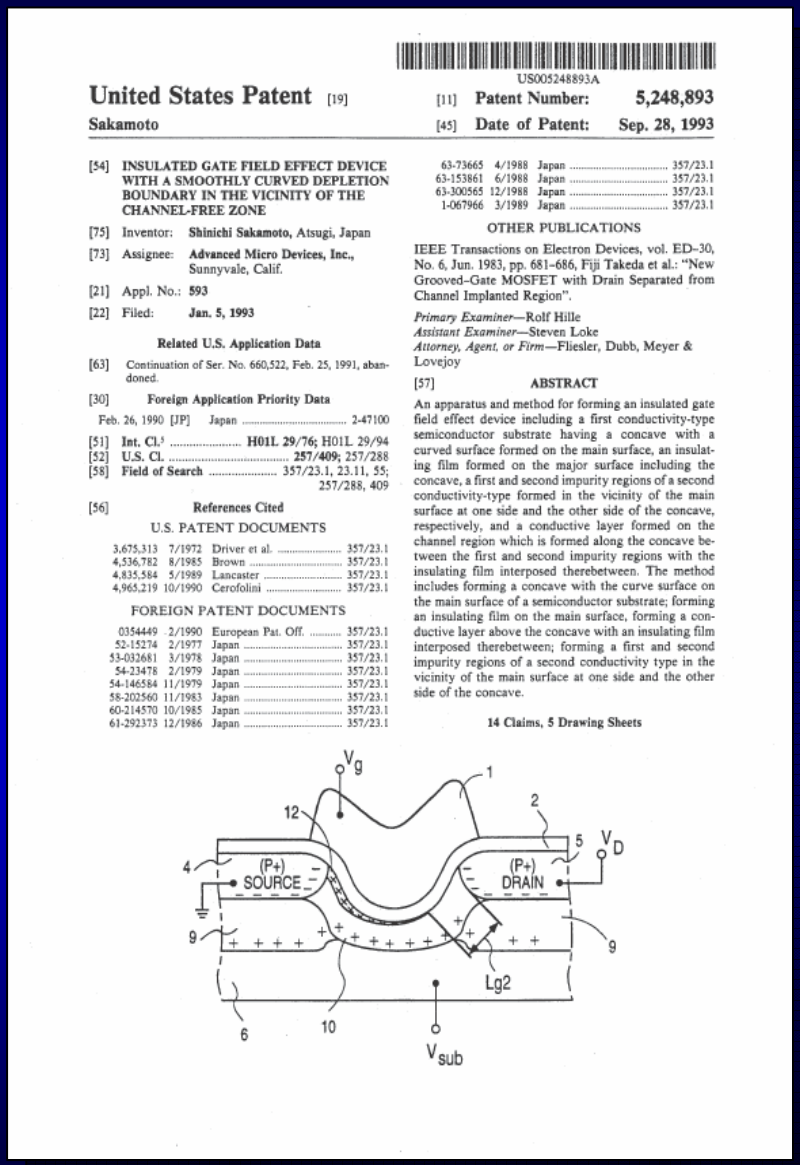
EXHIBIT G



US005248893A

United States Patent [19]

Sakamoto

[11] **Patent Number: 5,248,893**

[45] **Date of Patent: Sep. 28, 1993**

[54] **INSULATED GATE FIELD EFFECT DEVICE WITH A SMOOTHLY CURVED DEPLETION BOUNDARY IN THE VICINITY OF THE CHANNEL-FREE ZONE**

[75] Inventor: **Shinichi Sakamoto**, Atsugi, Japan

[73] Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, Calif.

[21] Appl. No.: **593**

[22] Filed: **Jan. 5, 1993**

Related U.S. Application Data

[63] Continuation of Ser. No. 660,522, Feb. 25, 1991, abandoned.

[30] **Foreign Application Priority Data**

Feb. 26, 1990 [JP] Japan 2-47100

[51] **Int. Cl.**[5] **H01L 29/76**; H01L 29/94

[52] **U.S. Cl.** **257/409**; 257/288

[58] **Field of Search** 357/23.1, 23.11, 55; 257/288, 409

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Primary Examiner—Rolf Hille
Assistant Examiner—Steven Loke
Attorney, Agent, or Firm—Fliesler, Dubb, Meyer & Lovejoy

[57] **ABSTRACT**

An apparatus and method for forming an insulated gate field effect device including a first conductivity-type semiconductor substrate having a concave with a curved surface formed on the main surface, an insulating film formed on the major surface including the concave, a first and second impurity regions of a second conductivity-type formed in the vicinity of the main surface at one side and the other side of the concave, respectively, and a conductive layer formed on the channel region which is formed along the concave between the first and second impurity regions with the insulating film interposed therebetween. The method includes forming a concave with the curve surface on the main surface of a semiconductor substrate; forming an insulating film on the main surface, forming a conductive layer above the concave with an insulating film interposed therebetween; forming a first and second impurity regions of a second conductivity type in the vicinity of the main surface at one side and the other side of the concave.

14 Claims, 5 Drawing Sheets

Sakamoto

U.S. Patent No. 5,248,893

Sakamoto: ’893 Patent

The Goal: Smaller Transistors

Designers seek to make smaller transistors. When they shrink them, the distance between the source and the drain shrinks, and so does the channel and the channel-free length.

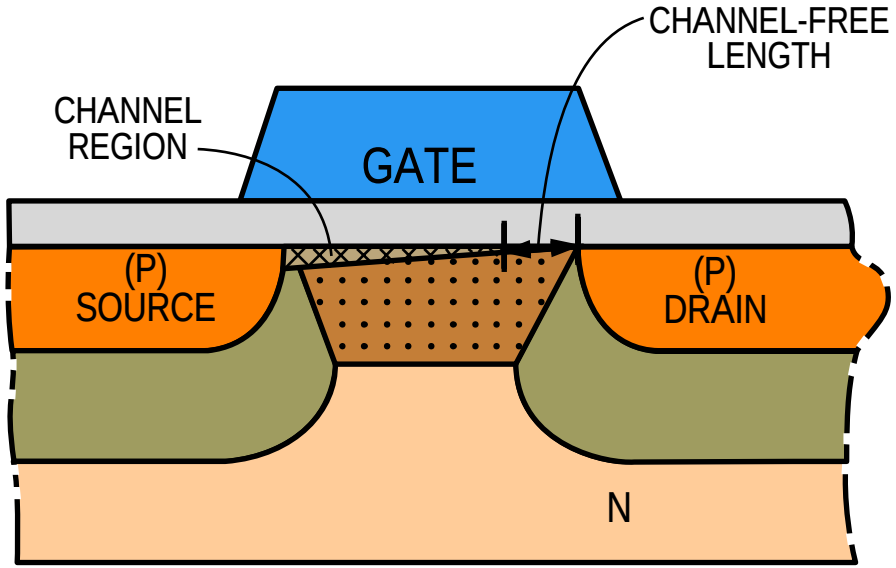


FIG. 9
PRIOR ART

Sakamoto: ’893 Patent

The Goal: Smaller Transistors

When the channel-free length gets too small:

1) current can flow when it should not;

2) current can escape from the channel region into other parts of the transistor. This causes the transistor to degrade to the point that it stops functioning.

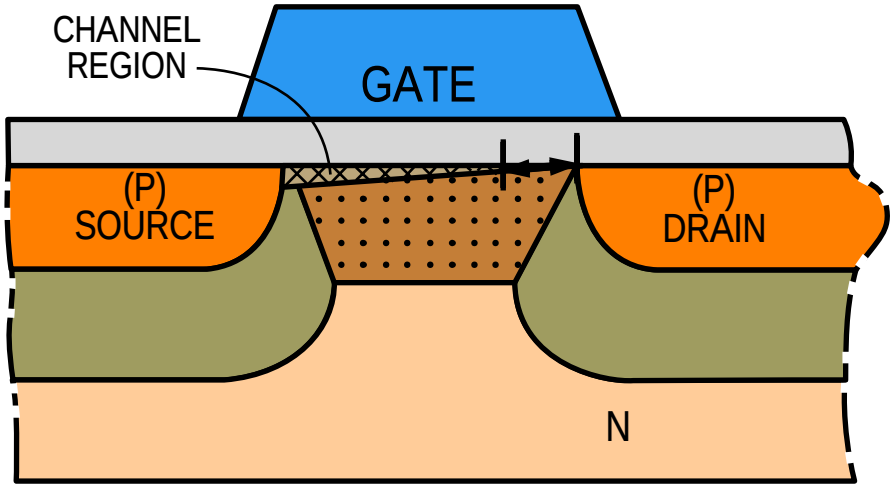


FIG. 9
PRIOR ART

Sakamoto: ’893 Patent
Invention

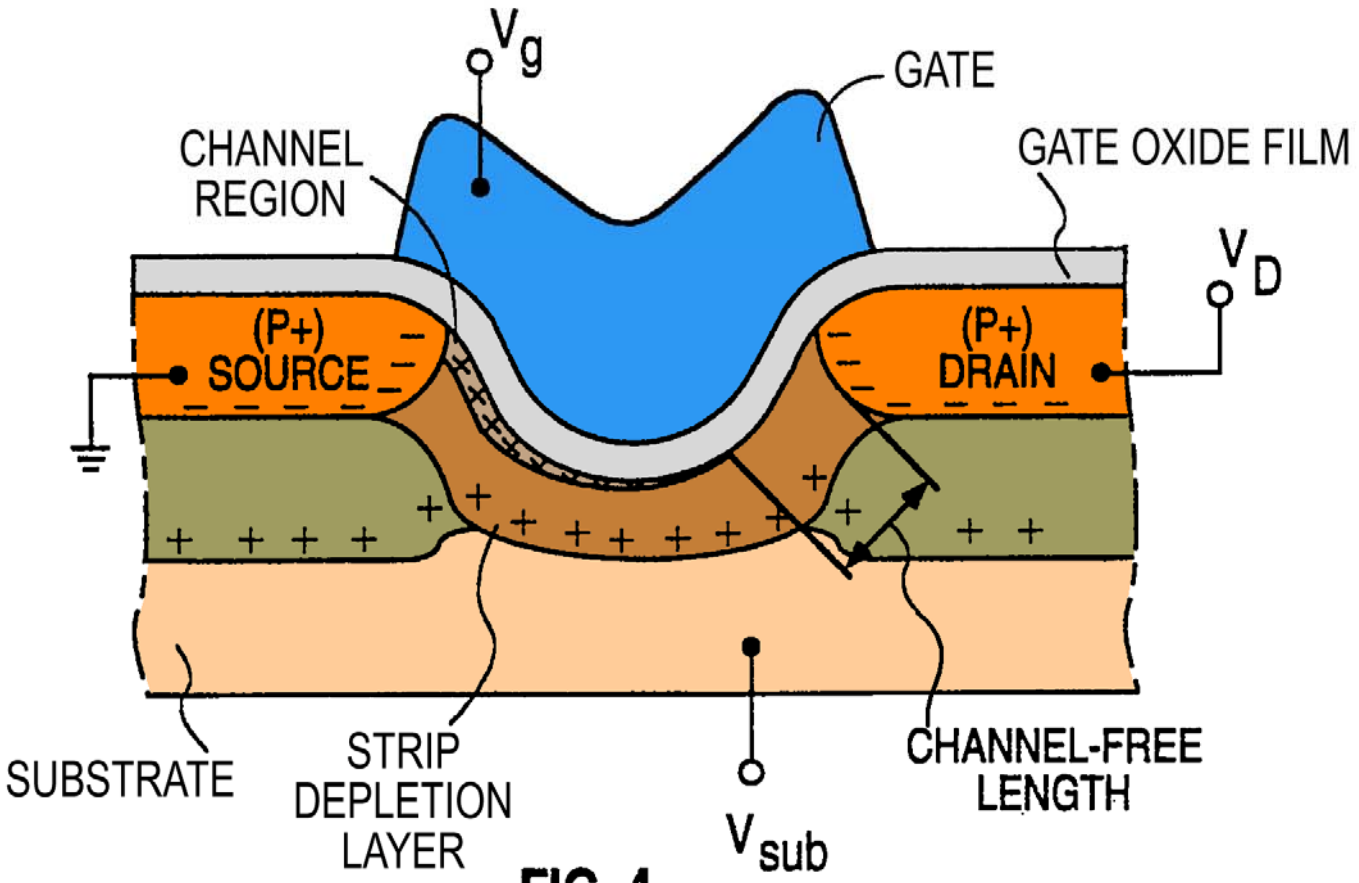
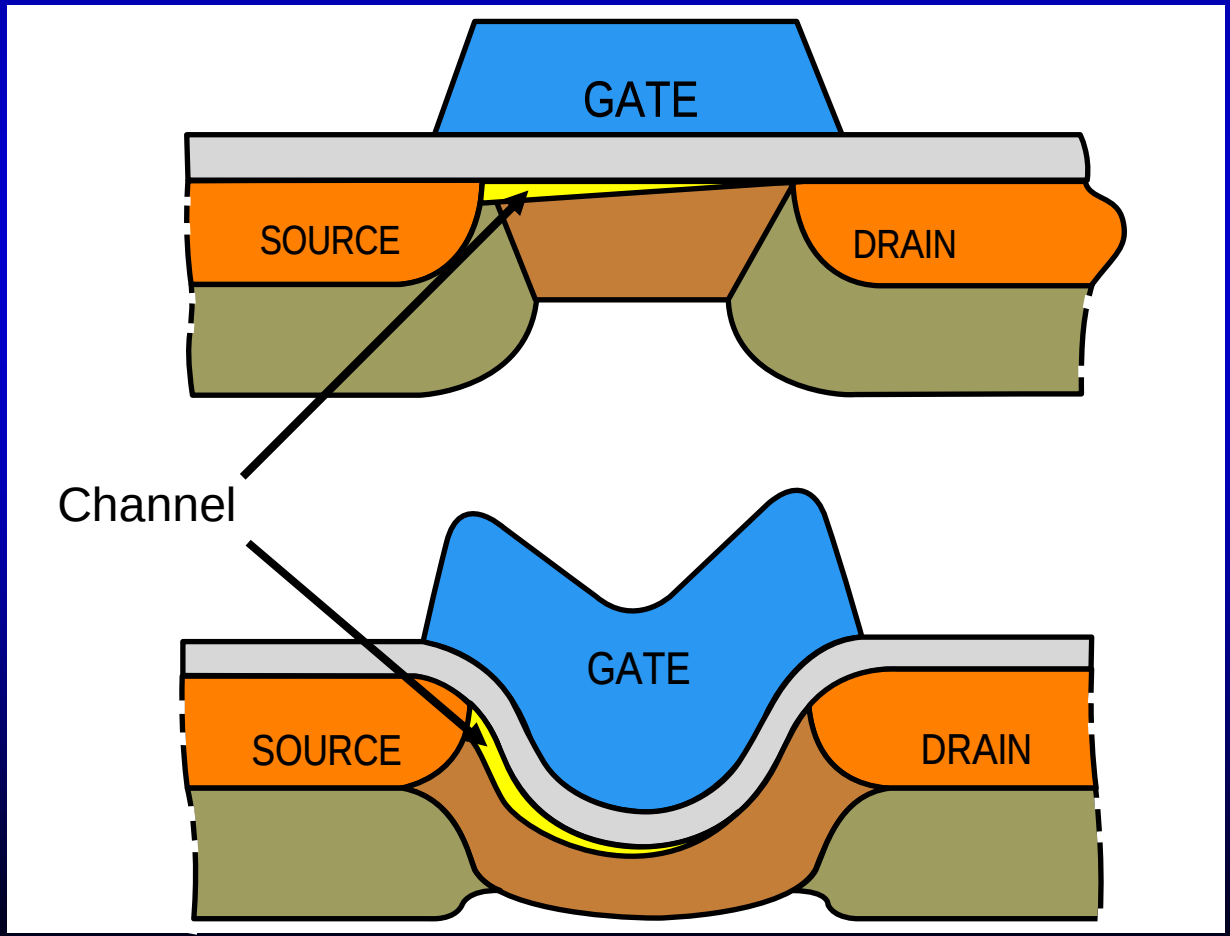


FIG. 4

Sakamoto: ’893 Patent

Using a curved, recessed gate to create a longer channel without increasing the size of the transistor.



Prior Art

Invention