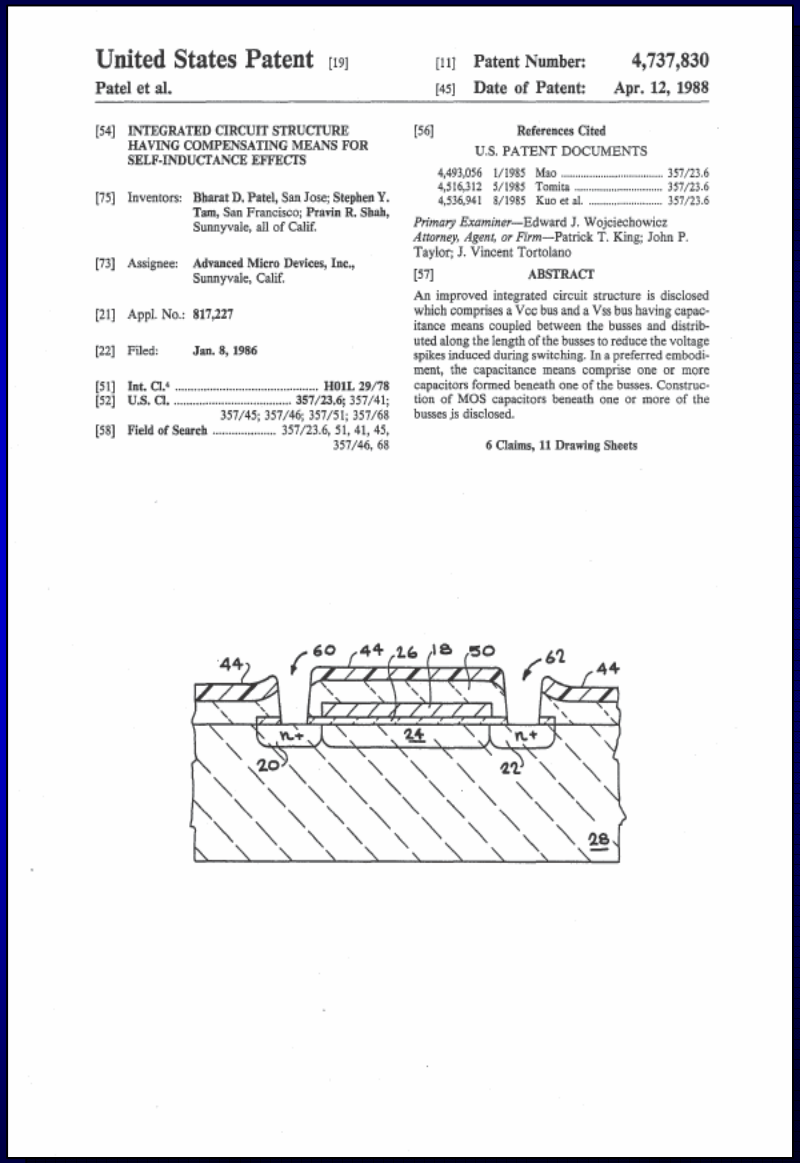
EXHIBIT H



United States Patent [19]

Patel et al.

[11] **Patent Number: 4,737,830**

[45] **Date of Patent: Apr. 12, 1988**

[54] **INTEGRATED CIRCUIT STRUCTURE HAVING COMPENSATING MEANS FOR SELF-INDUCTANCE EFFECTS**

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[73] Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, Calif.

[21] Appl. No.: **817,227**

[22] Filed: **Jan. 8, 1986**

[51] **Int. Cl.**[4] **H01L 29/78**

[52] **U.S. Cl.** **357/23.6**; 357/41; 357/45; 357/46; 357/51; 357/68

[58] **Field of Search** 357/23.6, 51, 41, 45, 357/46, 68

[56] **References Cited**

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[57] **ABSTRACT**

An improved integrated circuit structure is disclosed which comprises a Vcc bus and a Vss bus having capacitance means coupled between the busses and distributed along the length of the busses to reduce the voltage spikes induced during switching. In a preferred embodiment, the capacitance means comprise one or more capacitors formed beneath one of the busses. Construction of MOS capacitors beneath one or more of the busses is disclosed.

6 Claims, 11 Drawing Sheets

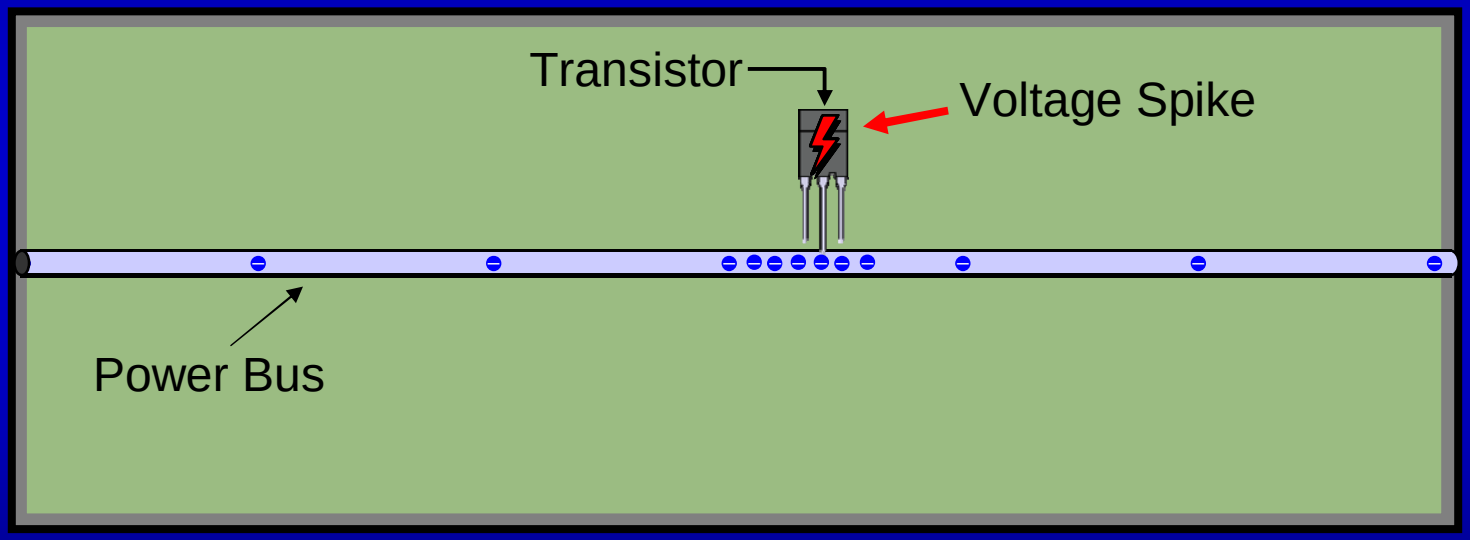
Patel

U.S. Patent No.

4,737,830

Patel: ’830 Patent

Voltage Spikes Damaged Transistors Attached to Power Bus



Patel: ’830 Patent

Statement of the Invention

Adding capacitance underneath the busses to reduce voltage spikes. The gate area of the capacitor is segmented, with each segment having a connection to the bus to improve efficiency and reliability.

Patel: ’830 Patent
Invention