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Time-Critical Software Deceleration in an FCCM

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Proceedings of the 12th Annual IEEE Symposium on Field-Programmable Custom Computing Machines [table of contents](#)
 Pages: 3 - 12
 Year of Publication: 2004
 ISBN:0-7695-2230-0

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Publisher IEEE Computer Society Washington, DC, USA

Bibliometrics Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Citation Count: 3

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↑ ABSTRACT

In this paper, we explore two important latency issues associated with using an embedded processor as an assistant to programmable logic within a logic-centric system implemented on a platform FPGA. The context is that of the 'software decelerator' - a term introduced by the authors in 2003 to describe a logic-centric counterpart of the familiar hardware accelerator. We first focus on minimizing latency in the logic-processor interface, introducing an efficient interrupt-driven control mechanism. Then, in the context of a case study on packet address lookup, we focus on minimizing latency in memory interfaces, using the processor's hardware cache mechanism for assistance.

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Bibliometrics: publication history

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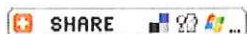
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