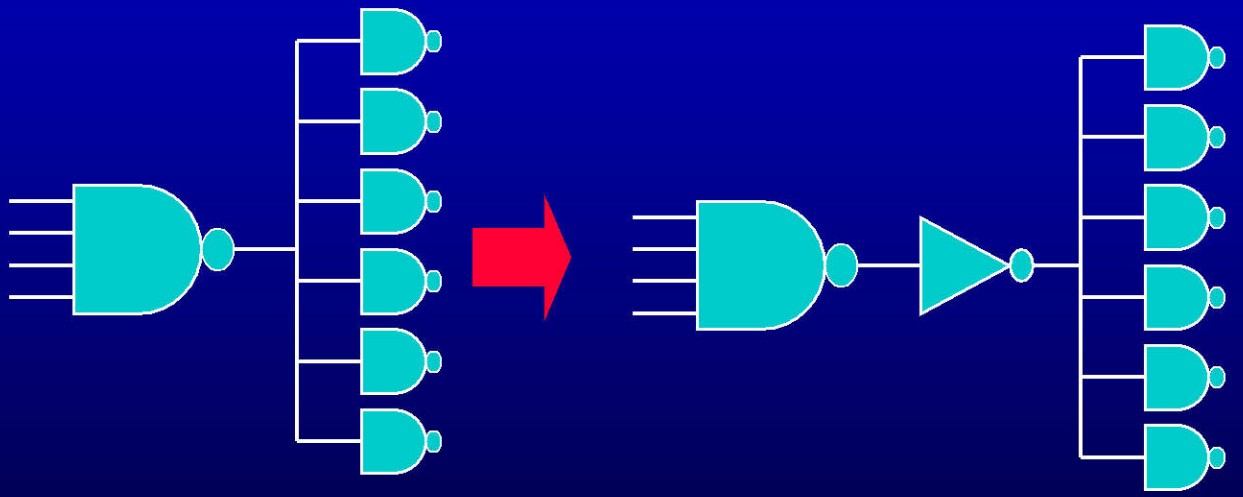
Exhibit F
(6 of 12)

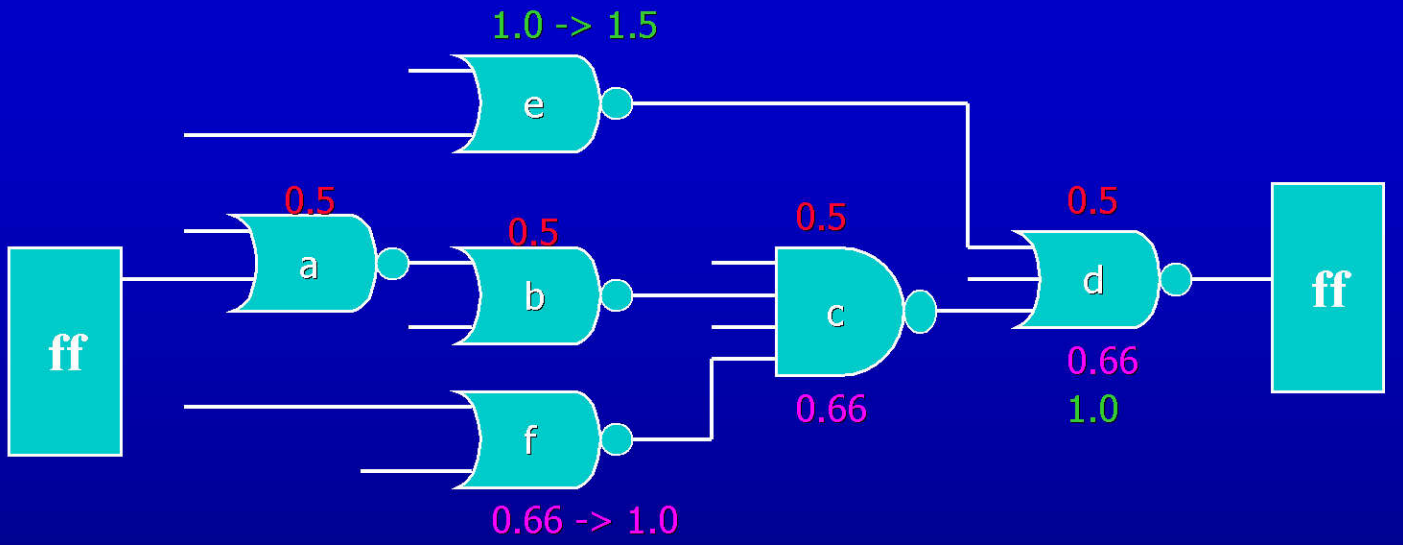
Choosing the right number of stages (logical depth)

- Logic depth is determined by synthesis
- pre-layout: Adding buffers to high-fanout nets generally improves speed due to the high inverter gain.



- During layout: Adding inverters for long-wire delay minimization.
- The optimum depth depends on the *path effort* and process parameters.
- Not very critical: being 50% off results in less than 10% delay penalty

Assigning delays



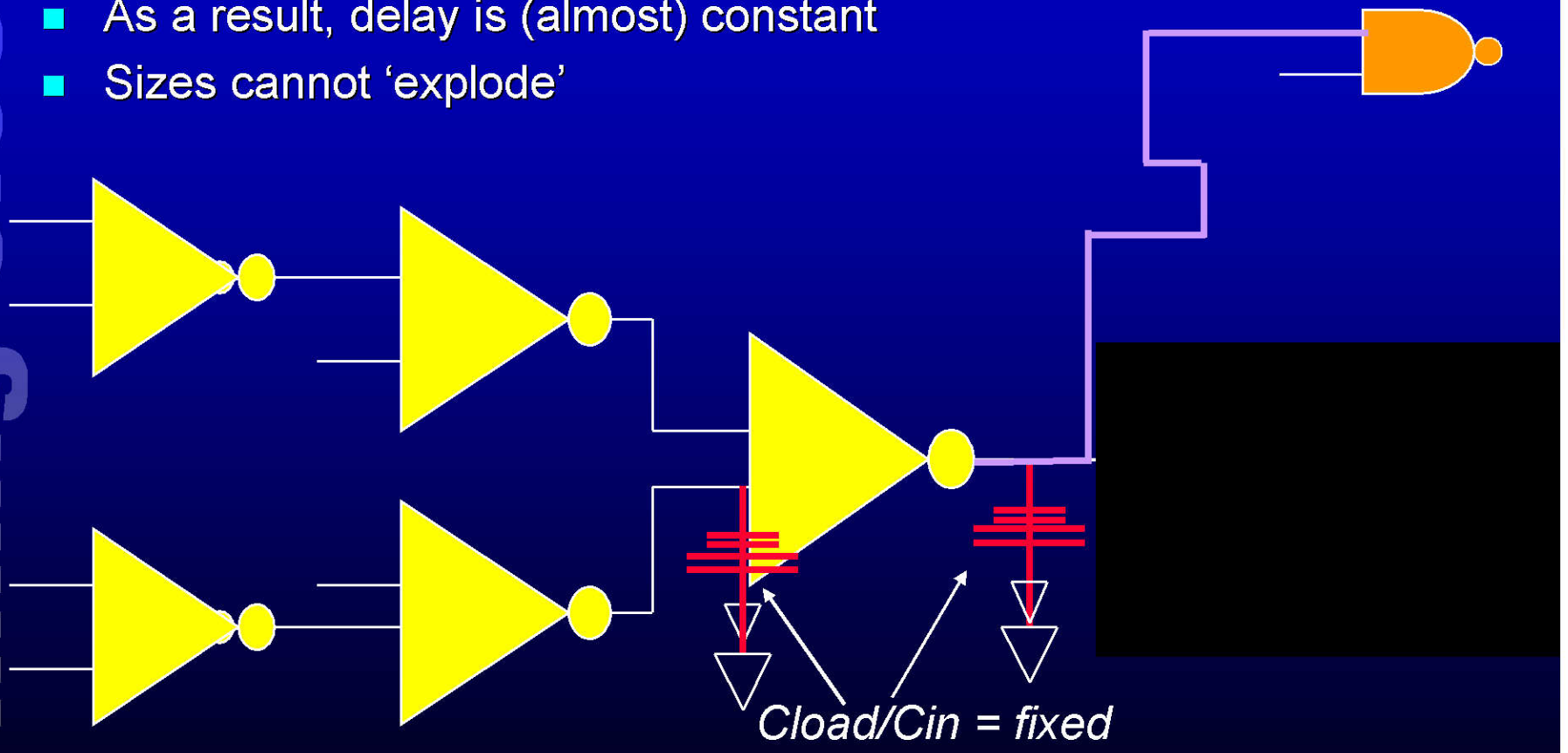
- Timing constraints determine the delay budget:
  - e.g. $d_{abcd} < 2.0ns$, $d_{ed} < 2.0ns$, $d_{fcd} < 2.0ns$
- Spread delay budgets evenly over all paths
  - If paths collide, take the smallest delay budget
  - Relax others
- Translate delay budgets into gain.

Pre-layout sign-off

- If there is no feasible gain assignment, the sizes literally ‘explode’.

Keeping delay constant during layout

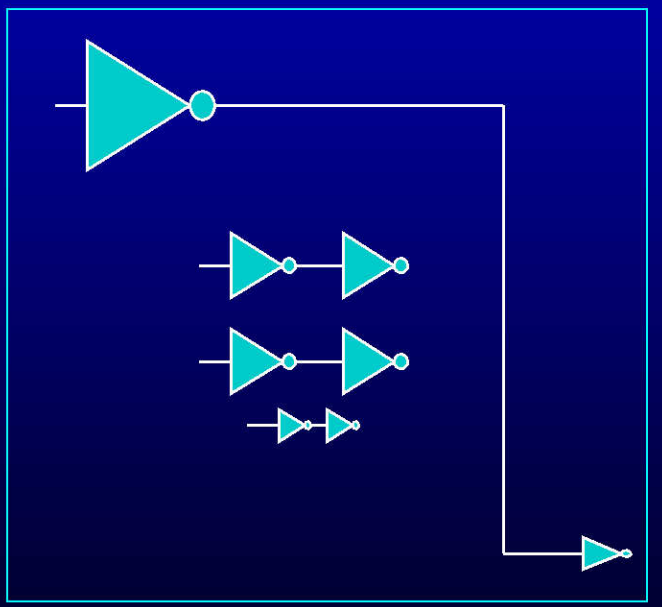
- The gain ratio (=Cload/Cin) is maintained is placement
- Sizes change *during* placement.
- As a result, delay is (almost) constant
- Sizes cannot ‘explode’



Timing closure

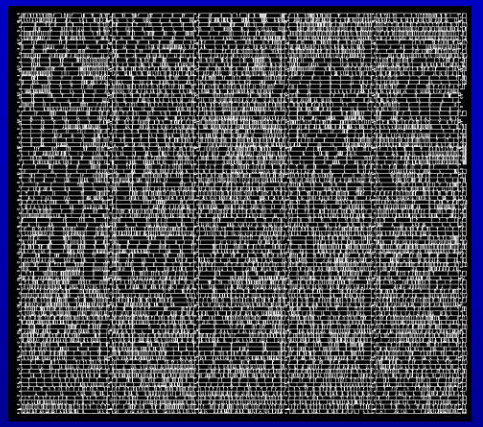
Sizing driven placement

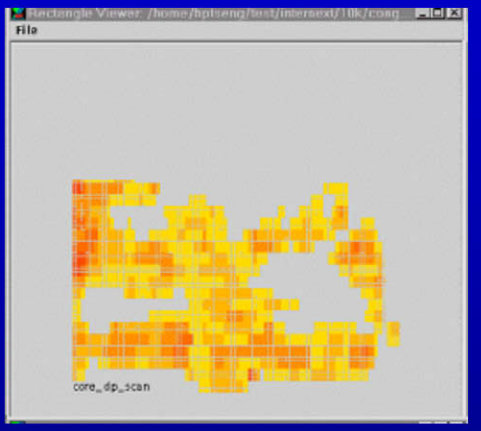
- Gate sizes change gradually during placement to keep delay constant.
- Placer much be able to cope with the net list changes due to buffering, cloning, restructuring, clock insertion, etc.
- .. while producing a routable result.



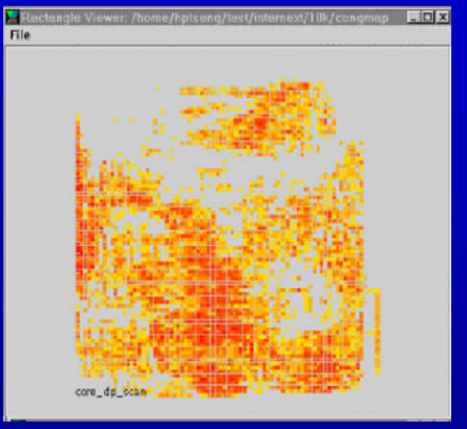
Automatic Congestion Handling

- During placement

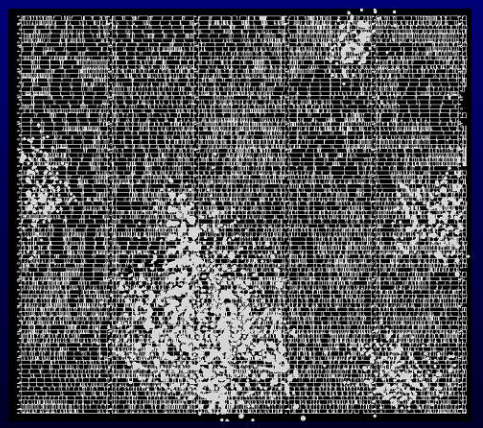




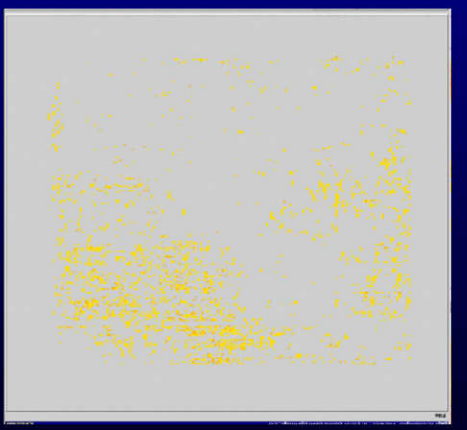
Routing Congestion



Utilization



Routing Congestion



Utilization

Timing closure

What happened

.... at the logical-physical boundary?

Timing closure

Conventional synthesis

- Cell Area fixed
- Delay is a gamble
- Worst case delay determines timing (max)
- Iterate to make ends meet.
- After timing finally closes, many gates will be too big:
  - waste of area
  - waste of power

Gain based synthesis

- Delay fixed
- Cell Area unknown
- Sum of areas determines chip size. (Additive)
- No iterations required
- Each gate has exactly the right drive strength:
  - Not too little (fanout violation, timing fails)
  - Not too much (waste of area)