# 1. Pin Information

This chapter describes, lists, and illustrates the CY8C21x34 PSoC device pins and pinout configurations.

## 1.1 Pinouts

The CY8C21x34 PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a "P") is capable of Digital IO and connection to the common analog bus. However, Vss, Vdd, SMP, and XRES are not capable of Digital IO.

### 1.1.1 16-Pin Part Pinout

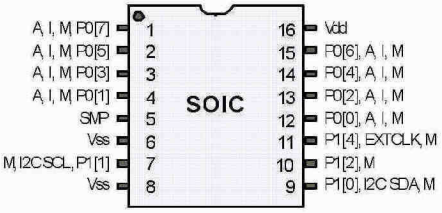
**Table 1-1. 16-Pin Part Pinout (SOIC)**

| Pin No. | Type | | Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | IO | I, M | P0[7] | Analog column mux input. |
| 2 | IO | I, M | P0[5] | Analog column mux input. |
| 3 | IO | I, M | P0[3] | Analog column mux input, integrating input. |
| 4 | IO | I, M | P0[1] | Analog column mux input, integrating input. |
| 5 | Power | | SMP | Switch Mode Pump (SMP) connection to required external components. |
| 6 | Power | | Vss | Ground connection. |
| 7 | IO | M | P1[1] | I2C Serial Clock (SCL), ISSP-SCLK*. |
| 8 | Power | | Vss | Ground connection. |
| 9 | IO | M | P1[0] | I2C Serial Data (SDA), ISSP-SDATA*. |
| 10 | IO | M | P1[2] | |
| 11 | IO | M | P1[4] | Optional External Clock Input (EXTCLK). |
| 12 | IO | I, M | P0[0] | Analog column mux input. |
| 13 | IO | I, M | P0[2] | Analog column mux input. |
| 14 | IO | I, M | P0[4] | Analog column mux input. |
| 15 | IO | I, M | P0[6] | Analog column mux input. |
| 16 | Power | | Vdd | Supply voltage. |

**LEGEND** A = Analog, I = Input, O = Output, and M = Analog Mux Input.

* These are the ISSP pins, which are not High Z at POR (Power On Reset). See the PSoC Mixed-Signal Array Technical Reference Manual for details.

**CY8C21234 16-Pin PSoC Device**



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### 1.1.2 20-Pin Part Pinout

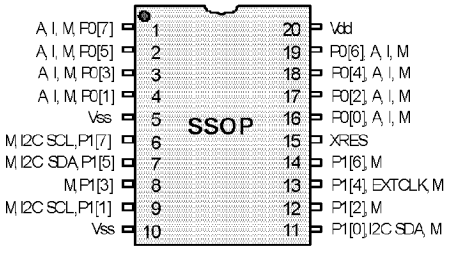
**Table 1-2. 20-Pin Part Pinout (SSOP)**

| Pin No. | Type | | Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | IO | I, M | P0[7] | Analog column mux input. |
| 2 | IO | I, M | P0[5] | Analog column mux input. |
| 3 | IO | I, M | P0[3] | Analog column mux input, integrating input. |
| 4 | IO | I, M | P0[1] | Analog column mux input, integrating input. |
| 5 | Power | | Vss | Ground connection. |
| 6 | IO | M | P1[7] | I2C Serial Clock (SCL). |
| 7 | IO | M | P1[5] | I2C Serial Data (SDA). |
| 8 | IO | M | P1[3] | |
| 9 | IO | M | P1[1] | I2C Serial Clock (SCL), ISSP-SCLK*. |
| 10 | Power | | Vss | Ground connection. |
| 11 | IO | M | P1[0] | I2C Serial Data (SDA), ISSP-SDATA*. |
| 12 | IO | M | P1[2] | |
| 13 | IO | M | P1[4] | Optional External Clock Input (EXT-CLK). |
| 14 | IO | M | P1[6] | |
| 15 | Input | | XRES | Active high external reset with internal pull down. |
| 16 | IO | I, M | P0[0] | Analog column mux input. |
| 17 | IO | I, M | P0[2] | Analog column mux input. |
| 18 | IO | I, M | P0[4] | Analog column mux input. |
| 19 | IO | I, M | P0[6] | Analog column mux input. |
| 20 | Power | | Vdd | Supply voltage. |

**LEGEND** A = Analog, I = Input, O = Output, and M = Analog Mux Input.

* These are the ISSP pins, which are not High Z at POR (Power On Reset). See the PSoC Mixed-Signal Array Technical Reference Manual for details.

**CY8C21334 20-Pin PSoC Device**



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### 1.1.3 28-Pin Part Pinout

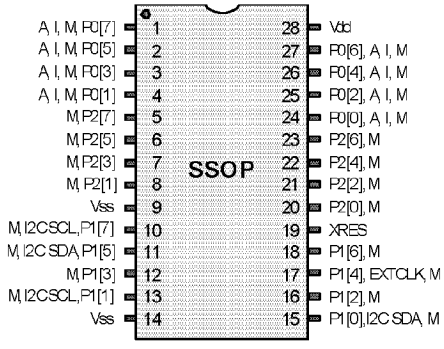
**Table 1-3. 28-Pin Part Pinout (SSOP)**

| Pin No. | Type | | Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | IO | I, M | P0[7] | Analog column mux input. |
| 2 | IO | I, M | P0[5] | Analog column mux input and column output. |
| 3 | IO | I, M | P0[3] | Analog column mux input and column output, integrating input. |
| 4 | IO | I, M | P0[1] | Analog column mux input, integrating input. |
| 5 | IO | M | P2[7] | |
| 6 | IO | M | P2[5] | |
| 7 | IO | I, M | P2[3] | Direct switched capacitor block input. |
| 8 | IO | I, M | P2[1] | Direct switched capacitor block input. |
| 9 | Power | | Vss | Ground connection. |
| 10 | IO | M | P1[7] | I2C Serial Clock (SCL). |
| 11 | IO | M | P1[5] | I2C Serial Data (SDA). |
| 12 | IO | M | P1[3] | |
| 13 | IO | M | P1[1] | I2C Serial Clock (SCL), ISSP-SCLK*. |
| 14 | Power | | Vss | Ground connection. |
| 15 | IO | M | P1[0] | I2C Serial Data (SDA), ISSP-SDATA*. |
| 16 | IO | M | P1[2] | |
| 17 | IO | M | P1[4] | Optional External Clock Input (EXT-CLK). |
| 18 | IO | M | P1[6] | |
| 19 | Input | | XRES | Active high external reset with internal pull down. |
| 20 | IO | I, M | P2[0] | Direct switched capacitor block input. |
| 21 | IO | I, M | P2[2] | Direct switched capacitor block input. |
| 22 | IO | M | P2[4] | |
| 23 | IO | M | P2[6] | |
| 24 | IO | I, M | P0[0] | Analog column mux input. |
| 25 | IO | I, M | P0[2] | Analog column mux input. |
| 26 | IO | I, M | P0[4] | Analog column mux input |
| 27 | IO | I, M | P0[6] | Analog column mux input. |
| 28 | Power | | Vdd | Supply voltage. |

**LEGEND** A: Analog, I: Input, O = Output, and M = Analog Mux Input.

* These are the ISSP pins, which are not High Z at POR (Power On Reset). See the PSoC Mixed-Signal Array Technical Reference Manual for details.

**CY8C21534 28-Pin PSoC Device**



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### 1.1.4 32-Pin Part Pinout

**Table 1-4. 32-Pin Part Pinout (QFN**)**

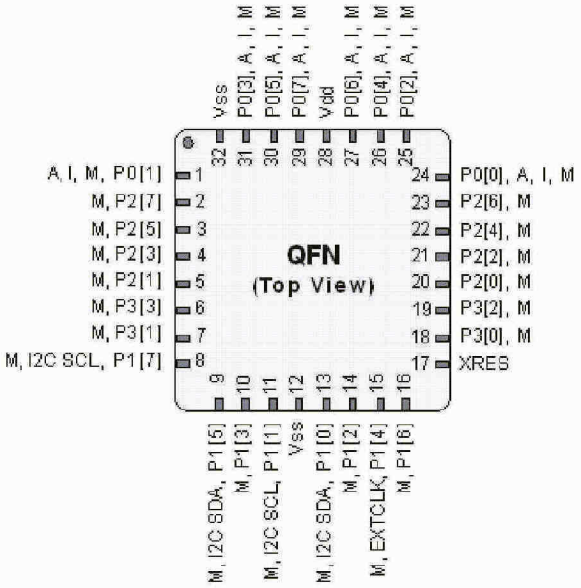
| Pin No. | Type | | Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | IO | I, M | P0[1] | Analog column mux input, integrating input. |
| 2 | IO | M | P2[7] | |
| 3 | IO | M | P2[5] | |
| 4 | IO | M | P2[3] | |
| 5 | IO | M | P2[1] | |
| 6 | IO | M | P3[3] | In CY8C21434 part. |
| 6 | Power | | SMP | Switch Mode Pump (SMP) connection to required external components in CY8C21634 part. |
| 7 | IO | M | P3[1] | In CY8C21434 part. |
| 7 | Power | | Vss | Ground connection in CY8C21634 part. |
| 8 | IO | M | P1[7] | I2C Serial Clock (SCL). |
| 9 | IO | M | P1[5] | I2C Serial Data (SDA). |
| 10 | IO | M | P1[3] | |
| 11 | IO | M | P1[1] | I2C Serial Clock (SCL), ISSP-SCLK*. |
| 12 | Power | | Vss | Ground connection. |
| 13 | IO | M | P1[0] | I2C Serial Data (SDA), ISSP-SDATA*. |
| 14 | IO | M | P1[2] | |
| 15 | IO | M | P1[4] | Optional External Clock Input (EXTCLK). |
| 16 | IO | M | P1[6] | |
| 17 | Input | | XRES | Active high external reset with internal pull down. |
| 18 | IO | M | P3[0] | |
| 19 | IO | M | P3[2] | |
| 20 | IO | M | P2[0] | |
| 21 | IO | M | P2[2] | |
| 22 | IO | M | P2[4] | |
| 23 | IO | M | P2[6] | |
| 24 | IO | I, M | P0[0] | Analog column mux input. |
| 25 | IO | I, M | P0[2] | Analog column mux input. |
| 26 | IO | I, M | P0[4] | Analog column mux input. |
| 27 | IO | I, M | P0[6] | Analog column mux input. |
| 28 | Power | | Vdd | Supply voltage. |
| 29 | IO | I, M | P0[7] | Analog column mux input. |
| 30 | IO | I, M | P0[5] | Analog column mux input. |
| 31 | IO | I, M | P0[3] | Analog column mux input, integrating input. |
| 32 | Power | | Vss | Ground connection. |

**LEGEND** A = Analog, I = Input, O = Output, and M = Analog Mux Input.

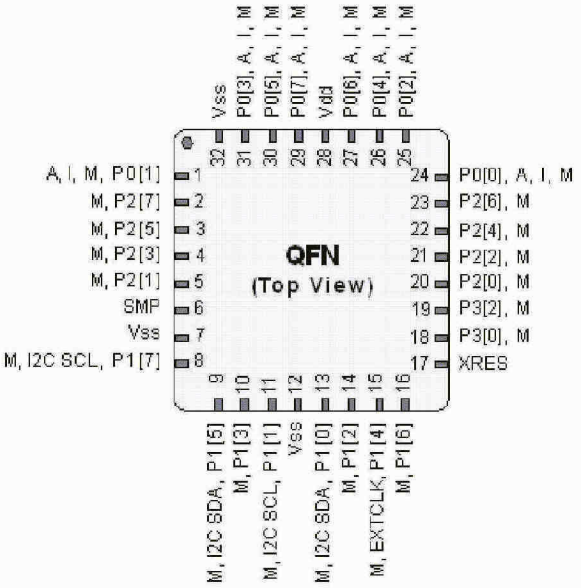
* These are the ISSP pins, which are not High Z at POR (Power On Reset). See the PSoC Mixed-Signal Array Technical Reference Manual for details.

** The center pad on the QFN package should be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.

**CY8C21434 32-Pin PSoC Device**




**CY8C21634 32-Pin PSoC Device**



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### 1.1.5 56-Pin Part Pinout

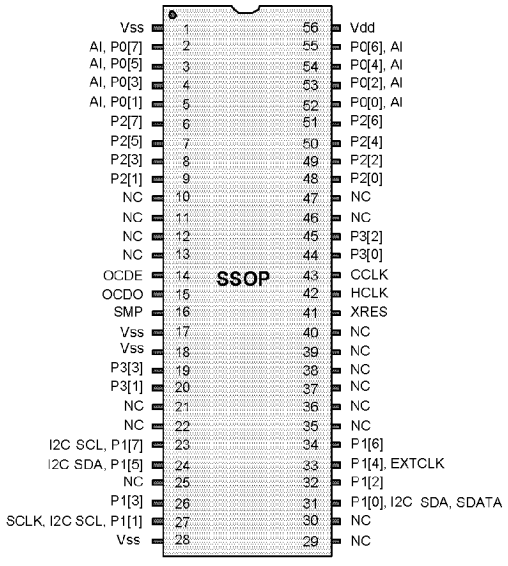
The 56-pin SSOP part is for the CY8C21001 On-Chip Debug (OCD) PSoC device.

**Note** This part is only used for in-circuit debugging. It is NOT available for production.

**Table 1-5. 56-Pin Part Pinout (SSOP)**

| Pin No. | Type | | Pin Name | Description |
|---|---|---|---|---|
| | Digital | Analog | | |
| 1 | Power | | Vss | Ground connection. |
| 2 | IO | I | P0[7] | Analog column mux input. |
| 3 | IO | I | P0[5] | Analog column mux input and column output. |
| 4 | IO | I | P0[3] | Analog column mux input and column output. |
| 5 | IO | I | P0[1] | Analog column mux input. |
| 6 | IO | | P2[7] | |
| 7 | IO | | P2[5] | |
| 8 | IO | I | P2[3] | Direct switched capacitor block input. |
| 9 | IO | I | P2[1] | Direct switched capacitor block input. |
| 10 | | | NC | No connection. |
| 11 | | | NC | No connection.. |
| 12 | | | NC | No connection. |
| 13 | | | NC | No connection.. |
| 14 | OCD | | OCDE | OCD even data IO. |
| 15 | OCD | | OCDO | OCD odd data output. |
| 16 | Power | | SMP | Switch Mode Pump (SMP) connection to required external components. |
| 17 | Power | | Vss | Ground connection. |
| 18 | Power | | Vss | Ground connection. |
| 19 | IO | | P3[3] | |
| 20 | IO | | P3[1] | |
| 21 | | | NC | No connection. |
| 22 | | | NC | No connection.. |
| 23 | IO | | P1[7] | I2C Serial Clock (SCL). |
| 24 | IO | | P1[5] | I2C Serial Data (SDA). |
| 25 | | | NC | No connection. |
| 26 | IO | | P1[3] | $I_{FMTEST}$. |
| 27 | IO | | P1[1] | Crystal Input (XTALin), I2C Serial Clock (SCL), ISSP-SCLK*. |
| 28 | Power | | Vss | Ground connection. |
| 29 | | | NC | No connection. |
| 30 | | | NC | No connection.. |
| 31 | IO | | P1[0] | Crystal Output (XTALout), I2C Serial Data (SDA), ISSP-SDATA*. |
| 32 | IO | | P1[2] | $V_{FMTEST}$. |
| 33 | IO | | P1[4] | Optional External Clock Input (EXTCLK). |
| 34 | IO | | P1[6] | |
| 35 | | | NC | No connection.. |
| 36 | | | NC | No connection. |
| 37 | | | NC | No connection.. |
| 38 | | | NC | No connection. |
| 39 | | | NC | No connection.. |
| 40 | | | NC | No connection.. |
| 41 | Input | | XRES | Active high external reset with internal pull down. |
| 42 | OCD | | HCLK | OCD high-speed clock output. |
| 43 | OCD | | CCLK | OCD CPU clock output. |
| 44 | IO | | P3[0] | |
| 45 | IO | | P3[2] | |
| 46 | | | NC | No connection. |
| 47 | | | NC | No connection.. |

**CY8C21001 56-Pin PSoC Device**




**Not for Production**



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**Table 1-5. 56-Pin Part Pinout (SSOP)**

| | | | | |
|---|---|---|---|---|
| 48 | IO | I | P2[0] | |
| 49 | IO | I | P2[2] | |
| 50 | IO | | P2[4] | |
| 51 | IO | | P2[6] | |
| 52 | IO | I | P0[0] | Analog column mux input. |
| 53 | IO | I | P0[2] | Analog column mux input and column output. |
| 54 | IO | I | P0[4] | Analog column mux input and column output. |
| 55 | IO | I | P0[6] | Analog column mux input. |
| 56 | Power | | Vdd | Supply voltage. |

**LEGEND**: A = Analog, I = Input, O = Output, and OCD = On-Chip Debug.

* These are the ISSP pins, which are not High Z at POR (Power On Reset). See the *PSoC Mixed-Signal Array Technical Reference Manual* for details.



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# 2. Register Reference

This chapter lists the registers of the CY8C21x34 PSoC device. For detailed register information, reference the *PSoC Mixed-Signal Array Technical Reference Manual*.

## 2.1 Register Conventions

The register conventions specific to this section are listed in the following table.

| Convention | Description |
|---|---|
| R | Read register or bit(s) |
| W | Write register or bit(s) |
| L | Logical register or bit(s) |
| C | Clearable register or bit(s) |
| # | Access is bit specific |

## 2.2 Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as IO space and is divided into two banks. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set the user is in Bank 1.

**Note** In the following register mapping tables, blank fields are Reserved and should not be accessed.



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## Register Map 0 Table: User Space

| Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access | Name | Addr (0,Hex) | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PRT0DR | 00 | RW | | 40 | | ASE10CR0 | 80 | RW | | C0 | |
| PRT0IE | 01 | RW | | 41 | | | 81 | | | C1 | |
| PRT0GS | 02 | RW | | 42 | | | 82 | | | C2 | |
| PRT0DM2 | 03 | RW | | 43 | | | 83 | | | C3 | |
| PRT1DR | 04 | RW | | 44 | | ASE11CR0 | 84 | RW | | C4 | |
| PRT1IE | 05 | RW | | 45 | | | 85 | | | C5 | |
| PRT1GS | 06 | RW | | 46 | | | 86 | | | C6 | |
| PRT1DM2 | 07 | RW | | 47 | | | 87 | | | C7 | |
| PRT2DR | 08 | RW | | 48 | | | 88 | | | C8 | |
| PRT2IE | 09 | RW | | 49 | | | 89 | | | C9 | |
| PRT2GS | 0A | RW | | 4A | | | 8A | | | CA | |
| PRT2DM2 | 0B | RW | | 4B | | | 8B | | | CB | |
| PRT3DR | 0C | RW | | 4C | | | 8C | | | CC | |
| PRT3IE | 0D | RW | | 4D | | | 8D | | | CD | |
| PRT3GS | 0E | RW | | 4E | | | 8E | | | CE | |
| PRT3DM2 | 0F | RW | | 4F | | | 8F | | | CF | |
| | 10 | | | 50 | | | 90 | | CUR_PP | D0 | RW |
| | 11 | | | 51 | | | 91 | | STK_PP | D1 | RW |
| | 12 | | | 52 | | | 92 | | | D2 | |
| | 13 | | | 53 | | | 93 | | IDX_PP | D3 | RW |
| | 14 | | | 54 | | | 94 | | MVR_PP | D4 | RW |
| | 15 | | | 55 | | | 95 | | MVW_PP | D5 | RW |
| | 16 | | | 56 | | | 96 | | I2C_CFG | D6 | RW |
| | 17 | | | 57 | | | 97 | | I2C_SCR | D7 | # |
| | 18 | | | 58 | | | 98 | | I2C_DR | D8 | RW |
| | 19 | | | 59 | | | 99 | | I2C_MSCR | D9 | # |
| | 1A | | | 5A | | | 9A | | INT_CLR0 | DA | RW |
| | 1B | | | 5B | | | 9B | | INT_CLR1 | DB | RW |
| | 1C | | | 5C | | | 9C | | | DC | |
| | 1D | | | 5D | | | 9D | | INT_CLR3 | DD | RW |
| | 1E | | | 5E | | | 9E | | INT_MSK3 | DE | RW |
| | 1F | | | 5F | | | 9F | | | DF | |
| DBB00DR0 | 20 | # | AMX_IN | 60 | RW | | A0 | | INT_MSK0 | E0 | RW |
| DBB00DR1 | 21 | W | AMUXCFG | 61 | RW | | A1 | | INT_MSK1 | E1 | RW |
| DBB00DR2 | 22 | RW | PWM_CR | 62 | RW | | A2 | | INT_VC | E2 | RC |
| DBB00CR0 | 23 | # | | 63 | | | A3 | | RES_WDT | E3 | W |
| DBB01DR0 | 24 | # | CMP_CR0 | 64 | # | | A4 | | | E4 | |
| DBB01DR1 | 25 | W | | 65 | | | A5 | | | E5 | |
| DBB01DR2 | 26 | RW | CMP_CR1 | 66 | RW | | A6 | | DEC_CR0 | E6 | RW |
| DBB01CR0 | 27 | # | | 67 | | | A7 | | DEC_CR1 | E7 | RW |
| DCB02DR0 | 28 | # | ADC0_CR | 68 | # | | A8 | | | E8 | |
| DCB02DR1 | 29 | W | ADC1_CR | 69 | # | | A9 | | | E9 | |
| DCB02DR2 | 2A | RW | | 6A | | | AA | | | EA | |
| DCB02CR0 | 2B | # | | 6B | | | AB | | | EB | |
| DCB03DR0 | 2C | # | TMP_DR0 | 6C | RW | | AC | | | EC | |
| DCB03DR1 | 2D | W | TMP_DR1 | 6D | RW | | AD | | | ED | |
| DCB03DR2 | 2E | RW | TMP_DR2 | 6E | RW | | AE | | | EE | |
| DCB03CR0 | 2F | # | TMP_DR3 | 6F | RW | | AF | | | EF | |
| | 30 | | | 70 | | RDI0RI | B0 | RW | | F0 | |
| | 31 | | | 71 | | RDI0SYN | B1 | RW | | F1 | |
| | 32 | | ACE00CR1 | 72 | RW | RDI0IS | B2 | RW | | F2 | |
| | 33 | | ACE00CR2 | 73 | RW | RDI0LT0 | B3 | RW | | F3 | |
| | 34 | | | 74 | | RDI0LT1 | B4 | RW | | F4 | |
| | 35 | | | 75 | | RDI0RO0 | B5 | RW | | F5 | |
| | 36 | | ACE01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| | 37 | | ACE01CR2 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| | 38 | | | 78 | | | B8 | | | F8 | |
| | 39 | | | 79 | | | B9 | | | F9 | |
| | 3A | | | 7A | | | BA | | | FA | |
| | 3B | | | 7B | | | BB | | | FB | |
| | 3C | | | 7C | | | BC | | | FC | |
| | 3D | | | 7D | | | BD | | DAC_D | FD | RW |
| | 3E | | | 7E | | | BE | | CPU_SCR1 | FE | # |
| | 3F | | | 7F | | | BF | | CPU_SCR0 | FF | # |

Blank fields are Reserved and should not be accessed. # Access is bit specific.



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## Register Map 1 Table: Configuration Space

| Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access | Name | Addr (1,Hex) | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PRT0DM0 | 00 | RW | | 40 | | ASE10CR0 | 80 | RW | | C0 | |
| PRT0DM1 | 01 | RW | | 41 | | | 81 | | | C1 | |
| PRT0IC0 | 02 | RW | | 42 | | | 82 | | | C2 | |
| PRT0IC1 | 03 | RW | | 43 | | | 83 | | | C3 | |
| PRT1DM0 | 04 | RW | | 44 | | ASE11CR0 | 84 | RW | | C4 | |
| PRT1DM1 | 05 | RW | | 45 | | | 85 | | | C5 | |
| PRT1IC0 | 06 | RW | | 46 | | | 86 | | | C6 | |
| PRT1IC1 | 07 | RW | | 47 | | | 87 | | | C7 | |
| PRT2DM0 | 08 | RW | | 48 | | | 88 | | | C8 | |
| PRT2DM1 | 09 | RW | | 49 | | | 89 | | | C9 | |
| PRT2IC0 | 0A | RW | | 4A | | | 8A | | | CA | |
| PRT2IC1 | 0B | RW | | 4B | | | 8B | | | CB | |
| PRT3DM0 | 0C | RW | | 4C | | | 8C | | | CC | |
| PRT3DM1 | 0D | RW | | 4D | | | 8D | | | CD | |
| PRT3IC0 | 0E | RW | | 4E | | | 8E | | | CE | |
| PRT3IC1 | 0F | RW | | 4F | | | 8F | | | CF | |
| | 10 | | | 50 | | | 90 | | GDI_O_IN | D0 | RW |
| | 11 | | | 51 | | | 91 | | GDI_E_IN | D1 | RW |
| | 12 | | | 52 | | | 92 | | GDI_O_OU | D2 | RW |
| | 13 | | | 53 | | | 93 | | GDI_E_OU | D3 | RW |
| | 14 | | | 54 | | | 94 | | | D4 | |
| | 15 | | | 55 | | | 95 | | | D5 | |
| | 16 | | | 56 | | | 96 | | | D6 | |
| | 17 | | | 57 | | | 97 | | | D7 | |
| | 18 | | | 58 | | | 98 | | MUX_CR0 | D8 | RW |
| | 19 | | | 59 | | | 99 | | MUX_CR1 | D9 | RW |
| | 1A | | | 5A | | | 9A | | MUX_CR2 | DA | RW |
| | 1B | | | 5B | | | 9B | | MUX_CR3 | DB | RW |
| | 1C | | | 5C | | | 9C | | | DC | |
| | 1D | | | 5D | | | 9D | | OSC_GO_EN | DD | RW |
| | 1E | | | 5E | | | 9E | | OSC_CR4 | DE | RW |
| | 1F | | | 5F | | | 9F | | OSC_CR3 | DF | RW |
| DBB00FN | 20 | RW | CLK_CR0 | 60 | RW | | A0 | | OSC_CR0 | E0 | RW |
| DBB00IN | 21 | RW | CLK_CR1 | 61 | RW | | A1 | | OSC_CR1 | E1 | RW |
| DBB00OU | 22 | RW | ABF_CR0 | 62 | RW | | A2 | | OSC_CR2 | E2 | RW |
| | 23 | | AMD_CR0 | 63 | RW | | A3 | | VLT_CR | E3 | RW |
| DBB01FN | 24 | RW | CMP_GO_EN | 64 | RW | | A4 | | VLT_CMP | E4 | R |
| DBB01IN | 25 | RW | | 65 | | | A5 | | ADC0_TR | E5 | RW |
| DBB01OU | 26 | RW | AMD_CR1 | 66 | RW | | A6 | | ADC1_TR | E6 | RW |
| | 27 | | ALT_CR0 | 67 | RW | | A7 | | | E7 | |
| DCB02FN | 28 | RW | | 68 | | | A8 | | IMO_TR | E8 | W |
| DCB02IN | 29 | RW | | 69 | | | A9 | | ILO_TR | E9 | W |
| DCB02OU | 2A | RW | | 6A | | | AA | | BDG_TR | EA | RW |
| | 2B | | CLK_CR3 | 6B | RW | | AB | | ECO_TR | EB | W |
| DCB03FN | 2C | RW | TMP_DR0 | 6C | RW | | AC | | | EC | |
| DCB03IN | 2D | RW | TMP_DR1 | 6D | RW | | AD | | | ED | |
| DCB03OU | 2E | RW | TMP_DR2 | 6E | RW | | AE | | | EE | |
| | 2F | | TMP_DR3 | 6F | RW | | AF | | | EF | |
| | 30 | | | 70 | | RDI0RI | B0 | RW | | F0 | |
| | 31 | | | 71 | | RDI0SYN | B1 | RW | | F1 | |
| | 32 | | ACE00CR1 | 72 | RW | RDI0IS | B2 | RW | | F2 | |
| | 33 | | ACE00CR2 | 73 | RW | RDI0LT0 | B3 | RW | | F3 | |
| | 34 | | | 74 | | RDI0LT1 | B4 | RW | | F4 | |
| | 35 | | | 75 | | RDI0RO0 | B5 | RW | | F5 | |
| | 36 | | ACE01CR1 | 76 | RW | RDI0RO1 | B6 | RW | | F6 | |
| | 37 | | ACE01CR2 | 77 | RW | | B7 | | CPU_F | F7 | RL |
| | 38 | | | 78 | | | B8 | | | F8 | |
| | 39 | | | 79 | | | B9 | | | F9 | |
| | 3A | | | 7A | | | BA | | FLS_PR1 | FA | RW |
| | 3B | | | 7B | | | BB | | | FB | |
| | 3C | | | 7C | | | BC | | | FC | |
| | 3D | | | 7D | | | BD | | DAC_CR | FD | RW |
| | 3E | | | 7E | | | BE | | CPU_SCR1 | FE | # |
| | 3F | | | 7F | | | BF | | CPU_SCR0 | FF | # |

Blank fields are Reserved and should not be accessed. # Access is bit specific.



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# 3. Electrical Specifications

This chapter presents the DC and AC electrical specifications of the CY8C21x34 PSoC device. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at http://www.cypress.com/psoc.

Specifications are valid for -40°C ≤ $T_A$ ≤ 85°C and $T_J$ ≤ 100°C as specified, except where noted.

Refer to Table 3-14 for the electrical specifications on the internal main oscillator (IMO) using SLIMO mode.

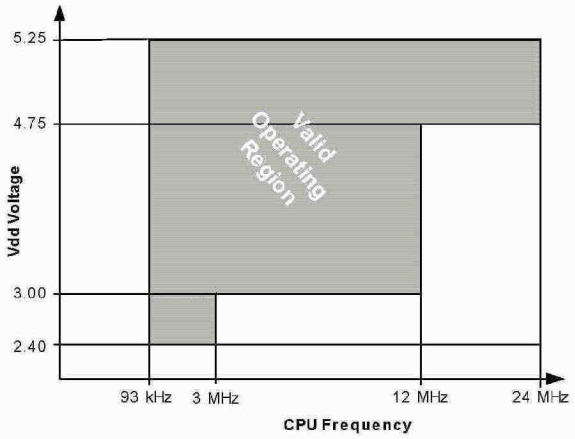


**Figure 3-1a. Voltage versus CPU Frequency**

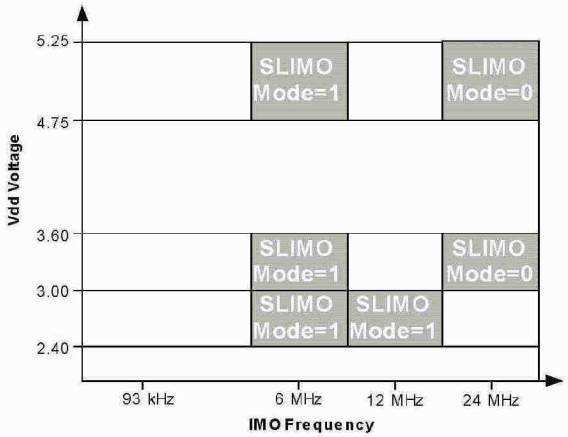


**Figure 3-1b. IMO Frequency Trim Options**

The following table lists the units of measure that are used in this chapter.

**Table 3-1: Units of Measure**

| Symbol | Unit of Measure | Symbol | Unit of Measure |
|---|---|---|---|
| °C | degree Celsius | µW | microwatts |
| dB | decibels | mA | milli-ampere |
| fF | femto farad | ms | milli-second |
| Hz | hertz | mV | milli-volts |
| KB | 1024 bytes | nA | nanoampere |
| Kbit | 1024 bits | ns | nanosecond |
| kHz | kilohertz | nV | nanovolts |
| kΩ | kilohm | Ω | ohm |
| MHz | megahertz | pA | picoampere |
| MΩ | megaohm | pF | picofarad |
| µA | microampere | pp | peak-to-peak |
| µF | microfarad | ppm | parts per million |
| µH | microhenry | ps | picosecond |
| µs | microsecond | sps | samples per second |
| µV | microvolts | σ | sigma: one standard deviation |
| µVrms | microvolts root-mean-square | V | volts |




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## 3.1 Absolute Maximum Ratings

**Table 3-2. Absolute Maximum Ratings**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $T_{STG}$ | Storage Temperature | -55 | 25 | +100 | °C | Higher storage temperatures will reduce data retention time. Recommended storage temperature is +25°C +/- 25°C. Extended duration storage temperatures above 65°C will degrade reliability. |
| $T_A$ | Ambient Temperature with Power Applied | -40 | – | +85 | °C | |
| Vdd | Supply Voltage on Vdd Relative to Vss | -0.5 | – | +6.0 | V | |
| $V_{IO}$ | DC Input Voltage | Vss - 0.5 | – | Vdd + 0.5 | V | |
| $V_{IOZ}$ | DC Voltage Applied to Tri-state | Vss - 0.5 | – | Vdd + 0.5 | V | |
| $I_{MIO}$ | Maximum Current into any Port Pin | -25 | – | +50 | mA | |
| ESD | Electro Static Discharge Voltage | 2000 | – | – | V | Human Body Model ESD. |
| LU | Latch-up Current | – | – | 200 | mA | |

## 3.2 Operating Temperature

**Table 3-3. Operating Temperature**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $T_A$ | Ambient Temperature | -40 | – | +85 | °C | |
| $T_J$ | Junction Temperature | -40 | – | +100 | °C | The temperature rise from ambient to junction is package specific. See "Thermal Impedances" on page 36. The user must limit the power consumption to comply with this requirement. |

## 3.3 DC Electrical Characteristics

### 3.3.1 DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

**Table 3-4. DC Chip-Level Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Vdd | Supply Voltage | 2.40 | – | 5.25 | V | See table titled "DC POR and LVD Specifications" on page 22. |
| $I_{DD}$ | Supply Current, IMO = 24 MHz | – | 3 | 4 | mA | Conditions are Vdd = 5.0V, $T_A$ = 25°C, CPU = 3 MHz, 48 MHz disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.366 kHz. |
| $I_{DD3}$ | Supply Current, IMO = 6 MHz using SLIMO mode. | – | 1.2 | 2 | mA | Conditions are Vdd = 3.3V, $T_A$ = 25°C, CPU = 3 MHz, clock doubler disabled. VC1 = 375 kHz, VC2 = 23.4 kHz, VC3 = 0.091 kHz. |
| $I_{DD27}$ | Supply Current, IMO = 6 MHz using SLIMO mode. | – | 1.1 | 1.5 | mA | Conditions are Vdd = 2.55V, $T_A$ = 25°C, CPU = 3 MHz, clock doubler disabled. VC1 = 375 kHz, VC2 = 23.4 kHz, VC3 = 0.091 kHz. |
| $I_{SB27}$ | Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active. Mid temperature range. | – | 2.6 | 4. | µA | Vdd = 2.55V, 0°C ≤ $T_A$ ≤ 40°C. |
| $I_{SB}$ | Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active. | – | 2.8 | 5 | µA | Vdd = 3.3V, -40°C ≤ $T_A$ ≤ 85°C. |
| $V_{REF}$ | Reference Voltage (Bandgap) | 1.28 | 1.30 | 1.32 | V | Trimmed for appropriate Vdd. Vdd = 3.0V to 5.25V. |



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**Table 3-4. DC Chip-Level Specifications** *(continued)*

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{REF27}$ | Reference Voltage (Bandgap) | 1.16 | 1.30 | 1.33 | V | Trimmed for appropriate Vdd. Vdd = 2.4V to 3.0V. |
| AGND | Analog Ground | $V_{REF}$ - 0.003 | $V_{REF}$ | $V_{REF}$ + 0.003 | V | |

## 3.3.2 DC General Purpose IO Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, and 2.7V at 25°C and are for design guidance only.

**Table 3-5. 5V and 3.3V DC GPIO Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Pull-up Resistor | 4 | 5.6 | 8 | kΩ | |
| $R_{PD}$ | Pull-down Resistor | 4 | 5.6 | 8 | kΩ | |
| $V_{OH}$ | High Output Level | Vdd - 1.0 | – | – | V | IOH = 10 mA, Vdd = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). |
| $V_{OL}$ | Low Output Level | – | – | 0.75 | V | IOL = 25 mA, Vdd = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). |
| $V_{IL}$ | Input Low Level | – | – | 0.8 | V | Vdd = 3.0 to 5.25. |
| $V_{IH}$ | Input High Level | 2.1 | – | | V | Vdd = 3.0 to 5.25. |
| $V_H$ | Input Hysteresis | – | 60 | – | mV | |
| $I_{IL}$ | Input Leakage (Absolute Value) | – | 1 | – | nA | Gross tested to 1 µA. |
| $C_{IN}$ | Capacitive Load on Pins as Input | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25°C. |
| $C_{OUT}$ | Capacitive Load on Pins as Output | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25°C. |

**Table 3-6. 2.7V DC GPIO Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $R_{PU}$ | Pull-up Resistor | 4 | 5.6 | 8 | kΩ | |
| $R_{PD}$ | Pull-down Resistor | 4 | 5.6 | 8 | kΩ | |
| $V_{OH}$ | High Output Level | Vdd - 0.4 | – | – | V | IOH = 2.5 mA (6.25 Typ), Vdd = 2.4 to 3.0V (16 mA maximum, 50 mA Typ combined IOH budget). |
| $V_{OL}$ | Low Output Level | – | – | 0.75 | V | IOL = 10 mA, Vdd = 2.4 to 3.0V (90 mA maximum combined IOL budget). |
| $V_{IL}$ | Input Low Level | – | – | 0.75 | V | Vdd = 2.4 to 3.0. |
| $V_{IH}$ | Input High Level | 2.0 | – | – | V | Vdd = 2.4 to 3.0. |
| $V_H$ | Input Hysteresis | – | 90 | – | mV | |
| $I_{IL}$ | Input Leakage (Absolute Value) | – | 1 | – | nA | Gross tested to 1 µA. |
| $C_{IN}$ | Capacitive Load on Pins as Input | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25°C. |
| $C_{OUT}$ | Capacitive Load on Pins as Output | – | 3.5 | 10 | pF | Package and pin dependent. Temp = 25°C. |



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### 3.3.3 DC Operational Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

**Table 3-7. 5V DC Operational Amplifier Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{OSOA}$ | Input Offset Voltage (absolute value) | – | 2.5 | 15 | mV | |
| $TCV_{OSOA}$ | Average Input Offset Voltage Drift | – | 10 | – | µV/°C | |
| $I_{EBOA}$[a] | Input Leakage Current (Port 0 Analog Pins) | – | 200 | – | pA | Gross tested to 1 µA. |
| $C_{INOA}$ | Input Capacitance (Port 0 Analog Pins) | – | 4.5 | 9.5 | pF | Package and pin dependent. Temp = 25°C. |
| $V_{CMOA}$ | Common Mode Voltage Range | 0.0 | – | Vdd - 1 | V | |
| $G_{OLOA}$ | Open Loop Gain | – | 80 | – | dB | |
| $I_{SOA}$ | Amplifier Supply Current | – | 10 | 30 | µA | |

a. Atypical behavior: $I_{EBOA}$ of Port 0 Pin 0 is below 1 nA at 25°C; 50 nA over temperature. Use Port 0 Pins 1-7 for the lowest leakage of 200 nA.

**Table 3-8. 3.3V DC Operational Amplifier Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{OSOA}$ | Input Offset Voltage (absolute value) | – | 2.5 | 15 | mV | |
| $TCV_{OSOA}$ | Average Input Offset Voltage Drift | – | 10 | – | µV/°C | |
| $I_{EBOA}$[a] | Input Leakage Current (Port 0 Analog Pins) | – | 200 | – | pA | Gross tested to 1 µA. |
| $C_{INOA}$ | Input Capacitance (Port 0 Analog Pins) | – | 4.5 | 9.5 | pF | Package and pin dependent. Temp = 25°C. |
| $V_{CMOA}$ | Common Mode Voltage Range | 0 | – | Vdd - 1 | V | |
| $G_{OLOA}$ | Open Loop Gain | – | 80 | – | dB | |
| $I_{SOA}$ | Amplifier Supply Current | – | 10 | 30 | µA | |

a. Atypical behavior: $I_{EBOA}$ of Port 0 Pin 0 is below 1 nA at 25°C; 50 nA over temperature. Use Port 0 Pins 1-7 for the lowest leakage of 200 nA.

**Table 3-9. 2.7V DC Operational Amplifier Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{OSOA}$ | Input Offset Voltage (absolute value) | – | 2.5 | 15 | mV | |
| $TCV_{OSOA}$ | Average Input Offset Voltage Drift | – | 10 | – | µV/°C | |
| $I_{EBOA}$[a] | Input Leakage Current (Port 0 Analog Pins) | – | 200 | – | pA | Gross tested to 1 µA. |
| $C_{INOA}$ | Input Capacitance (Port 0 Analog Pins) | – | 4.5 | 9.5 | pF | Package and pin dependent. Temp = 25°C. |
| $V_{CMOA}$ | Common Mode Voltage Range | 0 | – | Vdd - 1 | V | |
| $G_{OLOA}$ | Open Loop Gain | – | 80 | – | dB | |
| $I_{SOA}$ | Amplifier Supply Current | – | 10 | 30 | µA | |

a. Atypical behavior: $I_{EBOA}$ of Port 0 Pin 0 is below 1 nA at 25°C; 50 nA over temperature. Use Port 0 Pins 1-7 for the lowest leakage of 200 nA.



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### 3.3.4 DC Switch Mode Pump Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

**Table 3-10. DC Switch Mode Pump (SMP) Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{PUMP5V}$ | 5V Output Voltage from Pump | 4.75 | 5.0 | 5.25 | V | Configuration of footnote.[a] Average, neglecting ripple. SMP trip voltage is set to 5.0V. |
| $V_{PUMP3V}$ | 3.3V Output Voltage from Pump | 3.00 | 3.25 | 3.60 | V | Configuration of footnote.[a] Average, neglecting ripple. SMP trip voltage is set to 3.25V. |
| $V_{PUMP2V}$ | 2.6V Output Voltage from Pump | 2.45 | 2.55 | 2.80 | V | Configuration of footnote.[a] Average, neglecting ripple. SMP trip voltage is set to 2.55V. |
| $I_{PUMP}$ | Available Output Current | | | | | Configuration of footnote.[a] |
| | $V_{BAT}$ = 1.8V, $V_{PUMP}$ = 5.0V | 5 | – | – | mA | SMP trip voltage is set to 5.0V. |
| | $V_{BAT}$ = 1.5V, $V_{PUMP}$ = 3.25V | 8 | – | – | mA | SMP trip voltage is set to 3.25V. |
| | $V_{BAT}$ = 1.3V, $V_{PUMP}$ = 2.55V | 8 | – | – | mA | SMP trip voltage is set to 2.55V. |
| $V_{BAT5V}$ | Input Voltage Range from Battery | 1.8 | – | 5.0 | V | Configuration of footnote.[a] SMP trip voltage is set to 5.0V. |
| $V_{BAT3V}$ | Input Voltage Range from Battery | 1.0 | – | 3.3 | V | Configuration of footnote.[a] SMP trip voltage is set to 3.25V. |
| $V_{BAT2V}$ | Input Voltage Range from Battery | 1.0 | – | 2.8 | V | Configuration of footnote.[a] SMP trip voltage is set to 2.55V. |
| $V_{BATSTART}$ | Minimum Input Voltage from Battery to Start Pump | 1.2 | – | – | V | Configuration of footnote.[a] 0°C ≤ $T_A$ ≤ 100. 1.25V at $T_A$ = -40°C. |
| $\Delta V_{PUMP_Line}$ | Line Regulation (over Vi range) | – | 5 | – | $\%V_O$ | Configuration of footnote.[a] $V_O$ is the "Vdd Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 3-12 on page 22. |
| $\Delta V_{PUMP_Load}$ | Load Regulation | – | 5 | – | $\%V_O$ | Configuration of footnote.[a] $V_O$ is the "Vdd Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 3-12 on page 22. |
| $\Delta V_{PUMP_Ripple}$ | Output Voltage Ripple (depends on cap/load) | – | 100 | – | mVpp | Configuration of footnote.[a] Load is 5 mA. |
| $E_3$ | Efficiency | 35 | 50 | – | % | Configuration of footnote.[a] Load is 5 mA. SMP trip voltage is set to 3.25V. |
| $E_2$ | Efficiency | 35 | 80 | – | % | For I load = 1mA, $V_{PUMP}$ = 2.55V, $V_{BAT}$ = 1.3V, 10 uH inductor, 1 uF capacitor, and Schottky diode. |
| $F_{PUMP}$ | Switching Frequency | – | 1.3 | – | MHz | |
| $DC_{PUMP}$ | Switching Duty Cycle | – | 50 | – | % | |

a. $L_1$ = 2 µH inductor, $C_1$ = 10 µF capacitor, $D_1$ = Schottky diode. See Figure 3-2.

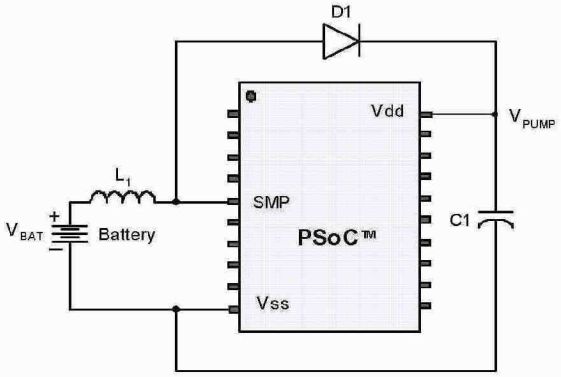


**Figure 3-2. Basic Switch Mode Pump Circuit**



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### 3.3.5 DC Analog Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

**Table 3-11. DC Analog Mux Bus Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $R_{SW}$ | Switch Resistance to Common Analog Bus | – | – | 400<br>800 | Ω<br>Ω | Vdd ≥ 2.7V<br>2.4V ≤ Vdd ≤ 2.7V |
| $R_{VDD}$ | Resistance of Initialization Switch to Vdd | – | – | 800 | Ω | |

### 3.3.6 DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ $T_A$ ≤ 85°C, 3.0V to 3.6V and -40°C ≤ $T_A$ ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ $T_A$ ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

**Table 3-12. DC POR and LVD Specifications**

| Symbol | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| | Vdd Value for PPOR Trip | | | | | Vdd must be greater than or equal to 2.5V during startup, reset from the XRES pin, or reset from Watchdog. |
| $V_{PPOR0}$ | PORLEV[1:0] = 00b | | 2.36 | 2.40 | V | |
| $V_{PPOR1}$ | PORLEV[1:0] = 01b | – | 2.82 | 2.95 | V | |
| $V_{PPOR2}$ | PORLEV[1:0] = 10b | | 4.55 | 4.70 | V | |
| | Vdd Value for LVD Trip | | | | | |
| $V_{LVD0}$ | VM[2:0] = 000b | 2.40 | 2.45 | 2.51[a] | V | |
| $V_{LVD1}$ | VM[2:0] = 001b | 2.85 | 2.92 | 2.99[b] | V | |
| $V_{LVD2}$ | VM[2:0] = 010b | 2.95 | 3.02 | 3.09 | V | |
| $V_{LVD3}$ | VM[2:0] = 011b | 3.06 | 3.13 | 3.20 | V | |
| $V_{LVD4}$ | VM[2:0] = 100b | 4.37 | 4.48 | 4.55 | V | |
| $V_{LVD5}$ | VM[2:0] = 101b | 4.50 | 4.64 | 4.75 | V | |
| $V_{LVD6}$ | VM[2:0] = 110b | 4.62 | 4.73 | 4.83 | V | |
| $V_{LVD7}$ | VM[2:0] = 111b | 4.71 | 4.81 | 4.95 | V | |
| | Vdd Value for PUMP Trip | | | | | |
| $V_{PUMP0}$ | VM[2:0] = 000b | 2.45 | 2.55 | 2.62[c] | V | |
| $V_{PUMP1}$ | VM[2:0] = 001b | 2.96 | 3.02 | 3.09 | V | |
| $V_{PUMP2}$ | VM[2:0] = 010b | 3.03 | 3.10 | 3.16 | V | |
| $V_{PUMP3}$ | VM[2:0] = 011b | 3.18 | 3.25 | 3.32[d] | V | |
| $V_{PUMP4}$ | VM[2:0] = 100b | 4.54 | 4.64 | 4.74 | V | |
| $V_{PUMP5}$ | VM[2:0] = 101b | 4.62 | 4.73 | 4.83 | V | |
| $V_{PUMP6}$ | VM[2:0] = 110b | 4.71 | 4.82 | 4.92 | V | |
| $V_{PUMP7}$ | VM[2:0] = 111b | 4.89 | 5.00 | 5.12 | V | |

a. Always greater than 50 mV above $V_{PPOR}$ (PORLEV = 00) for falling supply.
b. Always greater than 50 mV above $V_{PPOR}$ (PORLEV = 01) for falling supply.
c. Always greater than 50 mV above $V_{LVD0}$.
d. Always greater than 50 mV above $V_{LVD3}$.



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