3.3.7 DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 3-13. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd_{IWRITE}	Supply Voltage for Flash Write Operations	2.70	–	–	V	
I_{DDP}	Supply Current During Programming or Verify	–	5	25	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.2	–	–	V	
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	Vss + 0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	Vdd - 1.0	–	Vdd	V	
$Flash_{ENPB}$	Flash Endurance (per block)	50,000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash Endurance (total)[a]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

a. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.

3.4 AC Electrical Characteristics

3.4.1 AC Chip-Level Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 3-14. 5V and 3.3V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO24}	Internal Main Oscillator Frequency for 24 MHz	23.4	24	24.6[a,b,c]	MHz	Trimmed for 5V or 3.3V operation using factory trim values. See Figure 3-1b on page 17. SLIMO mode = 0.
F_{IMO6}	Internal Main Oscillator Frequency for 6 MHz	5.75	6	6.35[a,b,c]	MHz	Trimmed for 5V or 3.3V operation using factory trim values. See Figure 3-1b on page 17. SLIMO mode = 1.
F_{CPU1}	CPU Frequency (5V Nominal)	0.93	24	24.6[a,b]	MHz	24 MHz only for SLIMO mode = 0.
F_{CPU2}	CPU Frequency (3.3V Nominal)	0.93	12	12.3[b,c]	MHz	
F_{BLK5}	Digital PSoC Block Frequency (5V Nominal)	0	48	49.2[a,b,d]	MHz	Refer to the AC Digital Block Specifications below.
F_{BLK33}	Digital PSoC Block Frequency (3.3V Nominal)	0	24	24.6[b,d]	MHz	
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	
Jitter32k	32 kHz RMS Period Jitter	–	100	200	ns	
Jitter32k	32 kHz Peak-to-Peak Period Jitter	–	1400	–		
T_{XRST}	External Reset Pulse Width	10	–	–	µs	
DC24M	24 MHz Duty Cycle	40	50	60	%	
Step24M	24 MHz Trim Step Size	–	50	–	kHz	
Fout48M	48 MHz Output Frequency	46.8	48.0	49.2[a,c]	MHz	Trimmed. Utilizing factory trim values.
Jitter24M1	24 MHz Peak-to-Peak Period Jitter (IMO)	–	600		ps	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
T_{RAMP}	Supply Ramp Time	0	–	–	µs	

a. 4.75V < Vdd < 5.25V.
b. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
c. 3.0V < Vdd < 3.6V. See Application Note AN2012 "Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation" for information on trimming for operation at 3.3V.
d. See the individual user module data sheets for information on maximum frequencies for user modules.

Table 3-15. 2.7V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO12}	Internal Main Oscillator Frequency for 12 MHz	11.5	12	12.7[a,b,c]	MHz	Trimmed for 2.7V operation using factory trim values. See Figure 3-1b on page 17. SLIMO mode = 1.
F_{IMO6}	Internal Main Oscillator Frequency for 6 MHz	5.75	6	6.35[a,b,c]	MHz	Trimmed for 2.7V operation using factory trim values. See Figure 3-1b on page 17. SLIMO mode = 1.
F_{CPU1}	CPU Frequency (2.7V Nominal)	0.093	3	3.15[a,b]	MHz	24 MHz only for SLIMO mode = 0.
F_{BLK27}	Digital PSoC Block Frequency (2.7V Nominal)	0	12	12.5[a,b,c]	MHz	Refer to the AC Digital Block Specifications below.
F_{32K1}	Internal Low Speed Oscillator Frequency	8	32	96	kHz	
Jitter32k	32 kHz RMS Period Jitter	–	150	200	ns	
Jitter32k	32 kHz Peak-to-Peak Period Jitter	–	1400	–		
T_{XRST}	External Reset Pulse Width	10	–	–	µs	
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
T_{RAMP}	Supply Ramp Time	0	–	–	µs	

a. 2.4V < Vdd < 3.0V.
b. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
c. See Application Note AN2012 "Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation" for information on maximum frequency for user modules.

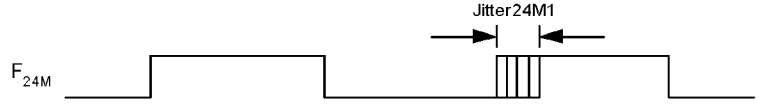


Figure 3-3. 24 MHz Period Jitter (IMO) Timing Diagram

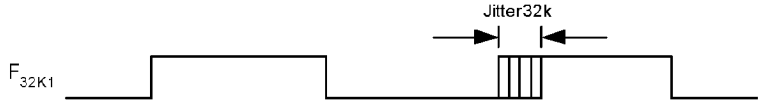


Figure 3-4. 32 kHz Period Jitter (ILO) Timing Diagram

3.4.2 AC General Purpose IO Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 3-16. 5V and 3.3V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	12	MHz	Normal Strong Mode
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	3	–	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	2	–	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	7	27	–	ns	Vdd = 3 to 5.25V, 10% - 90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	7	22	–	ns	Vdd = 3 to 5.25V, 10% - 90%

Table 3-17. 2.7V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	3	MHz	Normal Strong Mode
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	6	–	50	ns	Vdd = 2.4 to 3.0V, 10% - 90%
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	6	–	50	ns	Vdd = 2.4 to 3.0V, 10% - 90%
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	18	40	120	ns	Vdd = 2.4 to 3.0V, 10% - 90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	18	40	120	ns	Vdd = 2.4 to 3.0V, 10% - 90%

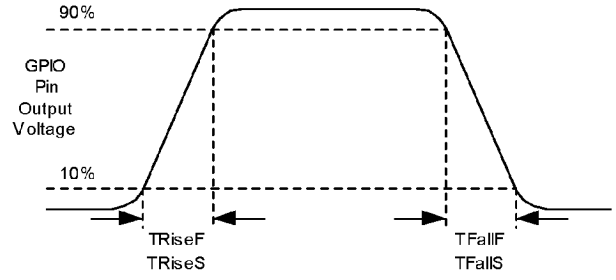


Figure 3-5. GPIO Timing Diagram

3.4.3 AC Operational Amplifier Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 3-18. AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{COMP}	Comparator Mode Response Time, 50 mV Overdrive			100 200	ns ns	Vdd ≥ 3.0V. 2.4V < Vcc < 3.0V.

3.4.4 AC Analog Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 3-19. AC Analog Mux Bus Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{SW}	Switch Rate	–	–	3.17	MHz	

3.4.5 AC Digital Block Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 3-20. 5V and 3.3V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All Functions	Maximum Block Clocking Frequency (> 4.75V)			49.2	MHz	4.75V < Vdd < 5.25V.
	Maximum Block Clocking Frequency (< 4.75V)			24.6	MHz	3.0V < Vdd < 4.75V.
Timer	Capture Pulse Width	50[a]	–	–	ns	
	Maximum Frequency, No Capture	–	–	49.2	MHz	4.75V < Vdd < 5.25V.
	Maximum Frequency, With or Without Capture	–	–	24.6	MHz	
Counter	Enable Pulse Width	50	–	–	ns	
	Maximum Frequency, No Enable Input	–	–	49.2	MHz	4.75V < Vdd < 5.25V.
	Maximum Frequency, Enable Input	–	–	24.6	MHz	
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50	–	–	ns	
	Disable Mode	50	–	–	ns	
	Maximum Frequency	–	–	49.2	MHz	4.75V < Vdd < 5.25V.
CRCPRS (PRS Mode)	Maximum Input Clock Frequency	–	–	49.2	MHz	4.75V < Vdd < 5.25V.
CRCPRS (CRC Mode)	Maximum Input Clock Frequency	–	–	24.6	MHz	
SPIM	Maximum Input Clock Frequency	–	–	8.2	MHz	Maximum data rate at 4.1 MHz due to 2 x over clocking.
SPIS	Maximum Input Clock Frequency	–	–	4.1	MHz	
	Width of SS_ Negated Between Transmissions	50	–	–	ns	

Table 3-20. 5V and 3.3V AC Digital Block Specifications *(continued)*

Transmitter	Maximum Input Clock Frequency	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.
	Maximum Input Clock Frequency with Vdd ≥ 4.75V, 2 Stop Bits	–	–	49.2	MHz	Maximum data rate at 6.15 MHz due to 8 x over clocking.
Receiver	Maximum Input Clock Frequency	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.
	Maximum Input Clock Frequency with Vdd ≥ 4.75V, 2 Stop Bits	–	–	49.2	MHz	Maximum data rate at 6.15 MHz due to 8 x over clocking.

a. 50 ns minimum input pulse width is based on the input synchronizers running at 12 MHz (84 ns nominal period).

Table 3-21. 2.7V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All Functions	Maximum Block Clocking Frequency			12.7	MHz	2.4V < Vdd < 3.0V.
Timer	Capture Pulse Width	100[a]	–	–	ns	
	Maximum Frequency, With or Without Capture	–	–	12.7	MHz	
Counter	Enable Pulse Width	100	–	–	ns	
	Maximum Frequency, No Enable Input	–	–	12.7	MHz	
	Maximum Frequency, Enable Input	–	–	12.7	MHz	
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	100	–	–	ns	
	Disable Mode	100	–	–	ns	
	Maximum Frequency	–	–	12.7	MHz	
CRCPRS (PRS Mode)	Maximum Input Clock Frequency	–	–	12.7	MHz	
CRCPRS (CRC Mode)	Maximum Input Clock Frequency	–	–	12.7	MHz	
SPIM	Maximum Input Clock Frequency	–	–	6.35	MHz	Maximum data rate at 3.17 MHz due to 2 x over clocking.
SPIS	Maximum Input Clock Frequency	–	–	4.1	MHz	
	Width of SS_ Negated Between Transmissions	100	–	–	ns	
Transmitter	Maximum Input Clock Frequency	–	–	12.7	MHz	Maximum data rate at 1.59 MHz due to 8 x over clocking.
Receiver	Maximum Input Clock Frequency	–	–	12.7	MHz	Maximum data rate at 1.59 MHz due to 8 x over clocking.

a. 100 ns minimum input pulse width is based on the input synchronizers running at 12 MHz (84 ns nominal period).

3.4.6 AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 3-22. 5V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
FOSCEXT	Frequency	0.093	–	24.6	MHz	
–	High Period	20.6	–	5300	ns	
–	Low Period	20.6	–	–	ns	
–	Power Up IMO to Switch	150	–	–	µs	

Table 3-23. 3.3V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
FOSCEXT	Frequency with CPU Clock divide by 1	0.093	–	12.3	MHz	Maximum CPU frequency is 12 MHz at 3.3V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
FOSCEXT	Frequency with CPU Clock divide by 2 or greater	0.186	–	24.6	MHz	If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider will ensure that the fifty percent duty cycle requirement is met.
–	High Period with CPU Clock divide by 1	41.7	–	5300	ns	
–	Low Period with CPU Clock divide by 1	41.7	–	–	ns	
–	Power Up IMO to Switch	150	–	–	µs	

Table 3-24. 2.7V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
FOSCEXT	Frequency with CPU Clock divide by 1	0.093	–	3.08	MHz	Maximum CPU frequency is 3 MHz at 2.7V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
FOSCEXT	Frequency with CPU Clock divide by 2 or greater	0.186	–	6.35	MHz	If the frequency of the external clock is greater than 3 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider will ensure that the fifty percent duty cycle requirement is met.
–	High Period with CPU Clock divide by 1	160	–	5300	ns	
–	Low Period with CPU Clock divide by 1	160	–	–	ns	
–	Power Up IMO to Switch	150	–	–	µs	

3.4.7 AC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 3-25. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RSCLK}	Rise Time of SCLK	1	–	20	ns	
T_{FSCLK}	Fall Time of SCLK	1	–	20	ns	
T_{SSCLK}	Data Set up Time to Falling Edge of SCLK	40	–	–	ns	
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
T_{ERASEB}	Flash Erase Time (Block)	–	15	–	ms	
T_{WRITE}	Flash Block Write Time	–	30	–	ms	
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	45	ns	3.6 < Vdd
T_{DSCLK3}	Data Out Delay from Falling Edge of SCLK	–	–	50	ns	3.0 ≤ Vdd ≤ 3.6
T_{DSCLK2}	Data Out Delay from Falling Edge of SCLK	–	–	70	ns	2.4 ≤ Vdd ≤ 3.0

3.4.8 AC I2C Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V, 3.3V, or 2.7V at 25°C and are for design guidance only.

Table 3-26. AC Characteristics of the I2C SDA and SCL Pins for Vdd ≥ 3.0V

Symbol	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
FSCLI2C	SCL Clock Frequency	0	100	0	400	kHz	
THDSTAI2C	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	
TLOWI2C	LOW Period of the SCL Clock	4.7	–	1.3	–	µs	
THIGHI2C	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs	
TSUSTAI2C	Set-up Time for a Repeated START Condition	4.7	–	0.6	–	µs	
THDDATI2C	Data Hold Time	0	–	0	–	µs	
TSUDATI2C	Data Set-up Time	250	–	100[a]	–	ns	
TSUSTOI2C	Set-up Time for STOP Condition	4.0	–	0.6	–	µs	
TBUFI2C	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	µs	
TSPI2C	Pulse Width of spikes are suppressed by the input filter.	–	–	0	50	ns	

a. A Fast-Mode I2C-bus device can be used in a Standard-Mode I2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I2C-bus specification) before the SCL line is released.

Table 3-27. 2.7V AC Characteristics of the I2C SDA and SCL Pins (Fast Mode not Supported)

Symbol	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
FSCLI2C	SCL Clock Frequency	0	100	–	–	kHz	
THDSTAI2C	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	–	–	µs	
TLOWI2C	LOW Period of the SCL Clock	4.7	–	–	–	µs	
THIGHI2C	HIGH Period of the SCL Clock	4.0	–	–	–	µs	
TSUSTAI2C	Set-up Time for a Repeated START Condition	4.7	–	–	–	µs	
THDDATI2C	Data Hold Time	0	–	–	–	µs	
TSUDATI2C	Data Set-up Time	250	–	–	–	ns	
TSUSTOI2C	Set-up Time for STOP Condition	4.0	–	–	–	µs	
TBUFI2C	Bus Free Time Between a STOP and START Condition	4.7	–	–	–	µs	
TSPI2C	Pulse Width of spikes are suppressed by the input filter.	–	–	–	–	ns	

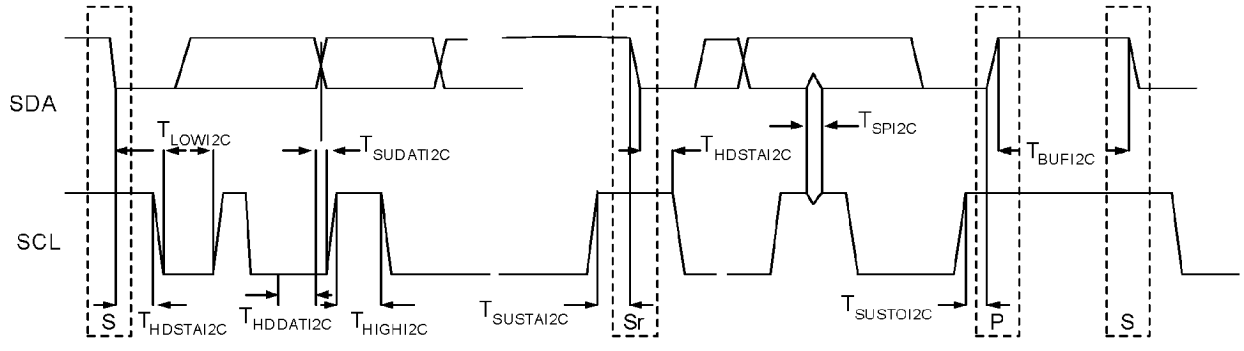


Figure 3-6. Definition for Timing for Fast/Standard Mode on the I2C Bus

4. Packaging Information

This chapter illustrates the packaging specifications for the CY8C21x34 PSoC device, along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at http://www.cypress.com/support/link.cfm?mr=poddim.

4.1 Packaging Dimensions

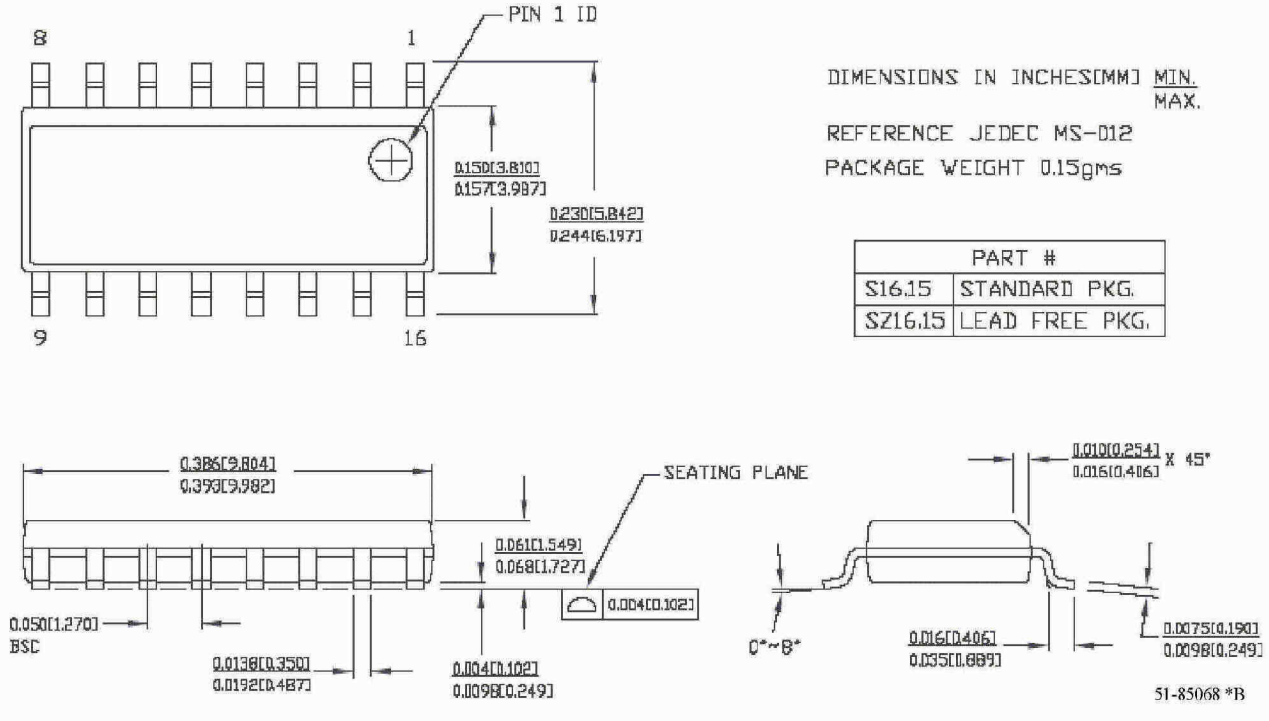


Figure 4-1. 16-Lead (150-Mil) SOIC

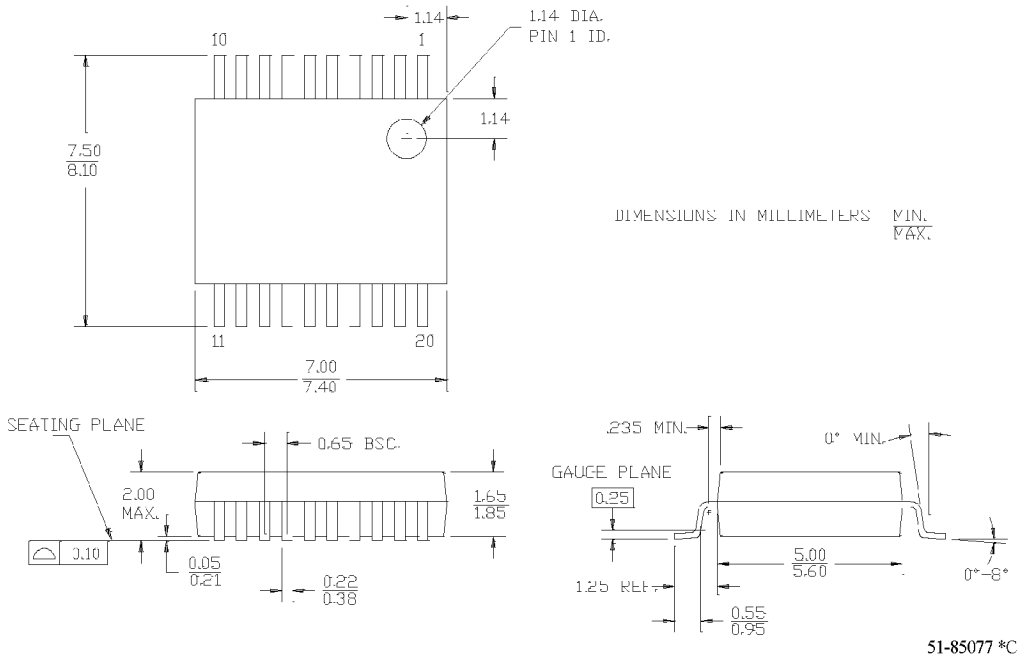


Figure 4-2. 20-Lead (210-MIL) SSOP

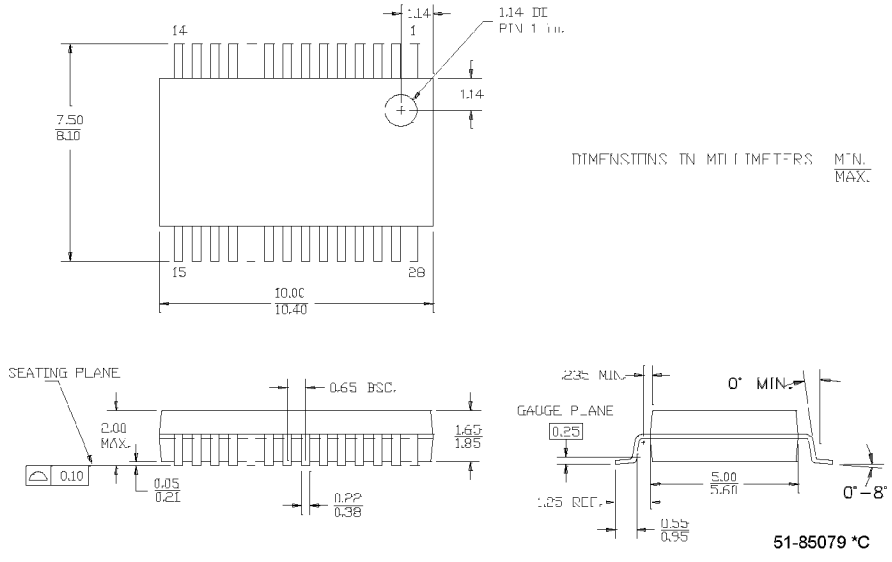
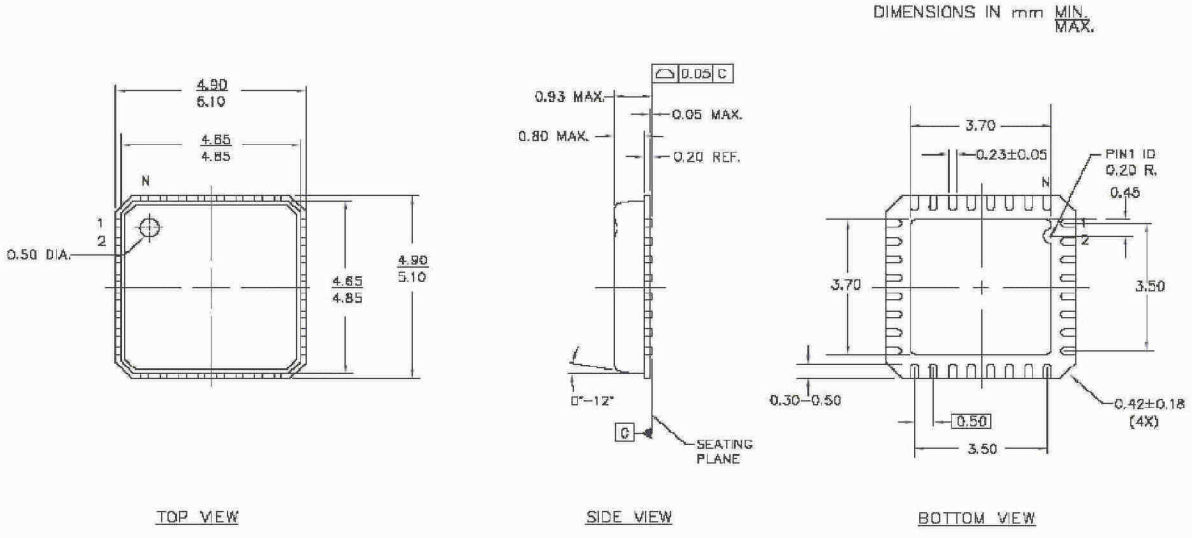


Figure 4-3. 28-Lead (210-Mil) SSOP

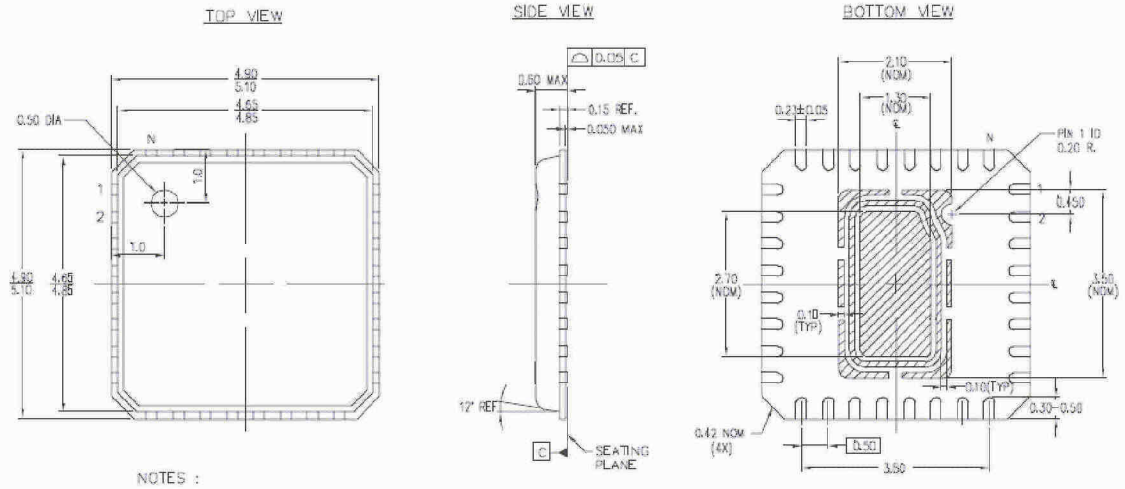


E-PAD X, Y for this product is 3.53 mm, 3.53 mm (+/-0.11 mm)

JEDEC # MO-220
Package Weight: 0.054 grams

51-85188 *A

Figure 4-4. 32-Lead (5x5 mm 0.93 MAX) QFN



NOTES :

HATCH AREA IS EXPOSED METAL

JEDEC # MO-220

DIMENSIONS IN mm MIN.
MAX.

UNIT PACKAGE WEIGHT : 0.0354 Grams

-PACKAGE CODE

PART NO.	DESCRIPTION
LJ32B	STANDARD
LK32B	PB-FREE

E-PAD X, Y for this product is 3.53 mm, 3.53 mm (+/-0.11 mm)

001-06392 **

Figure 4-5. 32-Lead (5x5 mm 0.60 MAX) QFN

Important Note For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.

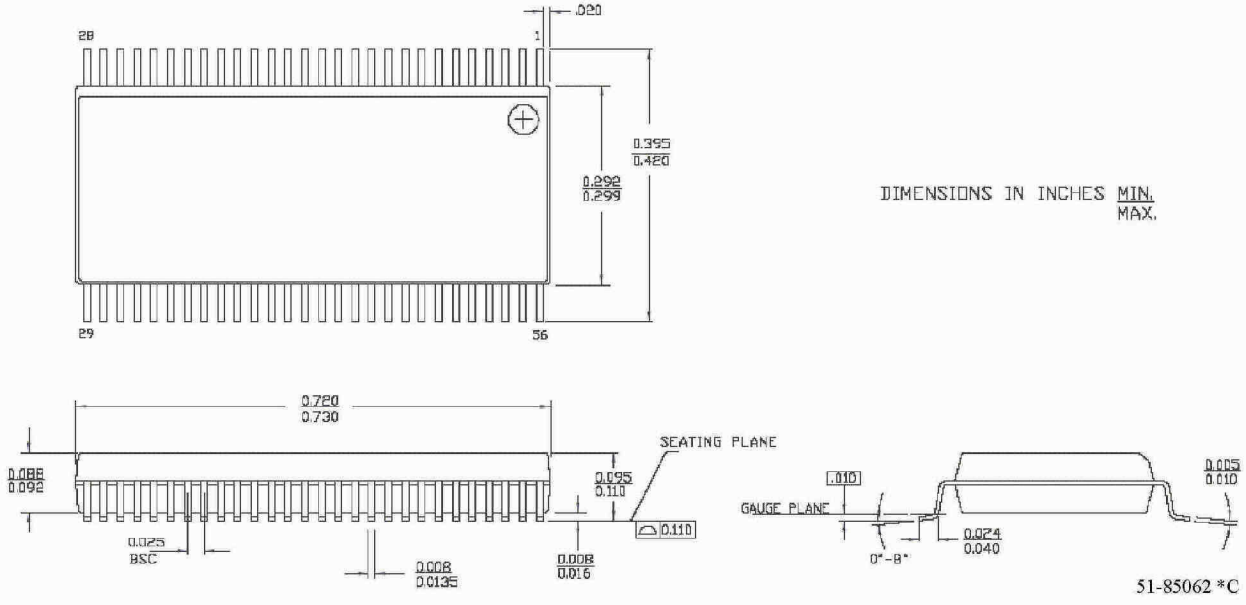


Figure 4-6. 56-Lead (300-Mil) SSOP

4.2 Thermal Impedances

Table 4-1. Thermal Impedances per Package

Package	Typical θ_{JA} *	Typical θ_{JC}
16 SOIC	123 °C/W	55 °C/W
20 SSOP	117 °C/W	41 °C/W
28 SSOP	96 °C/W	39 °C/W
32 QFN** 5x5 mm 0.60 MAX	27 °C/W	15 °C/W
32 QFN** 5x5 mm 0.93 MAX	22 °C/W	12 °C/W

* $T_J = T_A + \text{Power} \times \theta_{JA}$

** To achieve the thermal impedance specified for the QFN package, the center thermal pad should be soldered to the PCB ground plane.

4.3 Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 4-2. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature*	Maximum Peak Temperature
16 SOIC	240°C	260°C
20 SSOP	240°C	260°C
28 SSOP	240°C	260°C
32 QFN	240°C	260°C

*Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220+/-5°C with Sn-Pb or 245+/-5°C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

5. Ordering Information

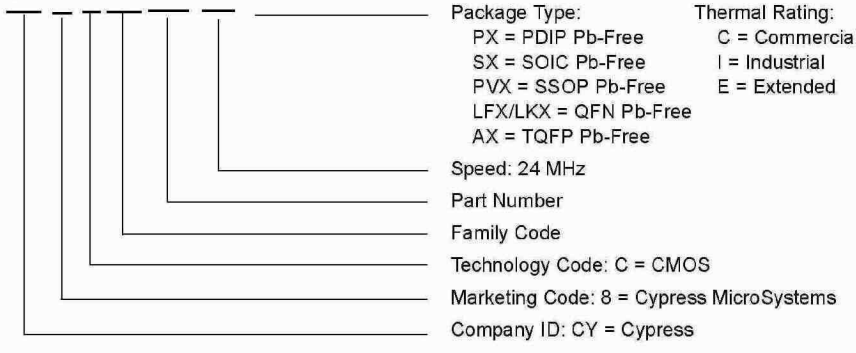
CY8C21x34 PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	Switch Mode Pump	Temperature Range	Digital Blocks	Analog Blocks	Digital IO Pins	Analog Inputs [a]	Analog Outputs	XRES Pin
16 Pin (150-Mil) SOIC	CY8C21234-24SXI	8K	512	Yes	-40°C to +85°C	4	4	12	12[a]	0	No
16 Pin (150-Mil) SOIC (Tape and Reel)	CY8C21234-24SXIT	8K	512	Yes	-40°C to +85°C	4	4	12	12[a]	0	No
20 Pin (210-Mil) SSOP	CY8C21334-24PVXI	8K	512	No	-40°C to +85°C	4	4	16	16[a]	0	Yes
20 Pin (210-Mil) SSOP (Tape and Reel)	CY8C21334-24PVXIT	8K	512	No	-40°C to +85°C	4	4	16	16[a]	0	Yes
28 Pin (210-Mil) SSOP	CY8C21534-24PVXI	8K	512	No	-40°C to +85°C	4	4	24	24[a]	0	Yes
28 Pin (210-Mil) SSOP (Tape and Reel)	CY8C21534-24PVXIT	8K	512	No	-40°C to +85°C	4	4	24	24[a]	0	Yes
32 Pin (5x5 mm **0.93 MAX**) QFN [b]	CY8C21434-24LFXI	8K	512	**No**	-40°C to +85°C	4	4	28	28[a]	0	Yes
32 Pin (5x5 mm **0.93 MAX**) QFN [b] (Tape and Reel)	CY8C21434-24LFXIT	8K	512	**No**	-40°C to +85°C	4	4	28	28[a]	0	Yes
32 Pin (5x5 mm **0.60 MAX**) QFN [b]	CY8C21434-24LKXI	8K	512	**No**	-40°C to +85°C	4	4	28	28[a]	0	Yes
32 Pin (5x5 mm **0.06 MAX**) QFN [b] (Tape and Reel)	CY8C21434-24LKXIT	8K	512	**No**	-40°C to +85°C	4	4	28	28[a]	0	Yes
32 Pin (5x5 mm **0.93 MAX**) QFN [b]	CY8C21634-24LFXI	8K	512	**Yes**	-40°C to +85°C	4	4	26	26[a]	0	Yes
32 Pin (5x5 mm **0.93 MAX**) QFN [b] (Tape and Reel)	CY8C21634-24LFXIT	8K	512	**Yes**	-40°C to +85°C	4	4	26	26[a]	0	Yes
56 Pin OCD SSOP	CY8C21001-24PVXI	8K	512	Yes	-40°C to +85°C	4	4	26	26[a]	0	Yes

a. All Digital IO Pins also connect to the common analog mux.
b. Refer to the "32-Pin Part Pinout" on page 11 for pin differences.

5.1 Ordering Code Definitions

CY 8 C 21 xxx-24xx



6. Sales and Service Information

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6.1 Revision History

Document Title: CY8C21234, CY8C21334, CY8C21434, CY8C21534, and CY8C21634 PSoC Mixed-Signal Array Final Data Sheet
Document Number: 38-12025

Revision	ECN #	Issue Date	Origin of Change	Description of Change
**	227340	5/19/2004	HMT	New silicon and document (Revision **).
*A	235992	See ECN	SFV	Updated Overview and Electrical Spec. chapters, along with revisions to the 24-pin pinout part. Revised the register mapping tables. Added a SSOP 28-pin part.
*B	248572	See ECN	SFV	Changed title to include all part #s. Changed 28-pin SSOP from CY8C21434 to CY8C21534. Changed pin 9 on the 28-pin SSOP from SMP pin to Vss pin. Added SMP block to architecture diagram. Update Electrical Specifications. Added another 32-pin MLF part: CY8C21634.
*C	277832	See ECN	HMT	Verify data sheet standards from SFV memo. Add Analog Input Mux to applicable pin outs. Update PSoC Characteristics table. Update diagrams and specs. Final.
*D	285293	See ECN	HMT	Update 2.7V DC GPIO spec. Add Reflow Peak Temp. table.
*E	301739	See ECN	HMT	DC Chip-Level Specification changes. Update links to new CY.com Portal.
*F	329104	See ECN	HMT	Re-add pinout ISSP notation. Fix TMP register names. Clarify ADC feature. Update Electrical Specifications. Update Reflow Peak Temp. table. Add 32 MLF E-PAD dimensions. Add ThetaJC to Thermal Impedance table. Fix 20-pin package order number. Add CY logo. Update CY copyright.
*G	352736	See ECN	HMT	Add new color and logo. Add URL to preferred dimensions for mounting MLF packages. Update Transmitter and Receiver AC Digital Block Electrical Specifications.
*H	390152	See ECN	HMT	Clarify MLF thermal pad connection info. Replace 16-pin 300-MIL SOIC with correct 150-MIL.
*I	413404	See ECN	HMT	Update 32-pin QFN E-Pad dimensions and rev. *A. Update CY branding and QFN convention.
*J	430185	See ECN	HMT	Add new 32-pin 5x5 mm 0.60 thickness QFN package and diagram, CY8C21434-24LKXI. Update thermal resistance data. Add 56-pin SSOP on-chip debug non-production part, CY8C21001-24PVXI. Update typical and recommended Storage Temperature per industrial specs. Update copyright and trademarks.

Distribution: External/Public **Posting**: None

6.2 Copyrights and Code Protection

Copyrights

Flash Code Protection Note the following details of the Flash code protection features on Cypress Semiconductor PSoC devices.

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