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ARLINGTON, VA 22201

TITLE: ~~ACTIVE MATRIX DISPLAY DEVICE AND A METHOD OF MANUFACTURING THE SAME~~ LIQUID CRYSTAL DISPLAY ELEMENT AND METHOD FOR TREATING DEFECTIVE PIXELS THEREIN

RT 4/29/93

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SEARCHED

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	334	8/6/91	RT
	332	8/7/91	RT
	331R	8/8/91	RT
340	784	8/7/91	RT
357	237	8/7/91	RT
350	351	8/8/91	RT
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	54	"	"
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UPDATED	ABOVE	8/19/92	RT
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345	93	2/7/94	RT

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INTERFERENCE SEARCHED

Class	Sub.	Date	Exmr.
359	54	4/29/93	RT
	58	"	"
	59	"	"
	87	"	"
257	72	"	"
340	784	4/29/93	RT
UPDATED	ABOVE	2/7/94	RT
345	93	2/7/94	RT

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SYMBOLS

R	Rejected
A	Allowed
(Through numeral)	Cancelled
O	Restricted
N	Non-elected
I	Interference
A	Appeal
O	Objected

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APPLICATION FOR UNITED STATES PATENT

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Invention: AN ACTIVE MATRIX DISPLAY DEVICE AND A METHOD OF MANUFACTURING THE SAME

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SPECIFICATION

ABSTRACT OF THE DISCLOSURE

An active matrix display device comprising: scanning branch lines each branching from the scanning line; and switching elements each formed on an end portion of the scanning branch line, wherein the distance between the scanning line side of the switching element and the scanning line is so provided as to enable the scanning branch line to be cut off by irradiation with light energy. Alternatively, an active matrix display device comprising: a conductive layer disposed under the signal line and the pixel electrode with an insulating film interposed therebetween; and a conductive piece formed between the pixel electrode and the insulating film.

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BACKGROUND OF THE INVENTION

1. Field of the Invention:

The present invention relates to a display device which performs its display function by applying driving signals to pixel electrodes via switching elements, and more particularly to an active matrix driving type display device which performs high-density display by using pixel electrodes arranged in a matrix pattern.

2. Description of the Prior Art:

In liquid crystal display devices, EL display devices, plasma display devices and the like, it is known how to produce a display pattern on a screen by selectively driving pixel electrodes arranged in a matrix pattern. In such display devices, voltage is applied between each selected pixel electrode and a counter electrode disposed facing it, to optically modulate a display medium such as liquid crystal or the like interposed between these electrodes. This optical modulation is recognized as a display pattern. As a method for driving pixel electrodes, an active matrix driving method is known in which independent pixel electrodes are arrayed and are driven via switching elements connected to the respective pixel electrodes. As the switching elements used to selectively drive the pixel electrodes, TFT (thin film transistor) elements, MIM (metal-insulator-metal) elements, MOS transistors, diodes, varistors, etc. are generally known. Because the active matrix driving method is capable of performing high contrast display, it has been put to practical use in liquid crystal televisions, word processors,

computer terminal displays and the like.

Figures 21 and 22 are plan views of active matrix substrates used in active matrix display devices according to a prior art. On the substrate shown in Figure 21, source bus lines 23 are disposed in parallel and intersecting at right angles with gate bus lines 21 which are arranged parallel with each other. A pixel electrode 41 is disposed in each rectangular area surrounded by two gate bus lines 21 and two source bus lines 23. On each gate bus line 21 and adjacent to the intersection of the gate bus line 21 and the source bus line 23, there is formed a TFT 31 which functions as a switching element, a portion of the gate bus line 21 functioning as the gate electrode of the TFT 31. The drain electrode of the TFT 31 is electrically connected to the pixel electrode 41, while a branch line branching from the source bus line 23 is connected to the source electrode of the TFT 31.

The active matrix substrate of Figure 22 is the same as that of Figure 21 except that the construction around the TFT 31 is different. In Figure 22, the TFT 31 is formed on a gate bus branch line 22 branching from the gate bus line 21, a portion of the gate bus branch line 22 functioning as the gate electrode of the TFT 31.

To achieve high-density display using such display devices, it is necessary to array a great number of pixel electrodes 41 and TFTs 31. However, there may be cases in which some TFTs 31 have been already formed as defective TFTs when they are formed

on a substrate. The pixel electrodes connected to such a defective TFT cause defective pixel elements that do not contribute to the display. Such defective pixel elements result in substantial damage to the image quality of the display device, and therefore, greatly reduces the product yield. Display devices having constructions to correct the defective TFTs are disclosed in Japanese Laid-Open Patent Publications Nos. 2-153324, 2-294623 and 2-254423. These display devices comprise spare TFTs which are connected to a pixel element electrode connected to the defective TFT.

There are two major cases of causes for the defective pixel elements. One is the failure to sufficiently charge the pixel electrode during the period in which the pixel electrode is selected by a scanning signal (hereinafter referred to as the "on-failure"). The other is a failure that causes the charge in the charged pixel electrode to leak during the period in which the pixel electrode is not selected (hereinafter referred to as the "off-failure"). The on-failure is attributable to a defective TFT. The off-failure is caused either by electrical leakage via the TFT or by electrical leakage between the pixel electrode and the bus line. In either causes of failure, since necessary voltage is not applied between the pixel electrode and the counter electrode, a defective pixel element is produced. When such failures occur, the defective pixel element appears as a bright spot in the normally white mode in which light transmittance is the highest when the voltage applied between the pixel electrode and the counter electrode is 0 V, and as a black spot in the normally black mode in which light transmittance

is the lowest when the voltage is 0 V.

Such a defective pixel element can be corrected by performing laser trimming, etc. However, correction of the defective pixel element must be done on an active matrix substrate before the substrate is assembled into a display device. It is easy to detect pixel defects after the display device has been assembled, but it is extremely difficult to detect pixel defects in an active matrix substrate before assembly, particularly in the case of a large-size display device having 100,000 to 500,000 pixels. Even if the detection and the correction of the defective pixel electrode can be achieved, it requires a high precision measuring instrument as disclosed in Japanese Laid-Open Patent Publication No. 1-144092. It involves a complicated inspection process and is detrimental to mass production efficiency to examine the electrical characteristics of all pixel electrodes and detect the defective TFTs. It therefore causes an increase in costs. For these reasons, as the situation stands now, it is not possible to correct defective pixels in an active matrix substrate before being assembled by the above-mentioned method using a laser beam in the case of large-size display devices having a great number of pixels.

SUMMARY OF THE INVENTION

The active matrix device of this invention, which overcomes the above-discussed and numerous other disadvantages and deficiencies of the prior art, comprises a pair of insulating substrates at least one of

which is light transmitting; scanning lines arranged on one of said pair of substrates; scanning branch lines each branching from said scanning line; and switching elements each formed on an end portion of said scanning branch line, wherein the distance between the scanning line side of said switching element and said scanning line is so provided as to enable said scanning branch line to be cut off by irradiation with light energy.

In a preferred embodiment, the active matrix display device further comprises a pixel electrode connected to said switching element and a supplemental capacitor electrode disposed opposite to said pixel electrode with an insulating film interposed therebetween, a supplemental capacitor being formed between said pixel electrode and said supplemental capacitor electrode.

In a preferred embodiment, the active matrix display device further comprises a pixel electrode connected to said switching element and disposed opposite to a scanning line adjacent to said scanning line with an insulating film interposed therebetween, a supplemental capacitor being formed at the superimposing portion of said pixel electrode and said adjacent scanning line.

Alternatively, the active matrix display device of this invention comprises: a pair of insulating substrates at least one of which is light transmitting; scanning lines arranged on one of said pair of substrates; scanning branch lines each branching from said scanning line; and switching elements each formed

on an end portion of said scanning branch line, wherein a portion of said scanning branch line other than the portion thereof where said switching element is formed is narrower than that of the portion thereof where said switching element is formed.

In a preferred embodiment, said narrower width portion is formed by cutting one or the other side of a portion of said scanning branch line other than the portion thereof where said switching element is formed.

In a preferred embodiment, the active matrix display device further comprises a pixel electrode connected to said switching element and a supplemental capacitor electrode disposed opposite to said pixel electrode with an insulating film interposed therebetween, a supplemental capacitor being formed between said pixel electrode and said supplemental capacitor electrode.

In a preferred embodiment, the active matrix display device further comprises a pixel electrode connected to said switching element and disposed opposite to a scanning line adjacent to said scanning line with an insulating film interposed therebetween, a supplemental capacitor being formed at the superimposed portion of said pixel electrode and said adjacent scanning line.

The method of manufacturing an active matrix display device of this invention comprises the steps of: forming an active matrix substrate which comprises

an insulating substrate, scanning lines and signal lines arranged in vertical and horizontal directions on said substrate, scanning branch lines each branching from said scanning line, switching elements each formed on an end portion of said scanning branch line, and pixel electrodes each connected to said switching element, the distance between the scanning line side of said switching element and said scanning line being so provided as to allow said scanning branch line to be cut off by irradiation with light energy; attaching an opposing substrate to said active matrix substrate with a display medium sandwiched between said active matrix substrate and said opposing substrate; detecting a pixel defect by applying a driving voltage to said pixel electrodes from said scanning lines and said signal lines via said switching elements; and irradiating light energy onto the switching element connected to a defective pixel electrode causing said pixel defect to electrically connect said defective pixel electrode to said signal line, and irradiating light energy onto said scanning branch line to disconnect said scanning branch line from said scanning line.

Alternatively, the active matrix display device comprises a pair of insulating substrates at least one of which is light transmitting; scanning lines and signal lines arranged in vertical and horizontal directions on one of said pair of substrates; and pixel electrodes each connected to said scanning line and said signal line via a switching element. The active matrix display device further comprises a conductive layer disposed under said signal line and said pixel electrode with an insulating film interposed

therebetween; and a conductive piece formed between said pixel electrode and said insulating film.

Alternatively, the active matrix display device comprises: a pair of insulating substrates at least one of which is light transmitting; scanning lines and signal lines arranged in vertical and horizontal directions on one of said pair of substrates; and pixel electrodes each connected to said scanning line and said signal line via a switching element. The active matrix display device further comprises a conductive layer disposed under said signal line and a pair of adjacent pixel electrodes with an insulating film interposed therebetween; and conductive pieces each formed between said insulating film and one of said pair of pixel electrodes.

In a preferred embodiment, said conductive layer is electrically connected to a scanning line adjacent to said scanning line connected to said pixel electrode with an anodic oxide film formed on said conductive layer.

In a preferred embodiment, the active matrix display device further comprises a supplemental capacitor electrode disposed opposite to said pixel electrode with said insulating film interposed therebetween, wherein said conductive layer is electrically connected to said supplemental capacitor electrode, and an anodic oxide film is formed on said conductive layer.

The method of manufacturing an active matrix display device of this invention comprises the steps

of: forming an active matrix substrate which comprises an insulating substrate, scanning lines and signal lines arranged in vertical and horizontal directions on said substrate, pixel electrodes each connected to said scanning line and said signal line via a switching element, conductive layers each disposed under said signal line and said pixel electrode with an insulating film interposed therebetween, and conductive pieces each formed between said pixel electrode and said insulating film; attaching an opposing substrate to said active matrix substrate with a display medium sandwiched between said active matrix substrate and said opposing substrate; detecting a pixel electrode by applying a driving voltage to said pixel electrodes from said scanning lines and said signal lines via said switching elements; and irradiating light energy onto the superimposed portion of said conductive layer and said conductive piece connected to a defective pixel electrode causing said pixel defect to electrically connect said defective pixel electrode to said conductive layer, and irradiating light energy onto the superimposed portion of said signal line and said conductive layer to electrically connect said signal line to said conductive layer.

In the active matrix display device of the present invention, when an on-failure or off-failure occurs because of a defective switching element, occurrence of a weak leakage current between a signal line and a pixel electrode, or the other reasons, the defective pixel can be corrected in an assembled display device. First, the scanning branch line concerned is cut off by irradiating a laser beam. In the display

device of the present invention, the distance between the scanning line side of a switching element and the scanning line is so provided as to allow the scanning branch line to be cut off by irradiation of light energy such as a laser beam or the like. Also, in another embodiment of the present invention, the scanning branch line is provided with a portion having a reduced width so as to facilitate the cutting thereof by laser beam irradiation. Therefore, in the display device of the present invention, the scanning branch line can be reliably cut off.

Next, light energy is irradiated to electrically interconnect the electrode of the switching element connected to the pixel electrode and the electrode thereof connected to the signal line. When the switching element is a TFT, the electrical interconnection is made by irradiating light energy onto the superimposed portion of the source electrode and the gate electrode and also onto the superimposed portion of the drain electrode and the gate electrode. When a laser beam is used as the light energy, a spot-like hole is made in each of the superimposed portions. Around these holes, the source electrode is electrically connected to the gate electrode and the drain electrode is electrically connected to the gate electrode. Thus, the source electrode and the drain electrode are electrically interconnected via the gate electrode.

In an active matrix display device having the conductive layer and the conductive piece of the present invention, when an on-failure or off-failure occurs because of a defective switching element, occur-

rence of a weak leakage current between a signal line and a pixel electrode, or the other reasons, the defect can be corrected in an assembled display device. First, light energy is irradiated onto the superimposed portion of the signal line and the conductive layer to electrically interconnect the signal line and the conductive layer. Next, light energy is projected onto the superimposed portion of the conductive layer and the conductive piece to electrically interconnect the conductive layer and the conductive piece. Thus, the signal line and the pixel electrode are directly interconnected electrically without interposition of the switching element. Further, in the construction in which the conductive layer is electrically connected to the scanning line or to the supplemental capacitor electrode, the electrical connection between the conductive layer and the scanning line or the supplemental capacitor electrode is cut by irradiating light energy.

Referring now to Figure 20, It will be explained how the voltage is applied to the pixel electrode which has been directly connected to the signal line in the above manner (hereinafter referred to as the "corrected pixel electrode"). In Figure 20, G_n represents the relationship of the signal voltage (plotted along the ordinate) on the n-th scanning line with respect to the time (plotted along the abscissa) while S_m illustrates the relationship of the signal voltage (plotted along the ordinate) on the m-th signal line with respect to the time (plotted along the abscissa). $P_{n,m}$ indicates the voltage applied to a normal pixel electrode connected to the n-th scanning line and the m-th signal line. $P'_{n,m}$ indicates the

voltage applied to a corrected pixel electrode connected to the n-th scanning line and the m-th signal line.

As shown in G_n and G_{n+1}, a signal (V_{gh}) for sequentially selecting the switching elements is output on the scanning line during a selection time T_{on}. Corresponding to the selection time T_{on} on the scanning line, a video signal voltage V_0 is output on the signal line, and in the case of a normal pixel electrode, the video signal voltage V_0 is held during a non-selection time T_{off} as shown in $P_{n,m}$. Then, when the next selection signal voltage V_{gh} is applied, a video signal $-V_0$ is applied to the signal line.

On the other hand, in the case of a corrected pixel electrode, since the video signal from the signal line is applied all the time as shown in $P'_{n,m}$, the corrected pixel electrode is unable to function properly. However, when the entire cycle is viewed, the pixel driven by the corrected pixel electrode produces a display corresponding to the root-mean-square value of the video signal applied to the signal line during that one cycle. Therefore, the pixel does not appear as a complete bright spot or black spot but produces a display having the average brightness of the pixels arrayed along the signal line. Thus, the defect of the pixel is made extremely difficult to discern.

It is required that the connections made in the above manner have an electrical resistance lower than the resistance of the switching element in a selected condition (hereinafter referred to as the "on-state resistance"). The reason is believed to be

as follows: The on-state resistance of the switching element is determined so that a current enough to charge the pixel electrode flows during the time in which the switching element is selected. Therefore, if the resistance at the above connection is higher than the on-state resistance, the signal voltage varying at every selection time of the switching element will not be completely written in the corrected pixel electrode, reducing the root-mean-square value of the voltage applied to the corrected pixel electrode. In such a condition, the difference in brightness increases between the pixel driven by the corrected pixel electrode and the normally operating pixels, so that the pixel defect becomes visually discernible.

Thus, it is an object of the present invention to provide an active matrix display device in which any pixel defect can be corrected to an undiscernible level within the assembled display device itself. It is another object of the present invention to provide a method of manufacturing an active matrix display device in which any pixel defect can be corrected to an undiscernible level in an assembled display device.

In the active matrix display device of the present invention, any pixel defect can be corrected to an undiscernible level with the display device in an assembled condition under which the pixel defect is easy to detect. Therefore, according to the present invention, the display device can be manufactured at a high yield ratio, thus contributing to a reduction of the cost of the display device.

BRIEF DESCRIPTION OF THE DRAWINGS

This invention may be better understood and its numerous objects and advantages will become apparent to those skilled in the art by reference to the accompanying drawings as follows:

Figure 1 is a plan view of an active matrix substrate used in an active matrix display device of the present invention.

Figure 2 is an enlarged plan view of a TFT and its adjacent portions as shown in Figure 1.

Figure 3 is a cross sectional view of a display device using the substrate of Figure 1, taken along line S-S in Figure 1.

Figures 4 and 5 are plan views of other embodiments each having a supplemental capacitor.

Figure 6 is a plan view showing an embodiment with a gate bus branch line having a reduced width portion.

Figure 7 is an enlarged plan view of the TFT and its adjacent portions shown in Figure 6.

Figure 8A and Figure 8B are plan views of gate bus branch lines in other embodiments of the present invention.

Figures 9 and 10 are plan views of other embodiments each having a supplemental capacitor.

Figure 11 is a plan view of an embodiment having a conductive layer and a conductive piece.

Figure 12A is an enlarged plan view of a portion where the conductive layer of Figure 11 is formed.

Figure 12B is a cross sectional view taken along line P-P in Figure 11.

Figure 13A to Figure 13C, Figure 14A and Figure 14B, and Figure 15 are plan views of other embodiments each having a conductive layer and a conductive piece.

Figures 16 to 19 are plan views of other embodiments of the present invention each having a supplemental capacitor.

Figure 20 is a diagram showing the relationship of the signal applied to a scanning line and a signal line with respect to the voltage applied to a pixel electrode.

Figures 21 and 22 respectively are plan views of active matrix substrates used in prior art active matrix display devices.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1 shows a plan view of an active matrix substrate used in one embodiment of the display device of the present invention. Figure 3 shows a cross sectional view of a display device using the substrate of Figure 1, taken along line S-S in Figure 1. The following describes the active matrix display device of this embodiment in the sequence of its manufacturing steps. In this embodiment, a transparent glass substrate is used as the insulating substrate. There are formed on the glass substrate 1 a gate bus line 21 which functions as a scanning line and a gate bus branch line 22 which branches from the gate bus line 21. Generally, the gate bus line 21 and the gate bus branch line 22 are formed from a single or multiple layer of such metals as Ta, Ti, Al, Cr, etc. In this embodiment, Ta is used as the material. The gate bus line 21 and the gate bus branch line 22 are formed by patterning the Ta metal layer deposited by using a sputtering method. A base coat film formed from Ta_2O_5, etc. may be formed on the glass substrate 1 prior to the formation of the gate bus line 21 and the gate bus branch line 22. The length of the gate bus branch line will be described later.

A base insulating film 11 made of SiN_x is formed all over the surface covering the gate bus line 21 and the gate bus branch line 22. The gate insulating film 11 is deposited to a thickness of 3000 Å using the plasma CVD technique.

Next, a TFT 31 which functions as a switching element is formed at an end portion of the gate bus branch line 22. A portion of the gate bus branch line 22 functions as the gate electrode 25 of the TFT 31. After forming the gate insulating film 11 as described above, an amorphous silicon (a-Si) layer which is later formed as a channel layer 12 and an SiN_x layer which is later formed as an etching stopper layer 13 are deposited. The thickness of the a-Si layer is 300 Å, and that of the SiN_x layer is 2000 Å. Next, the SiN_x layer is patterned to form the etching stopper layer 13. Furthermore, over the entire surfaces of the a-Si layer and the etching stopper layer 13, an n^+-a-Si layer doped with P (phosphorus) which is later formed as contact layers 14 and 14 is deposited to a thickness of 800 Å using the plasma CVD technique. After that, the a-Si layer and the n^+-a-Si layer are simultaneously patterned to form the channel layer 12 and the contact layers 14 and 14.

Next, a Ti metal layer is formed which is later formed as a source electrode 32, a source bus line 23 to function as a signal line, and a drain electrode 33. Generally, the source bus line 23 and others are formed from a single or multiple layers of such metals as Ti, Al, Mo, Cr, etc. In this embodiment, Ti is used as the material. The Ti metal layer is deposited by sputtering. The Ti metal layer is patterned to form the source electrode 32, the source bus line 23, and the drain electrode 33. The source bus line 23 and the gate bus line 21 intersect each other with the gate insulating film 11 interposed therebetween.

Next, a pixel electrode 41 made of ITO (indium tin oxide) is formed in a rectangular area surrounded by the gate bus line 21 and the source bus line 23, as shown in Figure 1. The pixel electrode 41 is superimposed on an end portion of the drain electrode 33 of the TFT 31 for electrical connection to the drain electrode 33.

Further, over the entire surface of the substrate on which the TFT 31 and the pixel electrode 41 are formed, a protective film 17 made of SiN_x is deposited. The protective film 17 may be formed in the shape of a window opened above the central portion of the pixel electrode 41. An orientation film 19 is formed over the protective film 17. On a glass substrate 2 disposed opposite to the glass substrate 1, there are formed a counter electrode 3 and an orientation film 9. A liquid crystal layer 18 is sandwiched between the substrates 1 and 2 to complete the active matrix display device of the present invention.

The construction around the TFT 31 will now be explained. Figure 2 shows an enlarged view of the TFT 31 and its adjacent portions. As previously described, the TFT 31 is formed on the gate bus branch line 22 branching from the gate bus line 21. The drain electrode 33 of the TFT 31 is electrically connected to the pixel electrode 41 while the source electrode 32 thereof is electrically connected to the source bus line 23. The distance X between the side of the TFT 31 nearer to the gate bus line 21 and the gate bus line 21 is greater than that in the prior art previously described in connection with Figure 22, so as to allow

the gate bus branch line 22 to be cut off using light energy such as a laser beam or the like. It has been confirmed that the line can be cut off reliably if the distance X is 10 μm or more. If the distance X is smaller than 10 μm, it not only makes it impossible to cut off the gate bus branch line 22 without damaging the TFT 31 but also gives rise to a possibility that the irradiation by a laser beam may adversely affect the intersection of the gate bus line 21 and the source bus line 23 and may cause insulation failure between the bus lines 21 and 23.

In the active matrix display device of the above construction, when the TFT 31 becomes defective or when a weak leakage current flows between the source bus line 23 and the pixel electrode 41, a pixel defect occurs. If this happens, correction is made in the following manner. First, light energy is irradiated onto an area 51 indicated by a broken line in Figure 2 to cut off the gate bus branch line 22. The gate bus branch line 22 is thus electrically isolated from the gate bus line 21. In this embodiment, a YAG laser beam is used as the light energy. As described, since the distance X is sufficiently large, the gate bus branch line 22 can be cut off reliably. The laser beam may be irradiated either through the substrate 1 or through the substrate 2. When a light shield film is formed on the substrate 2, which is often the case, the laser beam is irradiated through the substrate 1. In this embodiment also, the laser beam is irradiated through the substrate 1. Next, the laser beam is irradiated onto areas 52 and 53 indicated by broken lines in Figure 2, that is, onto the portions indicated by

arrows 26 and 27 in Figure 3. As a result, the source electrode 32 and the gate electrode 25 are electrically interconnected at the area 52, while at the area 53 the drain electrode 33 and the gate electrode 25 are electrically interconnected. Thus, the source electrode 32 and the drain electrode 33 are electrically interconnected via the gate electrode 25.

Since the signal from the source bus line 23 is applied at all times to the pixel electrode 41 (corrected pixel electrode) connected to the TFT 31 corrected in the above manner, the corrected pixel electrode is unable to function properly. However, since the pixel driven by the corrected pixel electrode performs a display corresponding to the root-mean-square value of the signal applied to the source bus line 23, the pixel does not appear as a complete bright spot or black spot but performs display having the average brightness of the pixels arrayed along the source bus line 23. Thus, the defect of the pixel is made extremely difficult to discern.

Even if the laser beam irradiates as described above, since the protective film 17 is formed over the gate bus branch line 22 and the TFT 31, molten metals or other foreign matter are prevented from entering the display medium, i.e. the liquid crystal layer 18, and therefore, no detrimental effects are caused to the display. Also, it has been found that by changing the irradiating conditions of the laser beam, the same laser beam can be used for melting and interconnecting the metal layers as well as for cutting the metal layers.

Also, in the above correction work, interconnections between the gate electrode 25, source electrode 32, and drain electrode 33 of the TFT 31 may be made prior to the cutting of the gate bus branch line 22.

The construction of the present invention may also be applied to an active matrix display device having a supplemental capacitor 42 as shown in Figure 4. The display device of Figure 4 is identical to the foregoing embodiment illustrated in Figures 1 to 3, except that the supplemental capacitor 42 is provided. The supplemental capacitor 42 is formed on the superimposed portion (shaded portion) of the pixel electrode 41 and a supplemental capacitor electrode 24 disposed on the substrate 1 in parallel with the gate bus line 21. In the display device of Figure 4 also, pixel defects can be corrected in the same manner as in the foregoing embodiment illustrated in Figures 1 to 3.

Furthermore, the present invention can be applied to an active matrix display device having a construction like that shown in Figure 5. The display device shown is so constructed as to prevent the opening area from being reduced by the provision of the supplemental capacitor 42 which is the case with the display device of Figure 4. That is, in the display device of Figure 5, the gate bus line 21 is enlarged in width so as to be superimposed on a portion of the pixel electrode 41. According to this construction, the adjacent gate bus line 21 which is in a non-selected condition can be used as the supplemental capacitor electrode. Further, since no gap is created between

the gate bus line 21 and the supplemental capacitor electrode 24 unlike the construction of Figure 4, the opening area is prevented from being reduced. In this display device also, pixel defects can be corrected in the same manner as in the foregoing embodiment illustrated in Figures 1 to 3.

Figure 6 shows a plan view of an active matrix substrate used in another embodiment of the display device of the present invention. This embodiment has the same construction as that of the embodiment illustrated in Figure 1, except that the shape of the gate bus branch line 22 is different when viewed from the top. The cross sectional view of a display device using the substrate of Figure 6, taken along line R-R in Figure 6, is the same as shown in Figure 3 previously described. Referring to Figure 7, the construction around the TFT 31 of this embodiment will be now explained. As previously described, the TFT 31 is formed on the gate bus branch line 22 branching from the gate bus line 21. The drain electrode 33 of the TFT 31 is electrically connected to the pixel electrode 41 while the source electrode 32 thereof is electrically connected to the source bus line 23. A portion of the gate bus branch line 22 other than the portion thereof where the TFT 31 is formed has a width narrower than that of the portion thereof where the TFT 31 is formed. By providing such a narrower width portion, it is possible to make the distance Y between the pixel electrode 41 and the gate bus branch line 22 larger than that in the prior art previously illustrated with reference to Figure 22. The provision of a sufficiently long distance Y allows the gate bus branch line 22

to be cut off more easily and reliably using light energy such as a laser beam or the like. It has been confirmed that the line can be cut off reliably if the distance Y is 10 μm or more. If the distance Y is smaller than 10 μm, it not only makes it impossible to cut off the gate bus branch line 22 without damaging the TFT 31 but also gives rise to a possibility that the irradiation by laser beam may adversely affect the intersection of the gate bus line 21 and the source bus line 23 and may cause insulation failure between the bus lines 21 and 23.

In the active matrix display device of the above construction, when the TFT 31 becomes defective or when a weak leakage current flows between the source bus line 23 and the pixel electrode 41, a pixel defect occurs. If this happens, the defect is corrected in the same manner as in the foregoing embodiment illustrated in Figure 1. First, light energy is irradiated onto an area 51 indicated by a broken line in Figure 7, to cut off the gate bus branch line 22. As a result, the gate bus branch line 22 is electrically isolated from the gate bus line 21. As previously described, since the gate bus branch line 22 has a portion where the width is narrower than the portion thereof on which the TFT 31 is formed, the gate bus branch line 22 can be cut off easily and reliably. Next, the laser beam is irradiated onto areas 52 and 53 indicated by broken lines in Figure 7. As a result, the source electrode 32 and the drain electrode 33 are electrically interconnected via the gate electrode 25.

The signal from the source bus line 23 is applied at all times to the pixel electrode 41 (corrected pixel electrode) connected to the TFT 31 corrected in the above manner. Therefore, the pixel defect is made extremely difficult to discern.

The gate bus branch line 22, when viewed from the top, may be formed as shown in Figure 8A or Figure 8B. In the gate bus branch line 22 shown in Figure 8A, the portion having a reduced width is formed by removing a portion from the pixel electrode 41 side of the gate bus branch line 22 shown in Figure 4. Likewise, in the gate bus branch line 22 shown in Figure 8B, the portion having a reduced width is formed by removing a portion from the source bus line 23 side of the gate bus branch line shown in Figure 21.

The present invention may also be applied to an active matrix display device having a supplemental capacitor 42 as shown in Figure 9. The display device of Figure 9 is identical to the foregoing embodiment illustrated in Figure 6, except that a supplemental capacitor 42 is provided. The supplemental capacitor 42 is formed on the superimposed portion (shaded portion) of the pixel electrode and a supplemental capacitor electrode 24 that is disposed on the substrate 1 in parallel with the gate bus line 21. In the display device of Figure 5 also, pixel defects can be corrected in the same manner as in the foregoing embodiment illustrated in Figure 6.

Furthermore, the present invention can be applied to an active matrix display device having a

construction as shown in Figure 10. The display device shown is so constructed as to prevent the opening area from being reduced by the provision of the supplemental capacitor 42 which is the case with the display device of Figure 9. That is, in the display device of Figure 10, the gate bus line 21 is enlarged in width so as to be superimposed on a portion of the pixel electrode 41. According to this construction, the adjacent gate bus line 21 which is in a non-selected condition can be used as the supplemental capacitor electrode. Further, since no gap is created between the gate bus line 21 and the supplemental capacitor electrode 24 unlike the construction of Figure 9, the opening area is prevented from being reduced. In this display device also, pixel defects can be corrected in the same manner as in the foregoing embodiment illustrated in Figure 6.

Any of the embodiments shown in Figures 1 to 10 uses a TFT as the switching element. For the embodiments of Figures 1 to 10, there can be used any switching element as long as the signal line side electrode and the pixel electrode side electrode thereof can be electrically interconnected by irradiating light energy such as a laser beam or the like.

Figure 11 shows a plan view of an active matrix substrate in still another embodiment of the present invention. Figure 12A is a view of an enlarged portion of a conductive layer 34 of Figure 11, and Figure 12B shows a cross sectional view taken along line P-P in Figure 11. The cross sectional view of a display device using the substrate of Figure 11, taken along line Q-Q in Figure 11, is the same as shown in

Figure 3 previously described. The following describes the active matrix display device of this embodiment in the sequence of its manufacturing steps. A gate bus line 21, a gate bus branch line 22 branching from the gate bus line 21, and a conductive layer 34 are simultaneously formed on a glass substrate 1. Generally, the gate bus line 21 and the gate bus branch line 22 are formed from a single or multiple layers of such metals as Ta, Ti, Al, Cr, etc. In this embodiment, Ta is used as the material. The conductive layer 34 is formed from the same metal as used for the gate bus line 21. The gate bus line 21, the gate bus branch line 22, and the conductive layer 34 are formed by patterning the Ta metal layer which is formed by sputtering. A base coat film formed from Ta_2O_5 or the like may be formed on the glass substrate 1 prior to the formation of the gate bus line 21, the gate bus branch line 22, and the conductive layer 34.

A base insulating film 11 made of SiN_x is formed over the entire surface covering the gate bus line 21, the gate bus branch line 22, and the conductive layer 34. The gate insulating film 11 is deposited to a thickness of 3000 Å using the plasma CVD technique.

Next, a TFT 31 is formed on an end portion of the gate bus branch line 22 with a portion of the gate bus branch line 22 functioning as the gate electrode 25 of the TFT 31. After forming the gate insulating film 11 as describe above, a-Si layer which is later formed as a channel layer 12 and an SiN_x layer which is later formed as an etching stopper layer 13 are deposited.

Next, a pixel electrode 41 made of ITO (indium tin oxide) is formed in a rectangular area surrounded by the gate bus line 21 and the source bus line 23, as shown in Figure 11. The pixel electrode 41 is superimposed on an end portion of the drain electrode 33 of the TFT 31 for electrical connection to the drain electrode 33. The pixel electrode 41 is also formed so as to be superimposed on the conductive piece 35, as shown in Figure 12B.

Further, over the entire surface of the substrate on which the pixel electrode 41 are formed, a protective film 17 made of SiN_x is deposited. The protective film 17 may be formed in the shape of a window opened above the central portion of the pixel electrode 41. An orientation film 19 is formed over the protective film 17. On a glass substrate 2 disposed opposite to the glass substrate 1, there are formed a counter electrode 3 and an orientation film 9. A liquid crystal layer 18 is charged between the substrates 1 and 2 to complete the active matrix display device of the present invention.

In the active matrix display device of the above construction, when the TFT 31 becomes defective or when a weak leakage current flows between the source bus line 23 and the pixel electrode 41, a pixel defect occurs. If this happens, correction is made in the following manner. First, light energy is irradiated onto a superimposed region 61 of the source bus line 23 and the conductive layer 34, the region being indicated by a broken line in Figure 12A (a portion indicated by an arrow 65 in Figure 12B), and also onto a superim-

posing region 62 of the conductive layer 34 and the conductive piece 35 (a portion indicated by an arrow 64 in Figure 12B). As a result, the source bus line 23, the conductive layer 34, and the conductive piece 35 are electrically interconnected. Since the conductive piece 35 is electrically connected to the pixel electrode 41, the pixel electrode 41 is now connected electrically to the source bus line 23. In this embodiment also, a YAG laser beam (wave length: 1064 nm) is used as the light energy. The laser beam may irradiate either through the substrate 1 or through the substrate 2 (Figure 3). When a light shield film is formed on the substrate 2, which is often the case, the laser beam irradiates through the substrate 1. In this embodiment also, the laser beam irradiates through the substrate 1.

Since the signal from the source bus line 23 is applied at all times to the pixel electrode 41 (corrected pixel electrode) via the conductive layer 34, the corrected pixel electrode is unable to function properly. However, since the pixel driven by the corrected pixel electrode performs a display corresponding to the root-mean-square value of the signal applied to the source bus line 23, the pixel does not appear as a complete bright spot or black spot but performs a display having the average brightness of the pixels arrayed along the source bus line 23. Thus, the pixel defect is made extremely difficult to discern.

Even if the laser beam is irradiated as described above, since the protective film 17 is formed over the superimposing area of the conductive layer 34

and the source bus line 23 as well as over the superposed area of the conductive layer 34 and the conductive piece 35, molten metals or other foreign matter are prevented from entering the display medium, i.e. the liquid crystal layer 18, and therefore, no detrimental effects are caused to the display.

Figure 13A to Figure 13C show other embodiments of active matrix substrates each used in the display device of the present invention. In the substrate of Figure 13A, the source bus line 23 is provided with a projection 23a which is superimposed on the conductive layer 34. Other construction including the conductive piece 35, etc. is the same as that of Figure 11.

In the embodiment illustrated in Figure 11, the conductive layer 34 and the conductive piece 35 are disposed spaced apart from the TFT 31, but may be disposed at any position as long as they are positioned adjacent to the source bus line 23. Figure 13B shows an example in which the conductive layer 34 is formed adjacent to the TFT 31.

In the embodiment shown in Figure 13C, a source bus branch line 23b is formed which branches from the source bus line 23. The conductive layer 34 is formed in parallel with the source bus line 23 and the source bus branch line 23b is superimposed on the conductive layer 34.

In a display device using any of the substrates of Figure 13A to Figure 13C, pixel defects are

corrected in the same manner as in the foregoing embodiment illustrated in Figure 11. Although not shown, it is also possible to employ a construction in which the conductive layer 34, the conductive piece 35, etc. are disposed at the side of the source bus line 23 disposed opposite to the source bus line 23 shown in Figure 13A to Figure 13C across the pixel electrode 41.

Figure 14A and Figure 14B show other embodiments of active matrix substrates each used in the display device of the present invention. In the active matrix substrates illustrated in Figure 11 and Figure 13A to Figure 13C, since only the gate insulating film 11 is provided between the conductive layer 34 and the source bus line 23, spontaneous shorts may occur between the source bus line 23 and the conductive layer 34 and between the conductive layer 34 and the conductive piece 35. The active matrix substrates shown in Figure 14A and Figure 14B are designed to eliminate this problem. The conductive layer 34 on the substrate of Figure 14A is formed in such a way as to be connected to the gate bus line 21 disposed adjacent to the gate bus line connected to the pixel electrode 41 which is superimposed on the conductive layer 34. In many cases, an anodic oxide film is formed on the gate bus line 21 to ensure the insulation thereof. When the conductive layer 34 is formed in such a way as to be connected to the gate bus line 21, as in these embodiments, an anodic oxide film can also be formed on the conductive layer 34. When an anodic oxide film is formed on the conductive layer 34, it serves to prevent shorts between the source bus line 23 and the conductive layer 34 and between the conductive layer 34 and

the conductive piece 35.

In the substrate of Figure 14B, the conductive layer 34 and the conductive piece 35 are disposed in a corner opposite to the corner in which the TFT 31 is formed. Therefore, in this embodiment, the conductive layer 34 is superimposed by the source bus line 23 disposed adjacent to the source bus line connected to the pixel electrode which is superimposed on the conductive layer 34.

When a pixel defect has occurred in the display device using any of the substrates of Figure 14A and Figure 14B, connections are made between the conductive layer 34 and the source bus line 23 and between the conductive layer 34 and the conductive piece 35, in the same manner as in the foregoing embodiment illustrated in Figure 11. Further, in these substrates, light energy is irradiated onto an area 63 indicated by broken lines in Figure 14A and Figure 14B, to cut off the connection between the conductive layer 34 and the gate bus line 21. As a result of the above connections and cutting by irradiation with light energy, the pixel electrode 41 is directly connected to the source bus line 23. When the above correction has been made, on the substrate of Figure 14A, the pixel electrode 41 becomes directly connected to the source bus line 23 to which it was connected via the TFT 31, as in the case of the substrate of Figure 11, but on the substrate of Figure 14A, the pixel electrode 41 becomes connected to the source bus line disposed adjacent to the source bus line 23 to which it was connected via the TFT 31.

Figure 15 shows another embodiment of an active matrix substrate used in the display device of the present invention. In this embodiment, the conductive layer 34 is formed below two adjacent pixel electrodes 41a, 41b and the source bus line 23. In this embodiment, a single conductive layer 34 is provided for each pair of pixel electrodes. Conductive pieces 35a and 35b are formed on the respective end portions of the conductive layer 34 with the gate insulating film 11 interposed therebetween. The pixel electrodes 41a and 41b are superimposed directly on the conductive pieces 35a and 35b, respectively. Also, the conductive layer 34 is formed in such a way as to be connected electrically to the gate bus line 21 disposed adjacent to the gate bus line connected to the pixel electrodes 41a and 41b superimposed on the conductive layer 34. Since the conductive layer 34 is formed in such a way as to be connected to the gate bus line 21, an anodic oxide film can be formed on the conductive layer 34.

When a defect has occurred to the pixel electrode 41a or 41b in the display device using the substrate of Figure 15, a laser beam is irradiated first onto the superimposed portion of the source bus line 23 and the conductive layer 34. Then, the laser beam is irradiated onto the superimposed portion of the conductive layer 34 and the conductive piece 35a in the case of a defect in the pixel electrode 41a, and onto the superimposing portion of the conductive layer 34 and the conductive piece 35b in the case of a defect in the pixel electrode 41b. Furthermore, the laser beam is irradiated onto an area 63 indicated by a broken line in Figure 15, to cut off the electrical connection

between the conductive layer 34 and the gate bus line 21. As a result of the above correction, the defective pixel electrode 41a or 41b is directly connected to the source bus line 23.

When both pixel electrodes 41a and 41b are defective simultaneously, both pixel electrodes 41a and 41b are directly connected to the source bus line 23 to correct the respective defects. In the construction of this embodiment, the conductive layer 34 is connected to the gate bus line 21, but it may be so constructed that the conductive layer 34 is not connected to the gate bus line 21.

The construction of the present invention may also be applied to an active matrix display device having a supplemental capacitor as shown in Figure 16. The display device of Figure 16 is identical to the foregoing embodiment illustrated in Figure 13B, except that the supplemental capacitor 42 is provided. The supplemental capacitor 42 is formed on the superimposed area of the pixel electrode 41 and a supplemental capacitor electrode 24 which is disposed on the substrate 1 in parallel with the gate bus line 21. In the display device of Figure 16, pixel defects can also be corrected in the same manner as in the foregoing embodiment illustrated in Figure 11. The conductive layer 34, the conductive piece 35, and the source bus line 23 may also be constructed such as shown in Figure 11, Figure 13A, and Figure 13C. Furthermore, the conductive layer 34 and the conductive piece 35 shown in Figure 16 may also be constructed such as shown in Figure 14A, Figure 14B, and Figure 15. When the con-

ductive layer 34 and the conductive piece 35 are constructed such as shown in these figures, the conductive layer 34 is electrically connected to the supplemental capacitor electrode 24, not to the gate bus line 21. As an example, a substrate is shown in Figure 18 in which the conductive layer 34 and the conductive piece 35 are constructed such as shown in Figure 15. In the active matrix substrate shown in Figure 18, the conductive layer 34 is formed in such a way as to be connected to the supplemental capacitor electrode 24. In many cases, an anodic oxide film is also formed on the supplemental capacitor electrode 24. Therefore, with the conductive layer 34 connected to the supplemental capacitor electrode 24, it is possible to form an anodic oxide film also on the conductive layer 34.

Further, the present invention can be applied to an active matrix display device having a supplemental capacitor 42 as shown in Figure 17. The display device shown is designed so that the opening area is prevented from being reduced by the provision of the supplemental capacitor 42 which is the case with the display device of Figure 16. That is, in the display device of Figure 17, the gate bus line 21 is enlarged in width so that the pixel electrode 41 is superimposed on the gate bus line 21. According to this construction, the adjacent gate bus line 21 which is in a non-selected condition can be used as the supplemental capacitor electrode. Furthermore, since no gap is created between the gate bus line 21 and the supplemental capacitor electrode 24 unlike the construction of Figure 16, the opening area can be prevented from being reduced. In this display device also, pixel defects

are corrected in the same manner as in the foregoing embodiment illustrated in Figure 11. In the embodiment of Figure 17 also, the conductive layer 34, the conductive piece 35, and the source bus line 23 may be constructed such as shown in Figure 11, Figure 13A, and Figure 13C. Further, the conductive layer 34 and the conductive piece 35 in Figure 17 may also be constructed such as shown in Figure 14A, Figure 14B, and Figure 15. As an example, a substrate is shown in Figure 19 in which the conductive layer 34 and the conductive piece 35 in Figure 17 are constructed such as shown in Figure 15.

In any of the above embodiments, the TFT 31 shown has a gate electrode in the lower portion and a source electrode and a drain electrode in the upper portion, but alternatively, a TFT having a gate electrode in the upper portion and a source electrode and a drain electrode in the lower portion can be used. Also, in the embodiments of Figures 11 to 19, the TFT 31 is formed on the gate bus branch line 22, but alternatively, the TFT 31 may be formed on the gate bus line 21 with the source electrode thereof connected to the branch line branching from the source bus line 23.

Furthermore, any of the embodiments shown in Figures 11 to 19 uses a TFT as the switching element, but devices other than TFTs, such as MIM elements, MOS transistors, diodes, varistors, etc. may also be used.

It is understood that various other modifications will be apparent to and can be readily made by those skilled in the art without departing from the

scope and spirit of this invention. Accordingly, it is not intended that the scope of the claims appended hereto be limited to the description as set forth herein, but rather that the claims be construed as encompassing all the features of patentable novelty that reside in the present invention, including all features that would be treated as equivalents thereof by those skilled in the art to which this invention pertains.

What is claimed is:

1. An active matrix display device comprising: a pair of insulating substrates at least one of which is light transmitting; scanning lines arranged on one of said pair of substrates; scanning branch lines each branching from said scanning line; and switching elements each formed on an end portion of said scanning branch line,

wherein the distance between the scanning line side of said switching element and said scanning line is so provided as to enable said scanning branch line to be cut off by irradiation with light energy.

2. An active matrix display device according to claim 1, further comprising a pixel electrode connected to said switching element and a supplemental capacitor electrode disposed opposite to said pixel electrode with an insulating film interposed therebetween, a supplemental capacitor being formed between said pixel electrode and said supplemental capacitor electrode.

3. An active matrix display device according to claim 1, further comprising a pixel electrode connected to said switching element and disposed opposite to a scanning line adjacent to said scanning line with an insulating film interposed therebetween, a supplemental capacitor being formed at the superimposing portion of said pixel electrode and said adjacent scanning line.

4. An active matrix display device comprising: a pair of insulating substrates at least one of which is light

transmitting; scanning lines arranged on one of said pair of substrates; scanning branch lines each branching from said scanning line; and switching elements each formed on an end portion of said scanning branch line, wherein a portion of said scanning branch line other than the portion thereof where said switching element is formed is narrower than that of the portion thereof where said switching element is formed.

5. An active matrix display device according to claim 4, wherein said narrower width portion is formed by cutting one or the other side of a portion of said scanning branch line other than the portion thereof where said switching element is formed.

6. An active matrix display device according to claim 4, further comprising a pixel electrode connected to said switching element and a supplemental capacitor electrode disposed opposite to said pixel electrode with an insulating film interposed therebetween, a supplemental capacitor being formed between said pixel electrode and said supplemental capacitor electrode.

7. An active matrix display device according to claim 4, further comprising a pixel electrode connected to said switching element and disposed opposite to a scanning line adjacent to said scanning line with an insulating film interposed therebetween, a supplemental capacitor being formed at the superimposed portion of said pixel electrode and said adjacent scanning line.

8. A method of manufacturing an active matrix display device, comprising the steps of: forming an active

matrix substrate which comprises an insulating substrate, scanning lines and signal lines arranged in vertical and horizontal directions on said substrate, scanning branch lines each branching from said scanning line, switching elements each formed on an end portion of said scanning branch line, and pixel electrodes each connected to said switching element, the distance between the scanning line side of said switching element and said scanning line being so provided as to allow said scanning branch line to be cut off by irradiation with light energy;

attaching an opposing substrate to said active matrix substrate with a display medium sandwiched between said active matrix substrate and said opposing substrate;

detecting a pixel defect by applying a driving voltage to said pixel electrodes from said scanning lines and said signal lines via said switching elements; and

irradiating light energy onto the switching element connected to a defective pixel electrode causing said pixel defect to electrically connect said defective pixel electrode to said signal line, and irradiating light energy onto said scanning branch line to disconnect said scanning branch line from said scanning line.

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9. An active matrix display device comprising: a pair of insulating substrates at least one of which is light transmitting; scanning lines and signal lines arranged

in vertical and horizontal directions on one of said pair of substrates; and pixel electrodes each connected to said scanning line and said signal line via a switching element,

the active matrix display device further comprising: a conductive layer disposed under said signal line and said pixel electrode with an insulating film interposed therebetween; and a conductive piece formed between said pixel electrode and said insulating film.

10. An active matrix display device according to claim 9, wherein said conductive layer is electrically connected to a scanning line adjacent to said scanning line connected to said pixel electrode and an anodic oxide film is formed on said conductive layer.

11. An active matrix display device according to claim 9, further comprising a supplemental capacitor electrode disposed opposite to said pixel electrode with said insulating film interposed therebetween, wherein said conductive layer is electrically connected to said supplemental capacitor electrode and an anodic oxide film is formed on said conductive layer.

12. An active matrix display device comprising: a pair of insulating substrates at least one of which is light transmitting; scanning lines and signal lines arranged in vertical and horizontal directions on one of said pair of substrates; and pixel electrodes each connected to said scanning line and said signal line via a switching element,

the active matrix display device further comprising: a conductive layer disposed under said signal line and a pair of adjacent pixel electrodes with an insulating film interposed therebetween; and conductive pieces each formed between said insulating film and one of said pair of pixel electrodes.

13. An active matrix display device according to claim 12, wherein said conductive layer is electrically connected to a scanning line adjacent to said scanning line connected to said pixel electrode and an anodic oxide film is formed on said conductive layer.

14. An active matrix display device according to claim 12, further comprising a supplemental capacitor electrode disposed opposite to said pixel electrode with said insulating film interposed therebetween, wherein said conductive layer is electrically connected to said supplemental capacitor electrode and an anodic oxide film is formed on said conductive layer.

15. A method of manufacturing an active matrix display device, comprising the steps of:

forming an active matrix substrate which comprises an insulating substrate, scanning lines and signal lines arranged in vertical and horizontal directions on said substrate, pixel electrodes each connected to said scanning line and said signal line via a switching element, conductive layers each disposed under said signal line and said pixel electrode with an insulating film interposed therebetween, and conductive pieces each formed between said pixel electrode and

said insulating film;

attaching an opposing substrate to said active matrix substrate with a display medium sandwiched between said active matrix substrate and said opposing substrate;

detecting a pixel electrode by applying a driving voltage to said pixel electrodes from said scanning lines and said signal lines via said switching elements; and

irradiating light energy onto the superimposed portion of said conductive layer and said conductive piece connected to a defective pixel electrode causing said pixel defect to electrically connect said defective pixel electrode to said conductive layer, and irradiating light energy onto the superimposed portion of said signal line and said conductive layer to electrically connect said signal line to said conductive layer.

Nixon & Vanderhye P.C. (7/88)

RULE 63 (37 C.F.R. 1.63)
DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled AN ACTIVE MATRIX DISPLAY DEVICE AND A METHOD OF MANUFACTURING THE SAME, the specification of which (check applicable box(es)):

[x] is attached hereto.
[ ] was filed on _____ as U.S. Application Serial No. _____
[ ] was filed as PCT international application No. PCT/_____/_____ on _____
and (if applicable to U.S. or PCT application) was amended on _____.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with 37 C.F.R. 1.56(a). I hereby claim foreign priority benefits under 35 U.S.C. 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed or, if no priority is claimed, before the filing date of this application:

Prior Foreign Application(s):

Application Number	Country	Day/Month/Year Filed
Patent Appln No. 2-121787	Japan	11/May/1990
2-121788	Japan	11/May/1990
2-125191	Japan	14/May/1990
2-146857	Japan	04/June/1990

I hereby claim the benefit under 35 U.S.C. 120/365 of all prior United States and PCT international applications listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in such prior applications in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose material information as defined in 37 C.F.R. 1.56(a) which occurred between the filing date of the prior applications and the national or PCT international filing date of this application:

Prior U.S./PCT Application(s): Application Serial No.	Day/Month/Year Filed	Status: patented, pending, abandoned

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

And I hereby appoint Nixon & Vanderhye P.C., 2200 Clarendon Boulevard, 14th Floor, Arlington, Virginia 22201, telephone number (703) 875-0400 (to whom all communications are to be directed), and the following attorneys thereof (of the same address) individually and collectively my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and with the resulting patent: Arthur R. Crawford, 25327; Larry S. Nixon, 25640; Robert A. Vanderhye, 27076; James T. Hosmer, 30184; Robert W. Faris, 31352; Richard G. Besha, 22770; Mark E. Nusbaum, 32348; Michael J. Keenan, 32106; Bryan H. Davidson, 30251; Stanley C. Spooner, 27393; Leonard C. Mitchard, 29009.

1) Inventor's Signature Yuzuru Kanemori Date December 27, 1990
Inventor's Name (typed) Yuzuru (First) 4Q1QQ (Middle Initial) KANEMORI (Family Name) Japan (Citizenship)
Residence (City) Tenri-shi JPX (State/Foreign Country) Nara-ken Japan
Post Office Address 2613-1, Ichinomoto-cho, Tenri-shi, Nara-ken Japan Zip Code 632

2) Inventor's Signature Mikio Katayama Date December 27, 1990
Inventor's Name (typed) Mikio (First) 4Q2QQ (Middle Initial) KATAYAMA (Family Name) Japan (Citizenship)
Residence (City) Ikoma-shi JPX (State/Foreign Country) Nara-ken Japan
Post Office Address 1879-51-704, Tawaraguchi-cho, Ikoma-shi, Nara-ken Japan Zip Code 630-02

FOR ADDITIONAL INVENTORS, check box [ ] and attach sheet with same information and signature and date for each.

SHC 001269

3) Inventor's Signature Kiyoshi Nakazawa Date December 27, 1990

Inventor's Name (typed) First: Kiyoshi 4038 Middle Initial: Family Name: NAKAZAWA Citizenship: Japan

Residence (City): Fujiidera-shi JPX (State/Foreign Country): Osaka Japan

Post Office Address: 1-12-18, Emisaka, Fujiidera-shi, Osaka Japan Zip Code: 583

4) Inventor's Signature Hiroaki Kato Date December 27, 1990

Inventor's Name (typed) First: Hiroaki 4041 Middle Initial: Family Name: KATO Citizenship: Japan

Residence (City): Nara-shi JPX (State/Foreign Country): Nara-ken Japan

Post Office Address: 1-9-4, Tezukayama, Nara-shi, Nara-ken Japan Zip Code: 631

5) Inventor's Signature Kozo Yano Date December 27, 1990

Inventor's Name (typed) First: Kozo 4059 Middle Initial: Family Name: YANO Citizenship: Japan

Residence (City): Yamatokoriyama-shi JPX (State/Foreign Country): Nara-ken Japan

Post Office Address: 34-5, Izumihara-cho, Yamatokoriyama-shi, Nara-ken Japan Zip Code: 639-11

6) Inventor's Signature Naofumi Kondo Date December 27, 1990

Inventor's Name (typed) First: Naofumi 4066 Middle Initial: Family Name: KONDO Citizenship: Japan

Residence (City): Nara-shi JPX (State/Foreign Country): Nara-ken Japan

Post Office Address: 4-6-21, Wakaba-dai, Nara-shi, Nara-ken Japan Zip Code: 631

7) Inventor's Signature Hiroshi Fujiki Date December 27, 1990

Inventor's Name (typed) First: Hiroshi 4074 Middle Initial: Family Name: FUJIKI Citizenship: Japan

Residence (City): Sakai-shi JPX (State/Foreign Country): Osaka Japan

Post Office Address: 2366, Kanaoka-cho, Sakai-shi, Osaka Japan Zip Code: 591

8) Inventor's Signature Toshiaki Fujihara Date December 27, 1990

Inventor's Name (typed) First: Toshiaki 4082 Middle Initial: Family Name: FUJIHARA Citizenship: Japan

Residence (City): Higashiosaka-shi JPX (State/Foreign Country): Osaka Japan

Post Office Address: 1-8-29, Uryudou, Higashiosaka-shi, Osaka Japan Zip Code: 578

9) Inventor's Signature Hidenori Negoto Date December 27, 1990

Inventor's Name (typed) First: Hidenori 4090 Middle Initial: Family Name: NEGOTO Citizenship: Japan

Residence (City): Ikoma-shi JPX (State/Foreign Country): Nara-ken Japan

Post Office Address: 950-1, Tawaraguchi-cho, Ikoma-shi, Nara-ken Japan Zip Code: 630-02

10) Inventor's Signature Manabu Takahama Date December 27, 1990

Inventor's Name (typed) First: Manabu 4108 Middle Initial: Family Name: TAKAHAMA Citizenship: Japan

Residence (City): Tenri-shi JPX (State/Foreign Country): Nara-ken Japan

Post Office Address: 2613-1, Ichinomoto-cho, Tenri-shi, Nara-ken Japan Zip Code: 632

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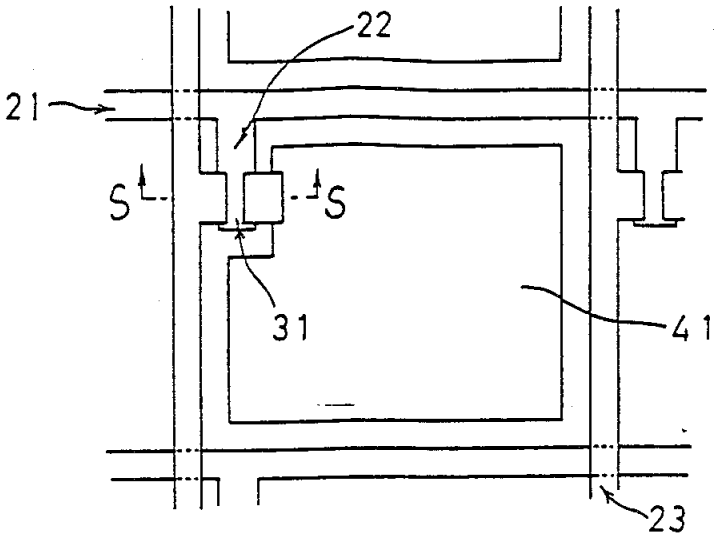
Fig. 1 GI 656845 18/14



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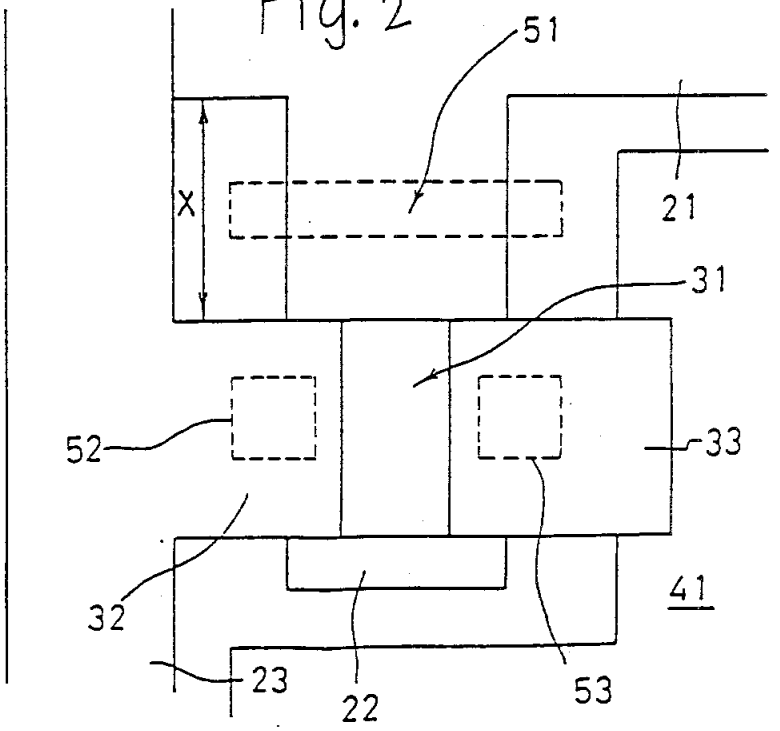

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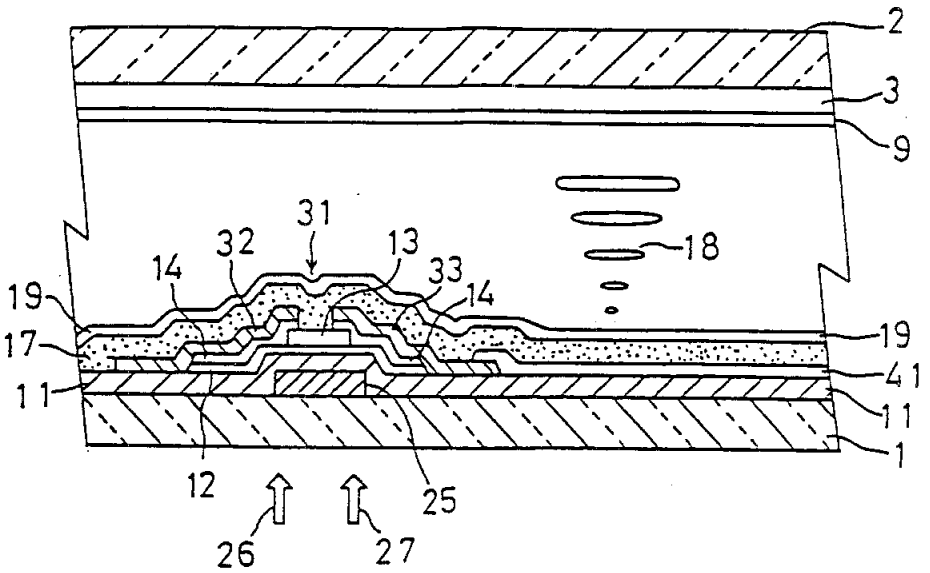

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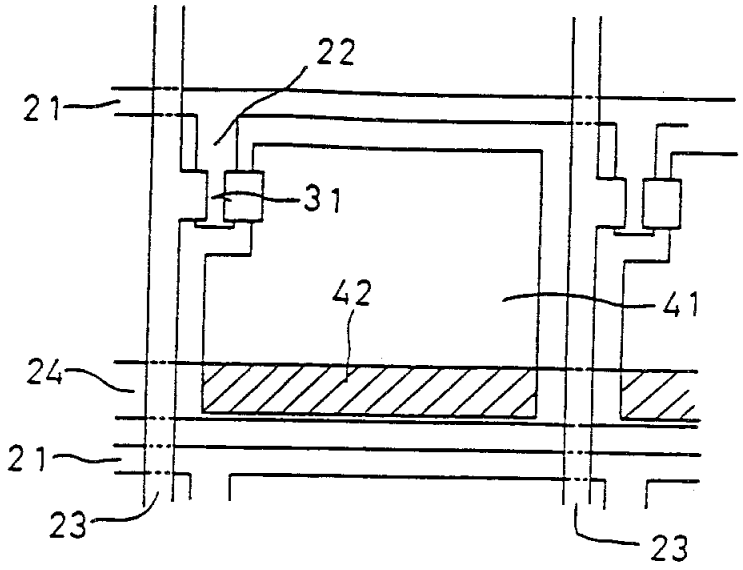

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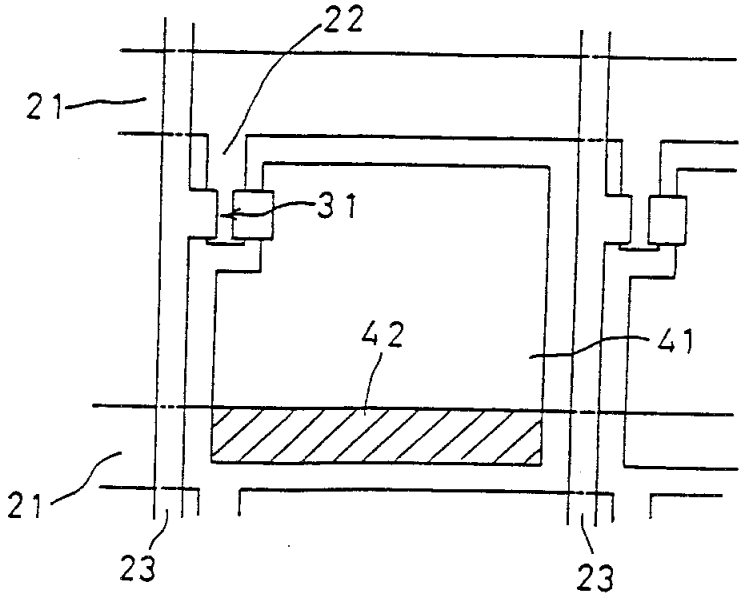

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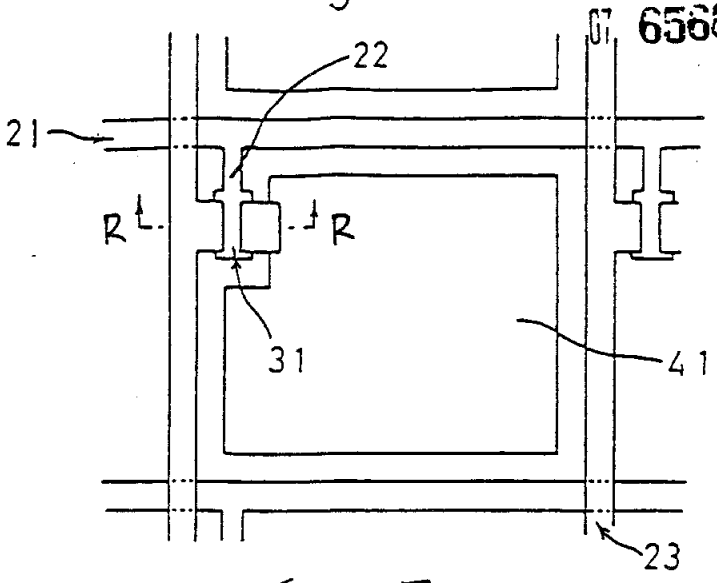

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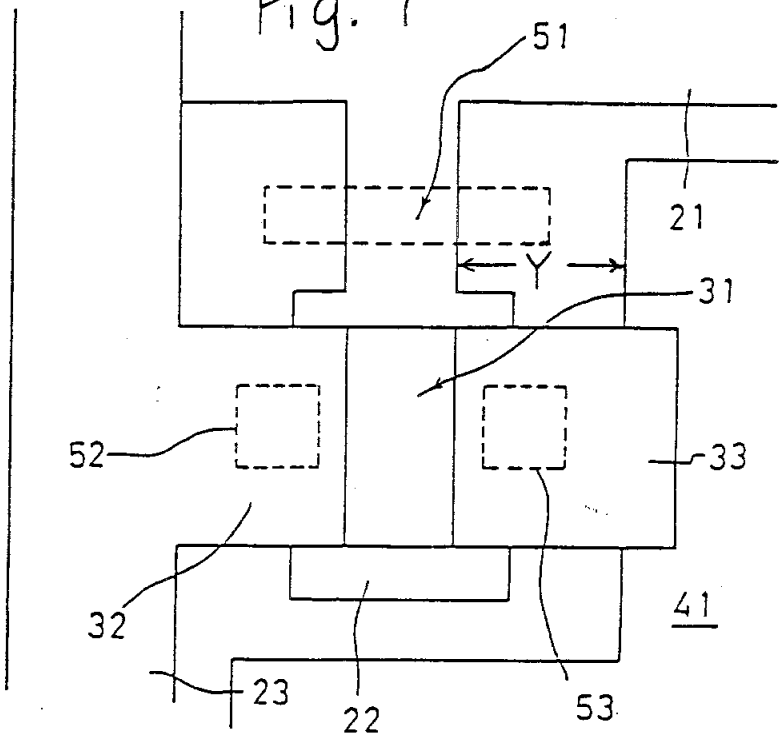

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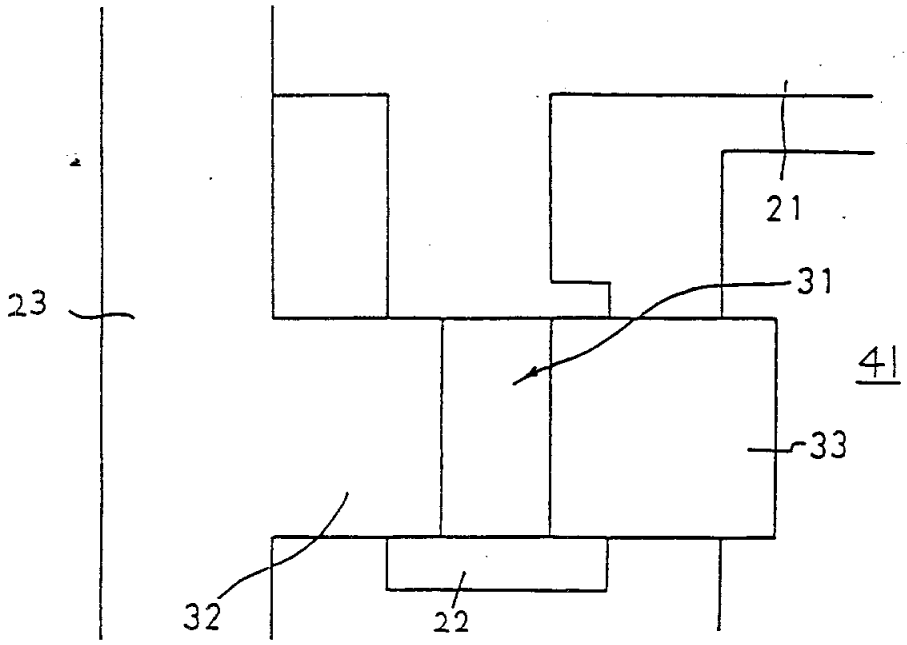

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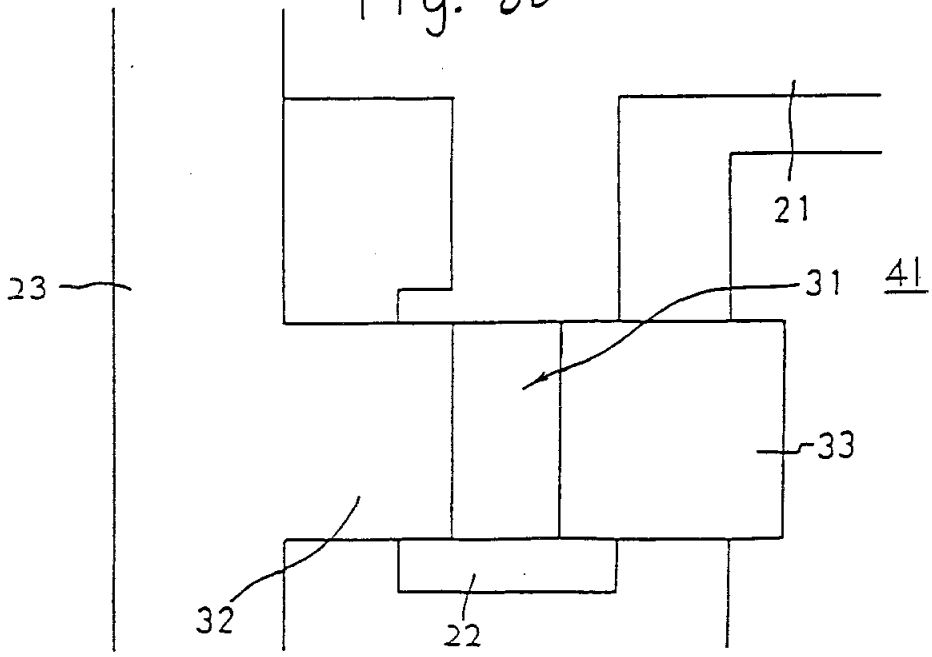

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Fig. 9

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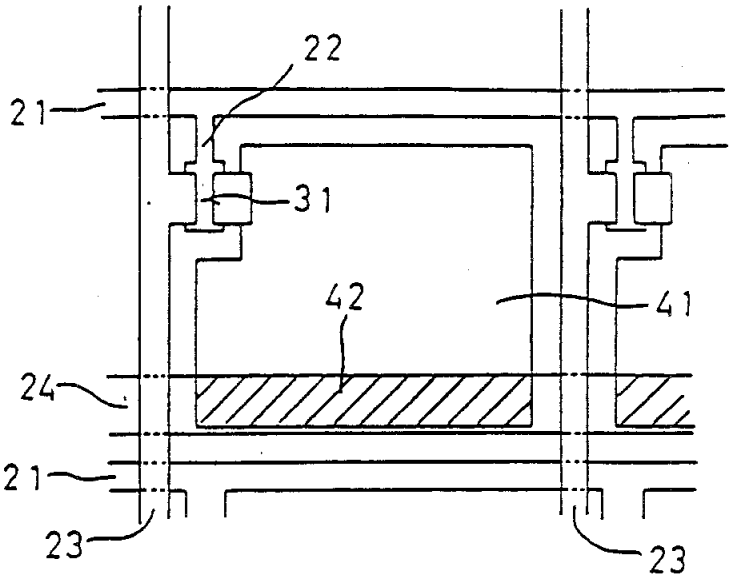

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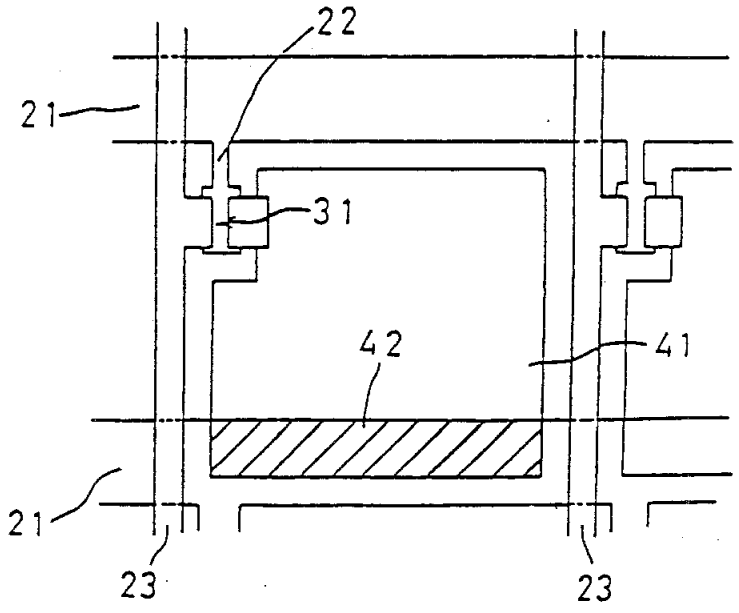

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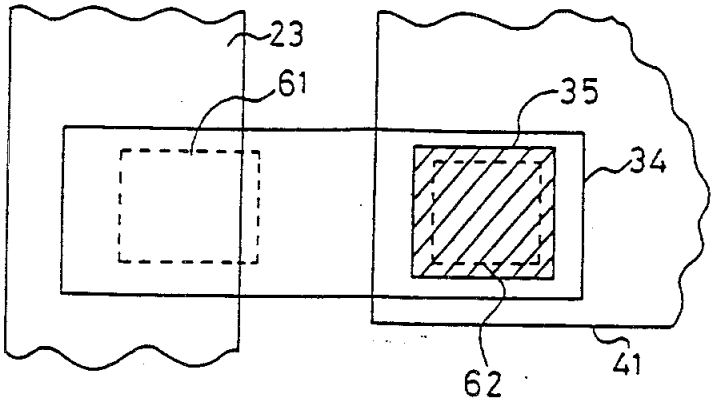

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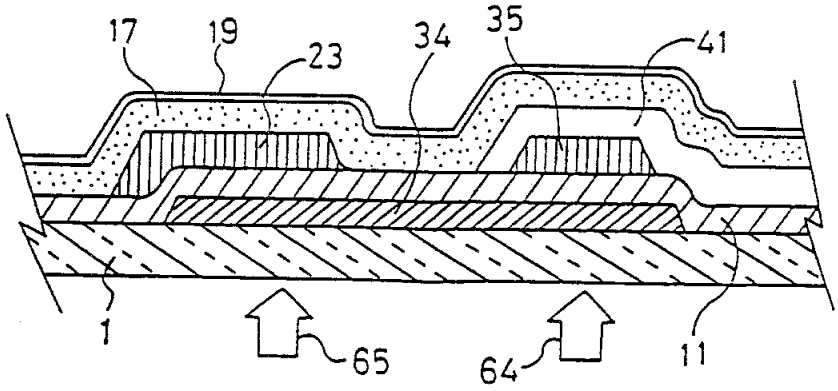

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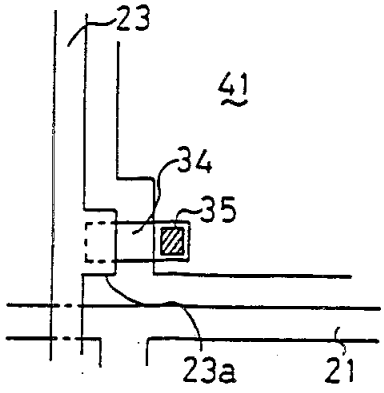

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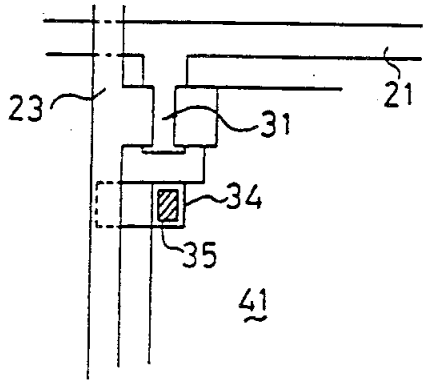

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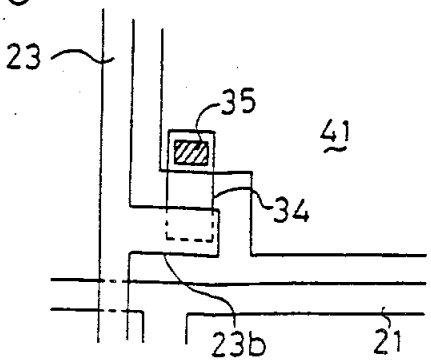

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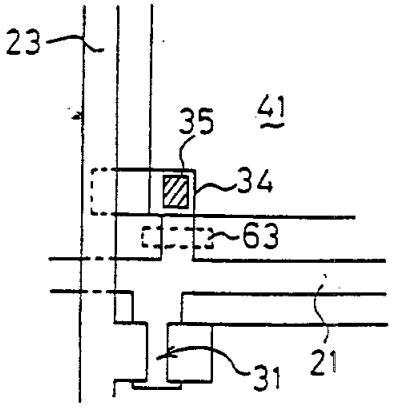

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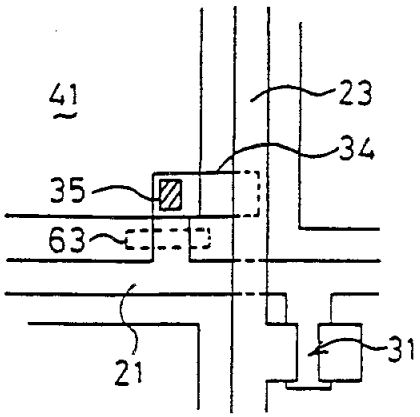

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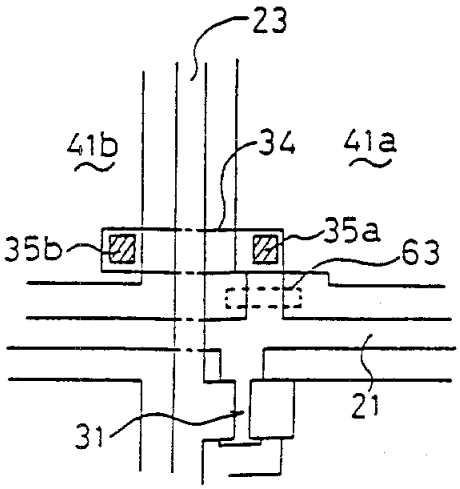

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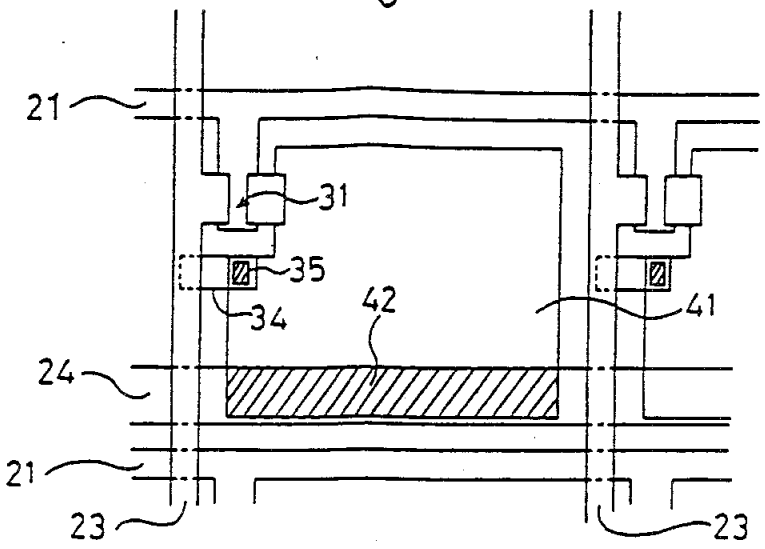

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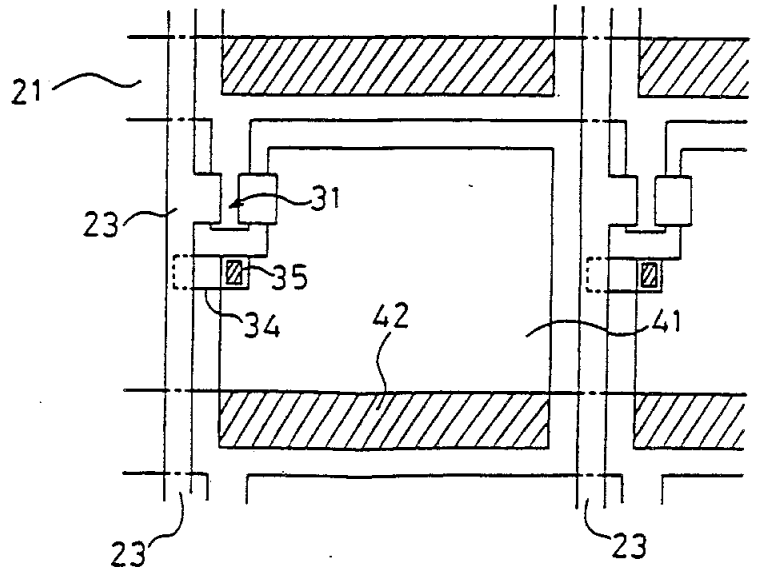

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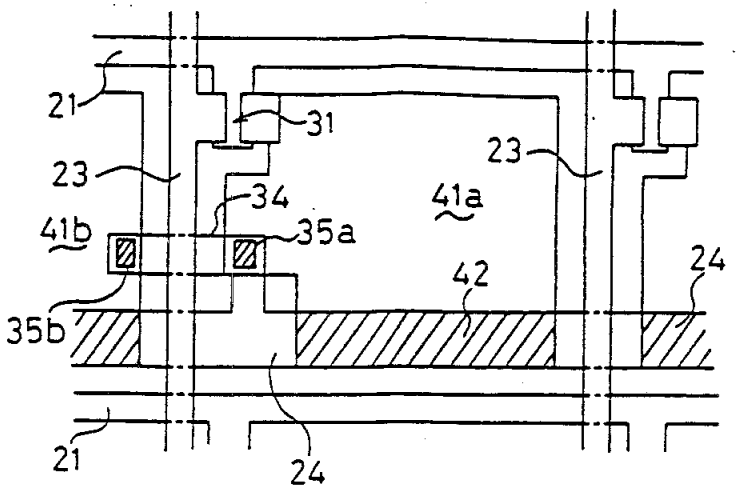
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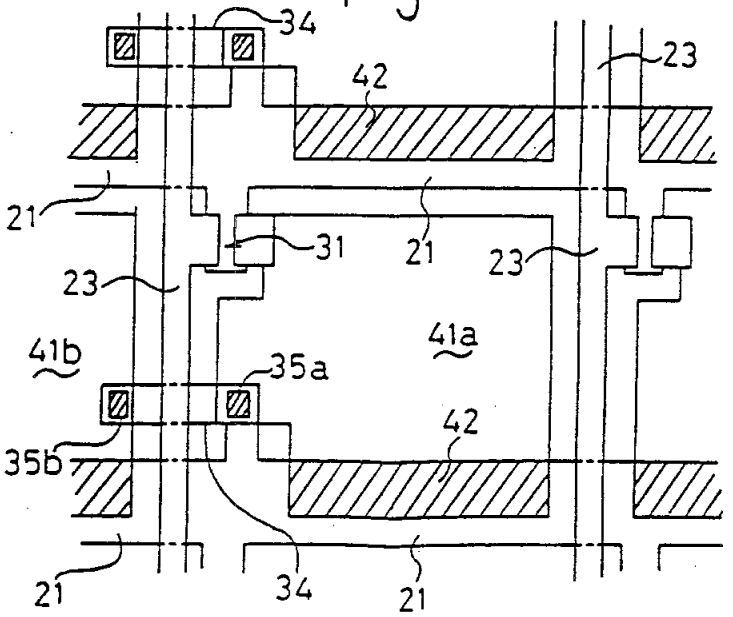
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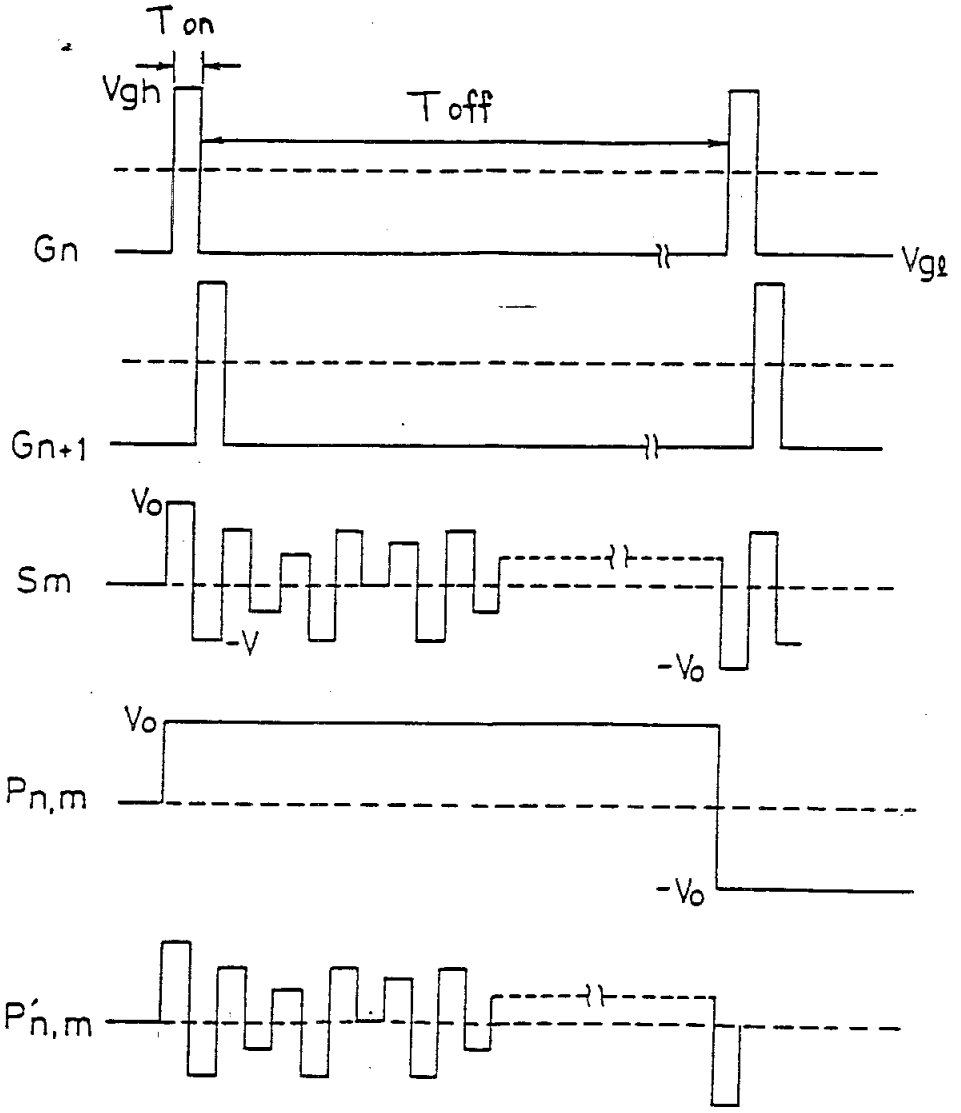
Fig. 20



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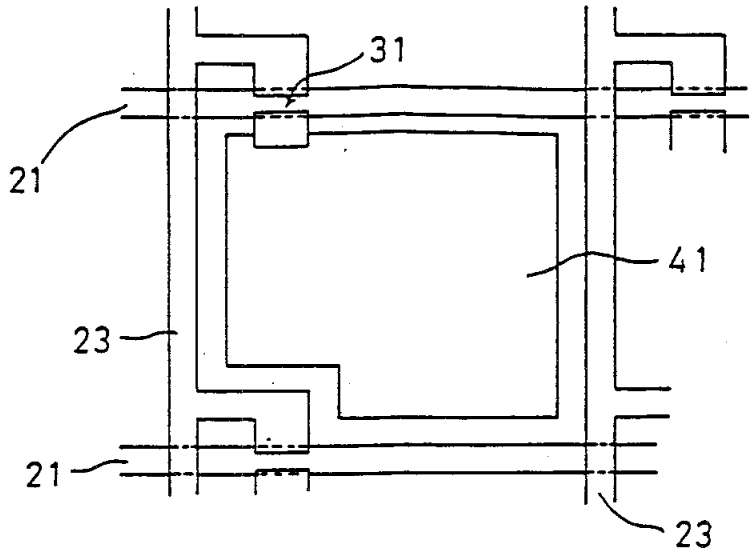

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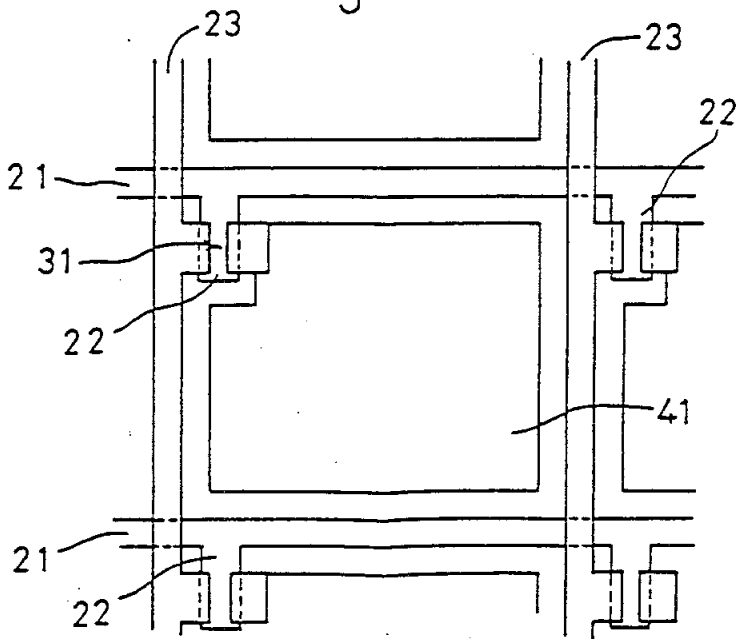

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Fig. 1 Of 656845

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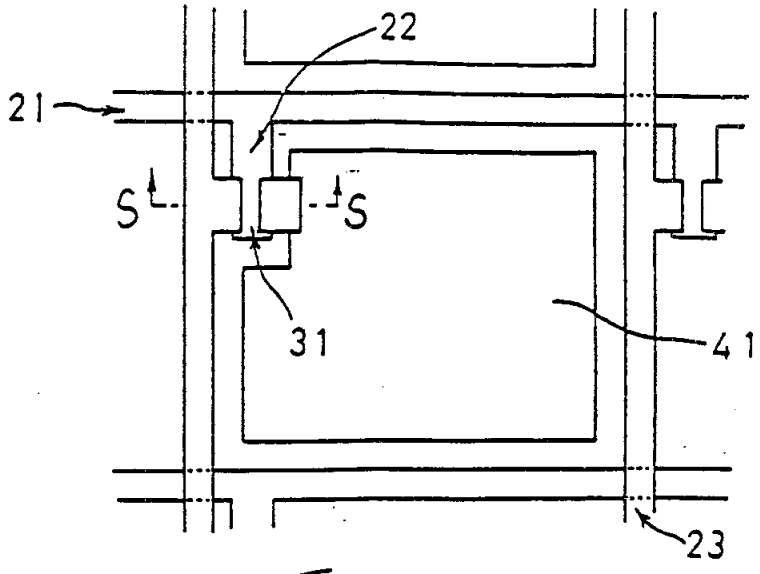

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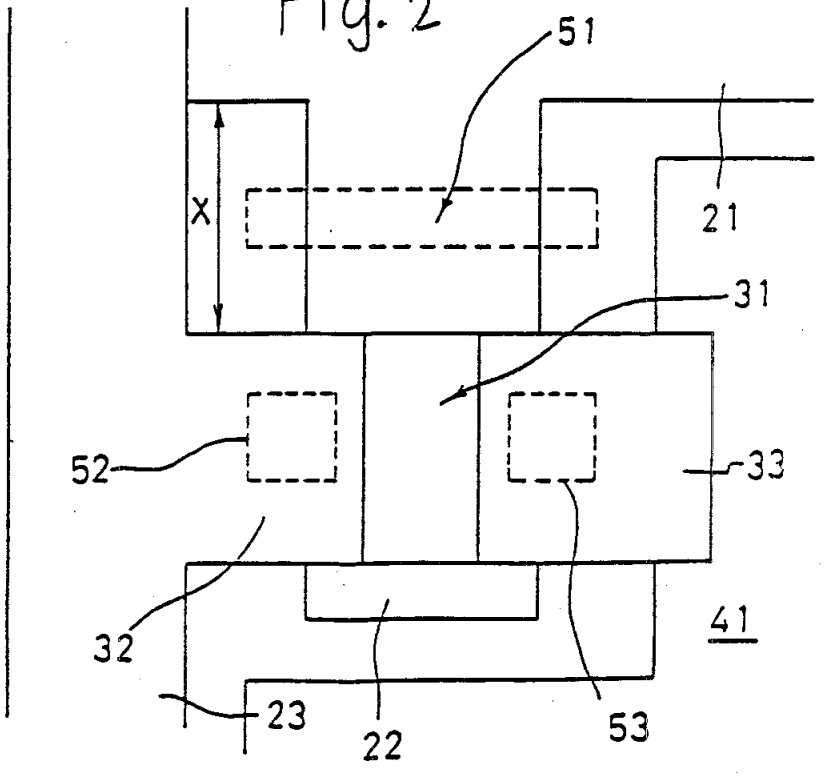

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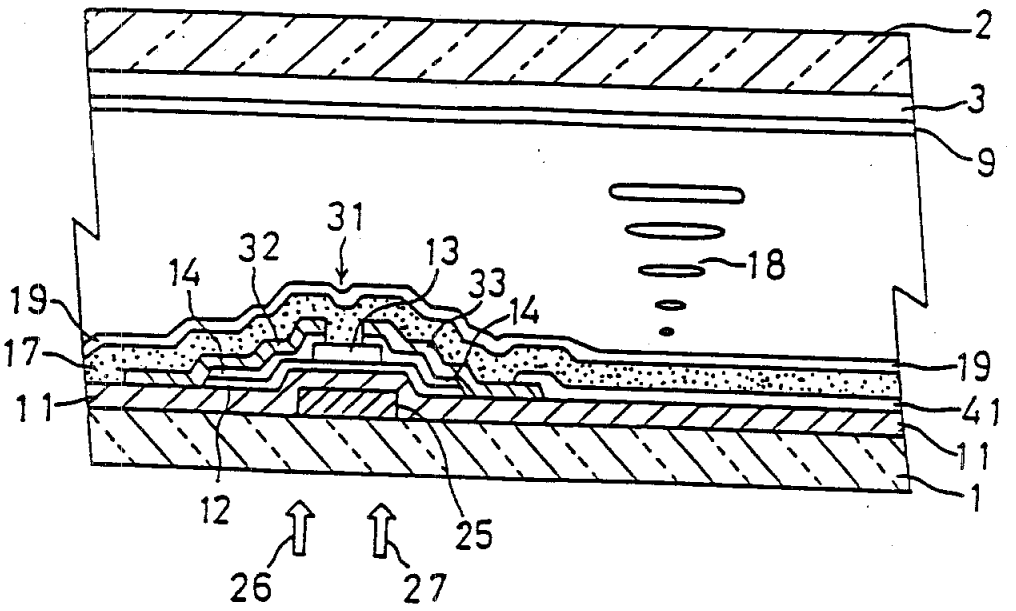

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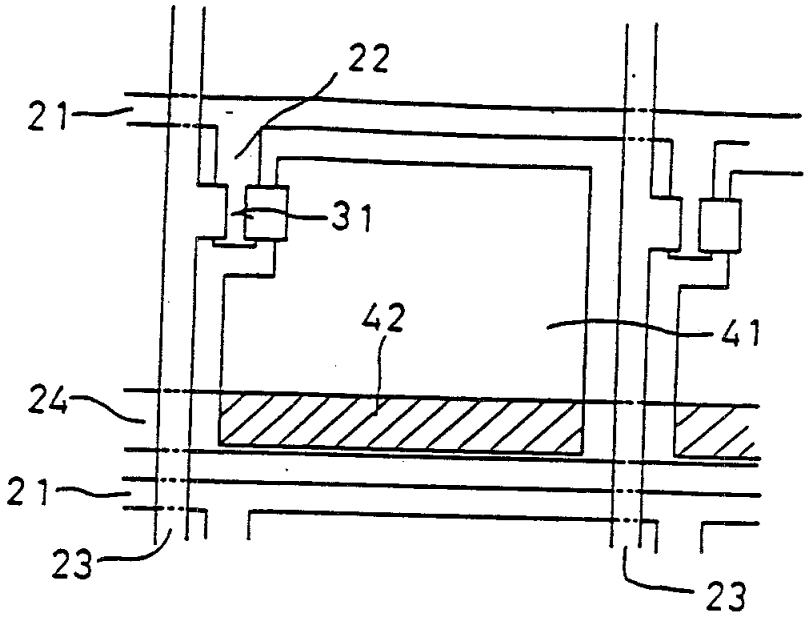

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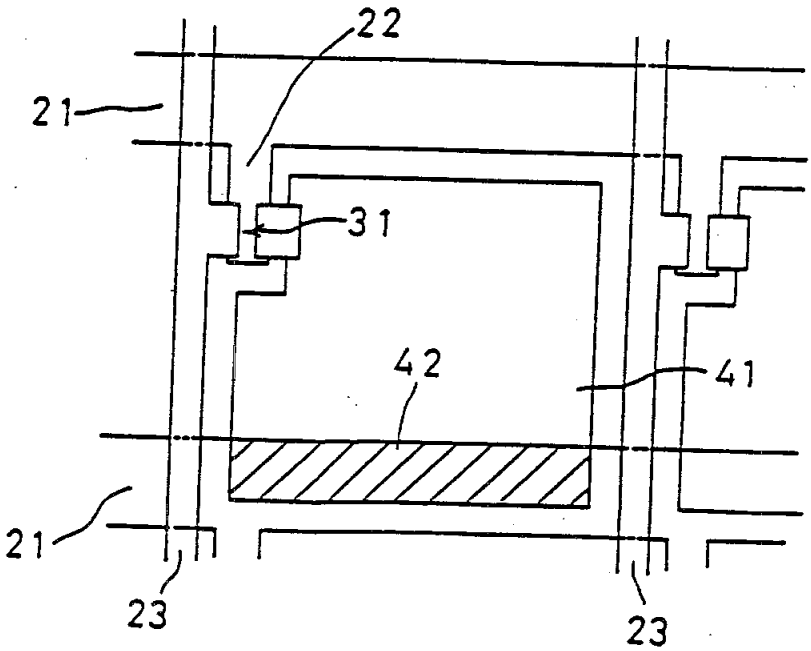

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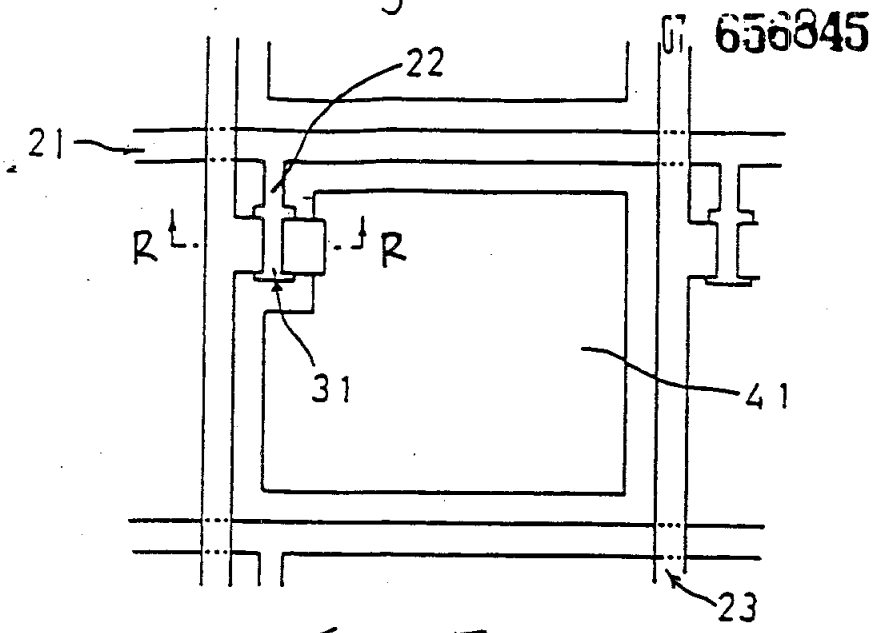

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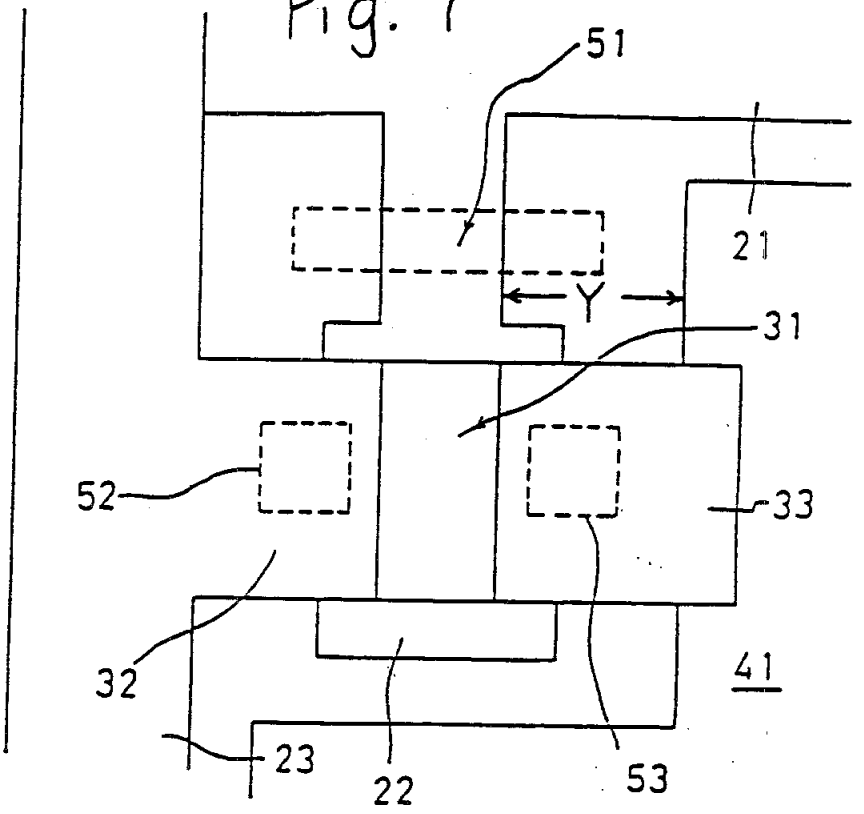

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Fig. 8A

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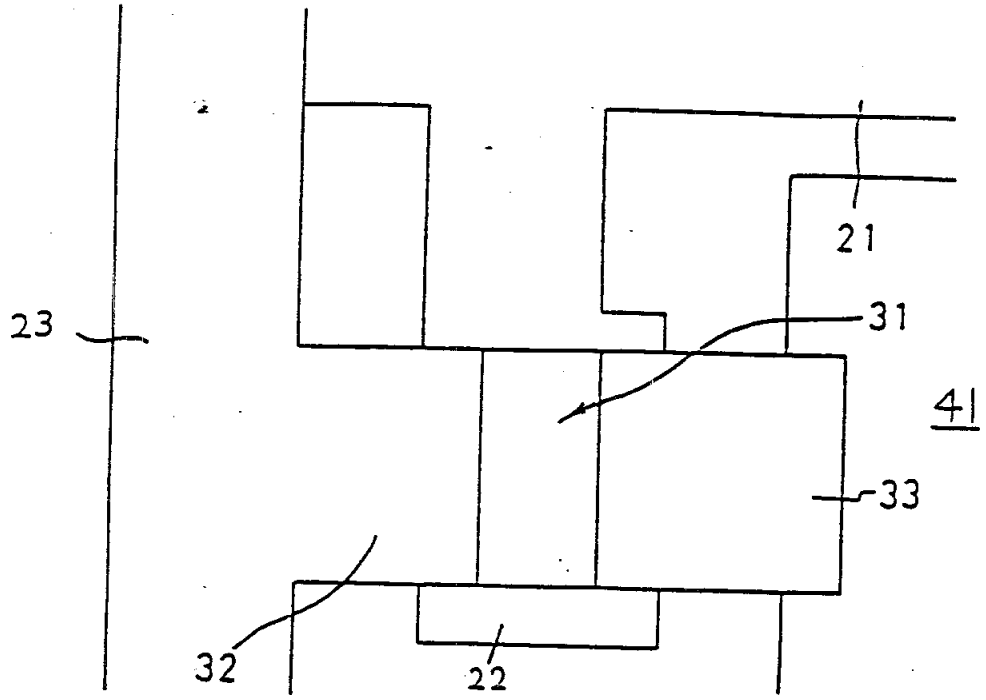

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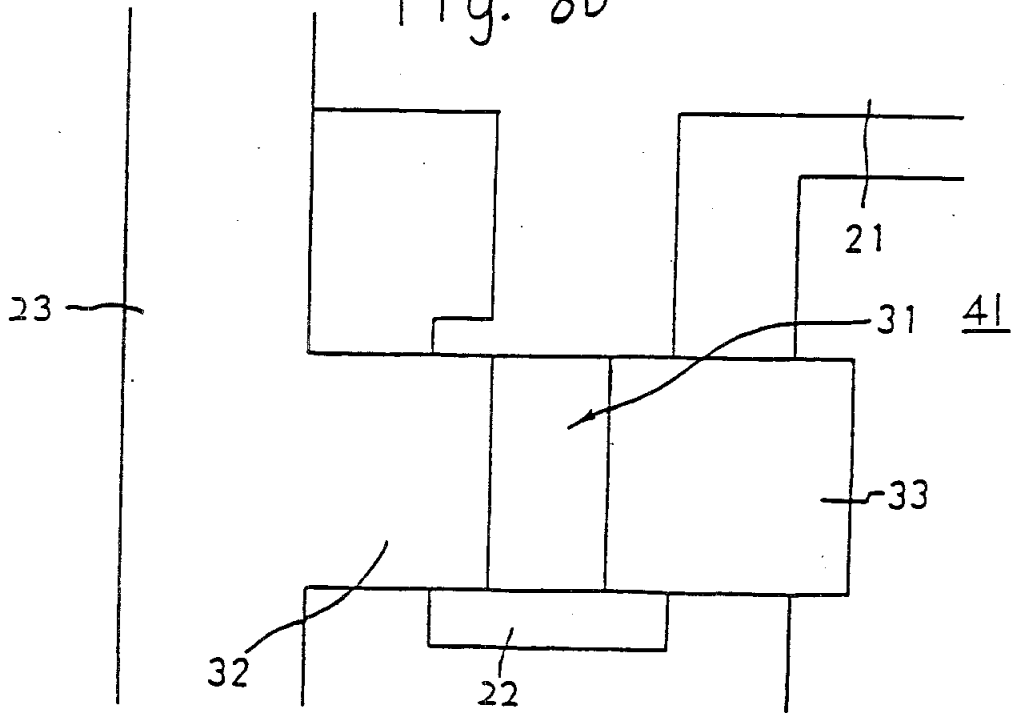

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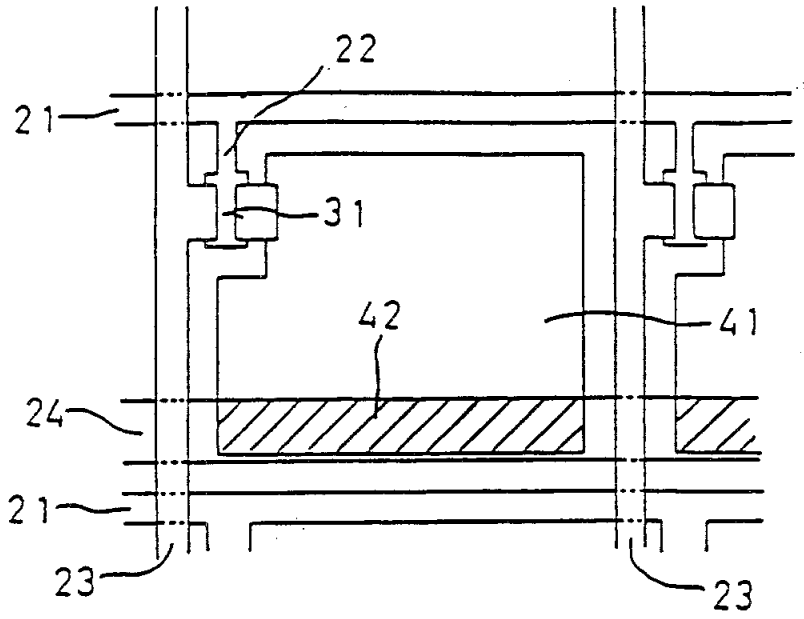

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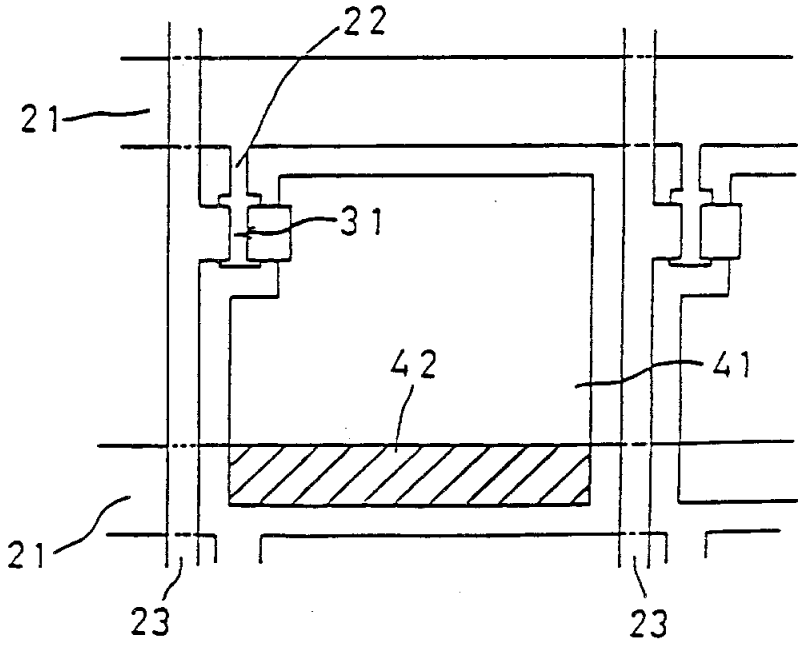

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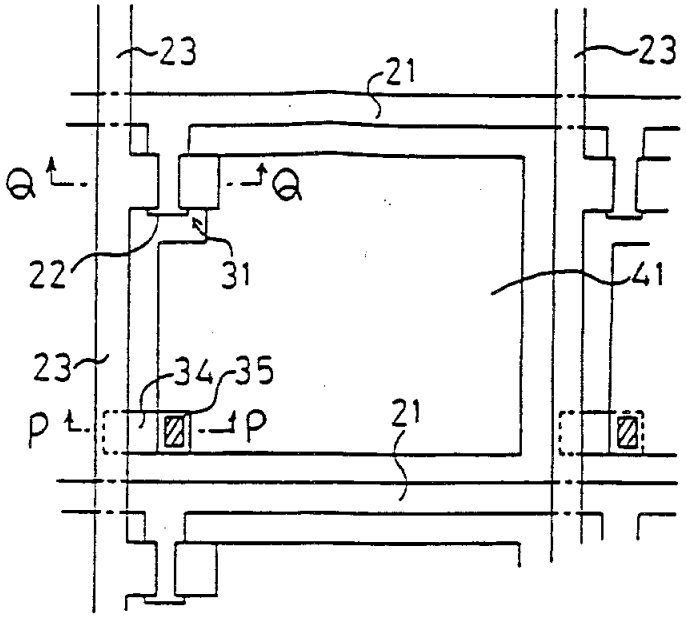

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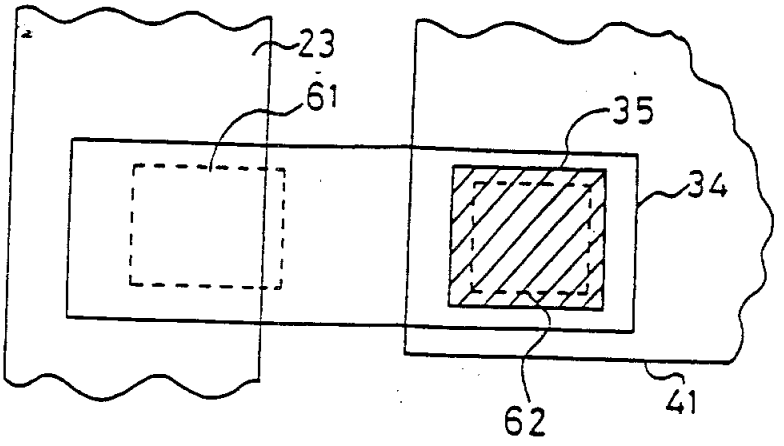

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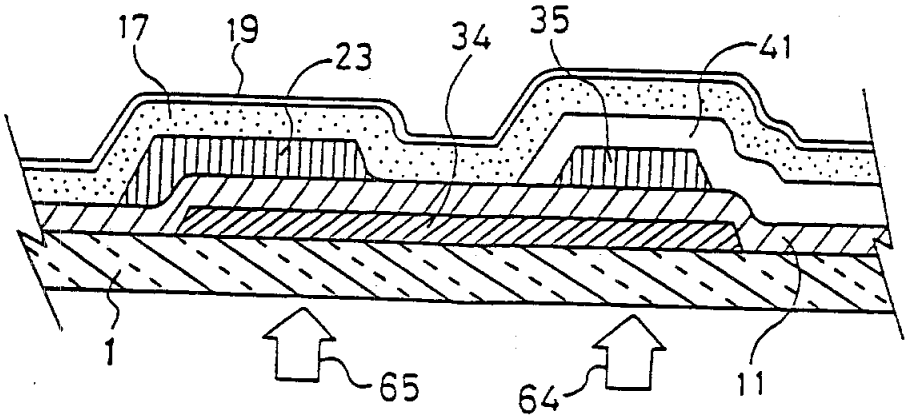

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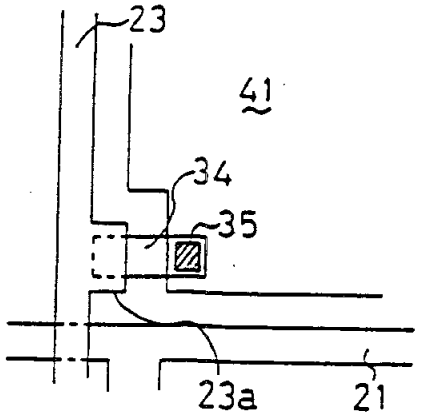

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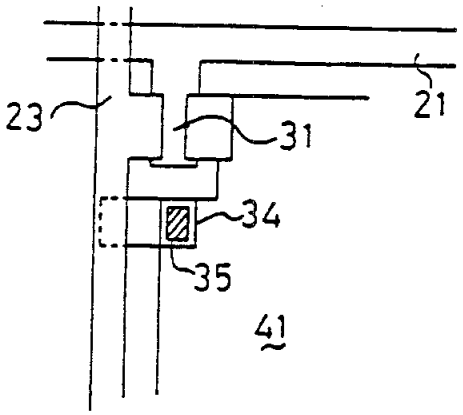

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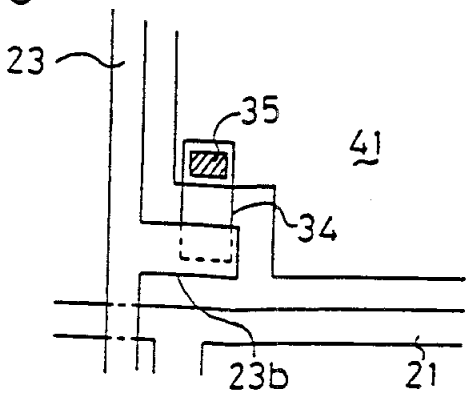

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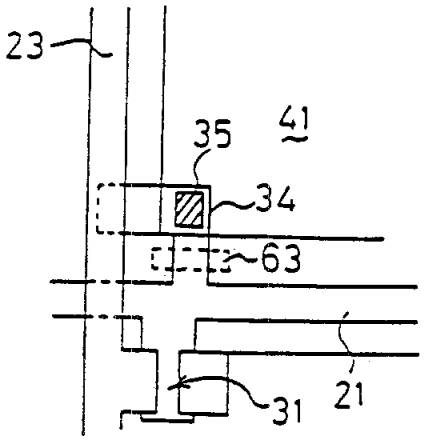

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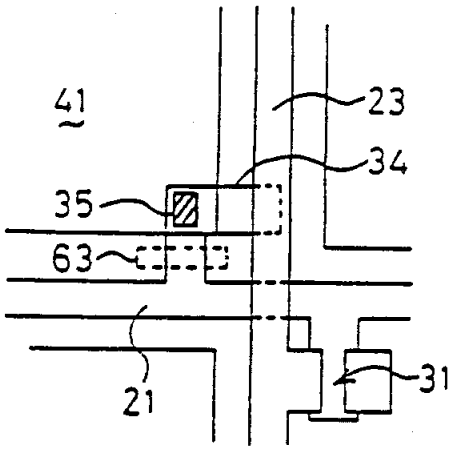

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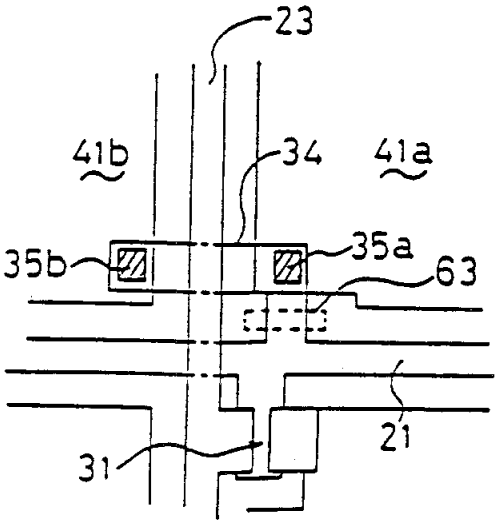

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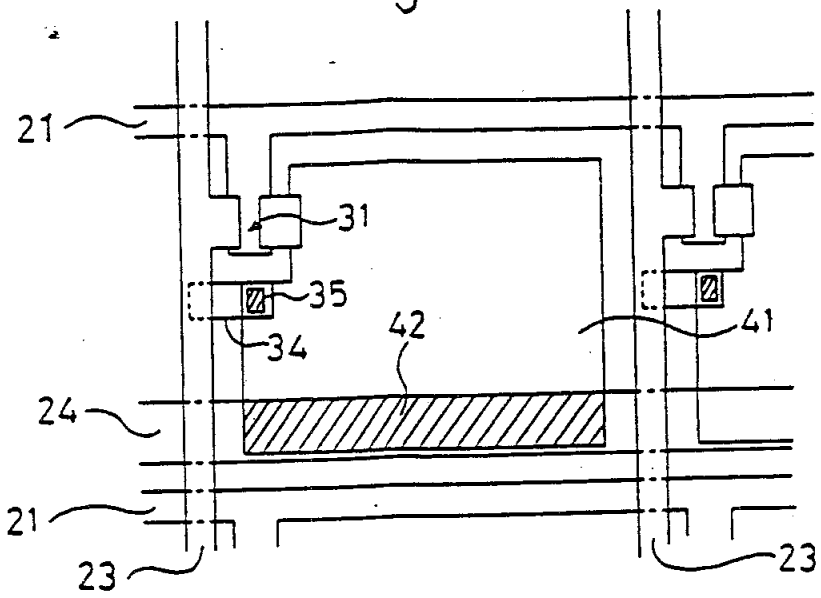

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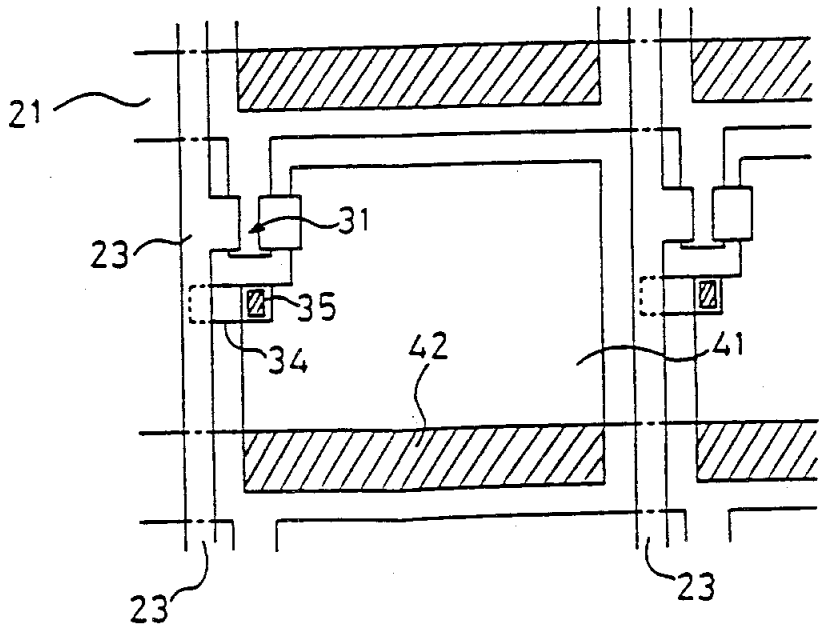

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GT 656845

Fig. 18

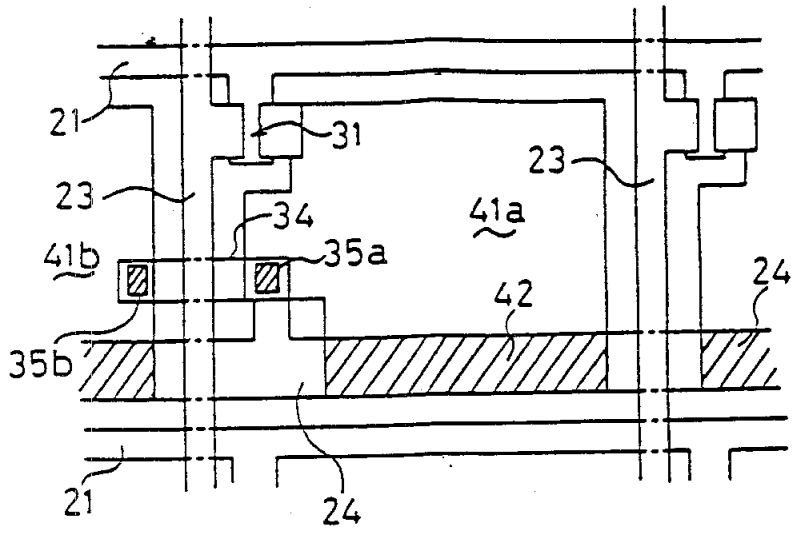
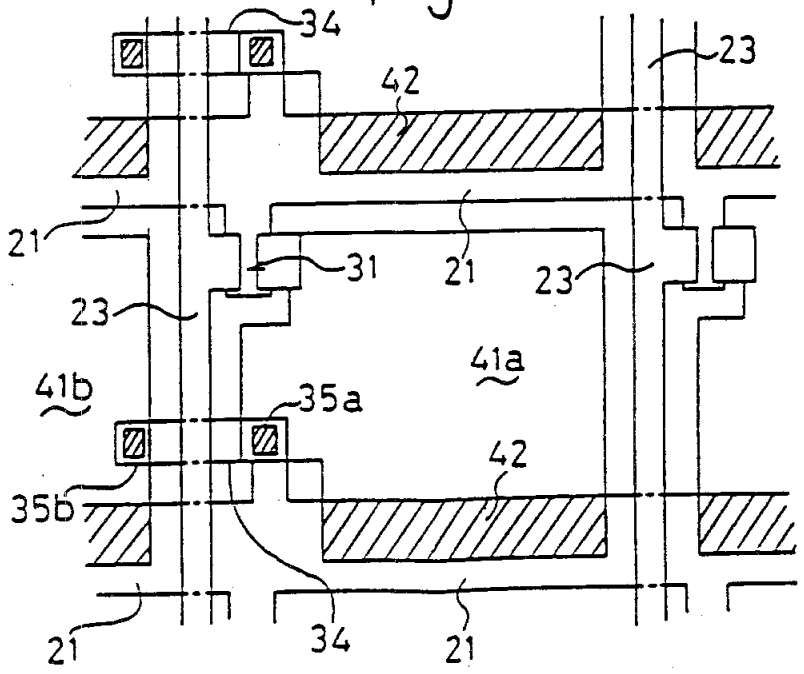


Fig. 19



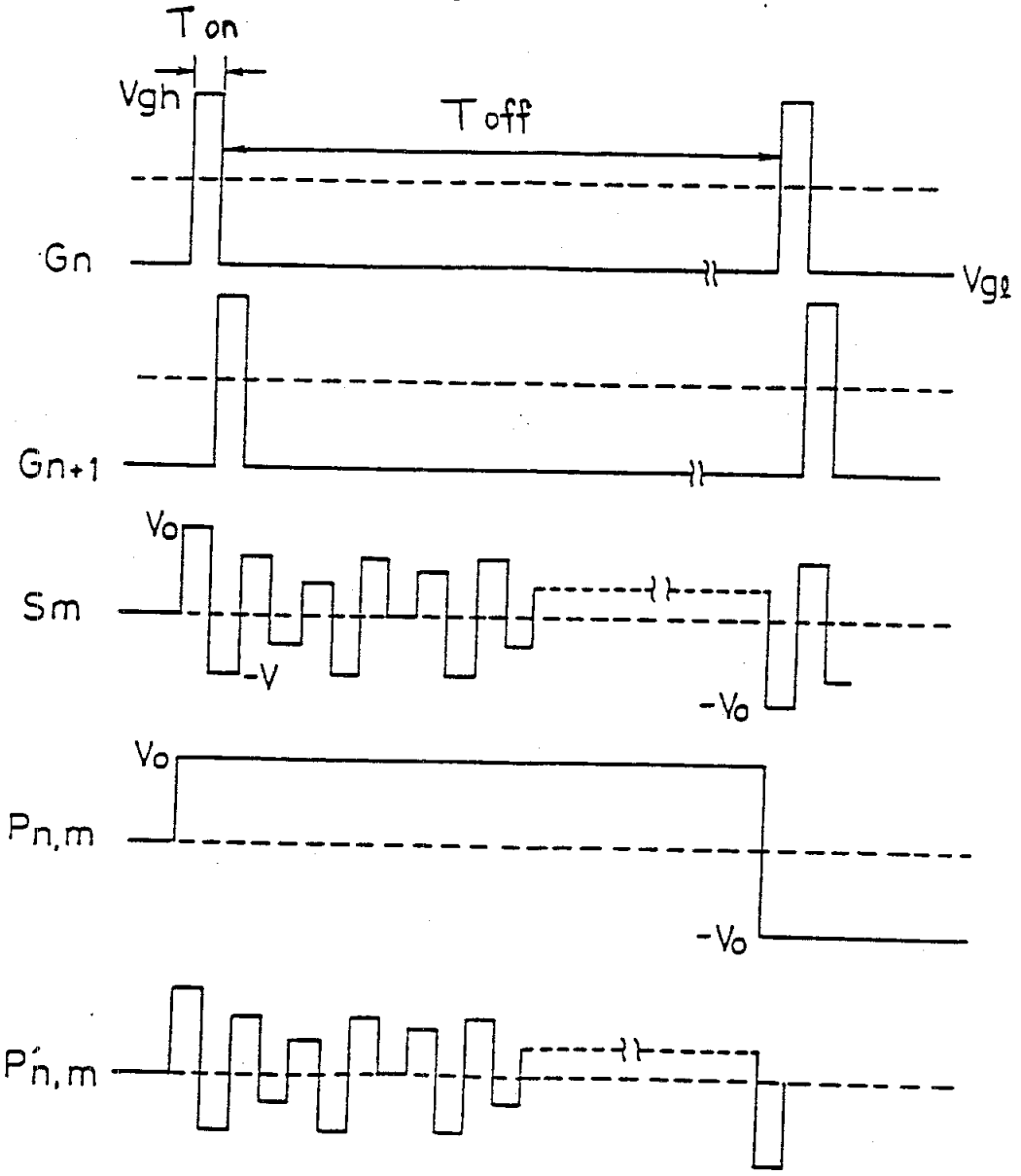
SHC 001296

Print Of Drawings
As Originally Filed

S90378

GI 656845

Fig. 20



Print Of Drawings
As Originally Filed

S90378

Fig. 21 Prior art

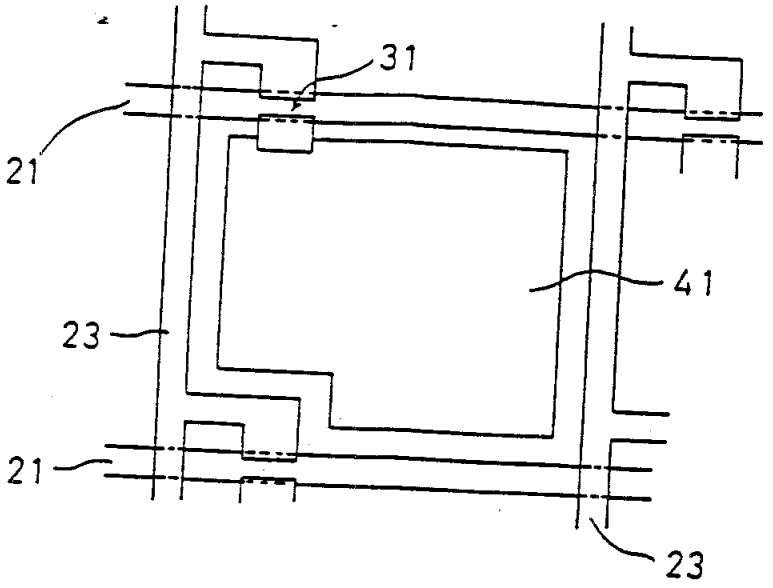
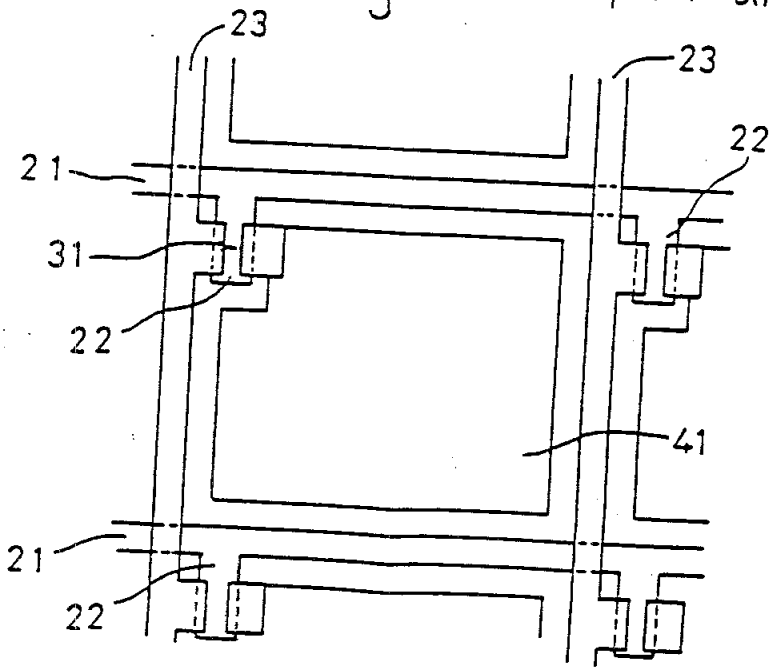


Fig. 22 Prior art



THE UNITED STATES PATENT AND TRADEMARK OFFICE 656845 #2

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231

Atty. Dkt. 829-61
C# M#

Sir:

Date: February 19, 1991

Attached for filing is the patent application of:

Inventor: **KANEMORI et al**

Entitled: **AN ACTIVE MATRIX DISPLAY DEVICE AND A METHOD OF MANUFACTURING THE SAME**

and including attachments as noted below:

[X] Declaration, X] Abstract,
[43] pages of specification and claims (including 15 numbered claims), and
[14] sheets of accompanying **Informal** drawing/s
[X] Record & return the attached assignment to the undersigned.
[X] Priority is hereby claimed under 35 USC 119 based on filing in **Jdapan**, of application(s) No(s). **2-121787, 2-121788, 2-125191 and 2-146857** filed on **May 11, 1990, May 11, 1990, May 14, 1990 and June 4, 1990,** respectively.
Certified copy(ies) [ ]attached or [ ]already filed on , respectively, in U.S. application Serial No. , filed .
[ ] Verified statement establishing "small entity" status under Rules 9 & 27.

[ ] **Preliminary amendment to claims (attached hereto), to be entered before calculation of the fee below.**

[ ] Also attached:

FILING FEE IS BASED ON CLAIMS AS FILED LESS ANY HEREWITH CANCELLED

Basic filing fee	$	630.00
Total effective claims 15 - 20 = 0 x $20	$	0.00
Independent claims 6 - 3 = 3 x $60	$	180.00
If any proper multiple dependent claims, add $200 *.....	$	
* (Ignore if improper claims)		
SUBTOTAL	$	810.00
If "small entity", then enter half (1/2) of subtotal and subtract.-$	$	()
TOTAL FILING FEE ENCLOSED	$	810.00
[X] Assignment recording fee ($8.00).....	$	818.00
TOTAL FEE ENCLOSED	$	818.00

The Commissioner is hereby authorized to charge any deficiency in the fee(s) filed, or asserted to be filed, or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Account No. 14-1140. A duplicate copy of this sheet is attached.

2200 Clarendon Blvd.
14th Floor
Arlington, VA 22201
Tel: (703) 875-0400

NIXON & VANDERHYE P.C.
By Atty: Larry S. Nixon, Reg. No. 25,640
Fee

Signature: Larry S. Nixon #33,626

LSN/bjc

SHC 001299

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
07/656,845	02/19/91	KANEMORI	929-61

TRICE, R EXAMINER

NIXON AND VANDERHYE
2200 CLARENDON BLVD. 14TH FLOOR
ARLINGTON, VA 22201

ART UNIT	PAPER NUMBER
254	3

DATE MAILED: 08/15/91

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☒ This application has been examined ☐ Responsive to communication filed on _____ ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), — days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☒ Notice of References Cited by Examiner, PTO-892.
2. ☒ Notice re Patent Drawing, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, Form PTO-152
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☒ Claims 1-15 are pending in the application.
   Of the above, claims _____ are withdrawn from consideration.
2. ☐ Claims _____ have been cancelled.
3. ☐ Claims _____ are allowed.
4. ☒ Claims 1-15 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ Claims _____ are subject to restriction or election requirement.
7. ☒ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice re Patent Drawing, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____, has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed _____, has been ☐ approved; ☐ disapproved (see explanation).
12. ☒ Acknowledgement is made of the claim for priority under U.S.C. 119. The certified copy has ☐ been received ☒ not been received ☐ been filed in parent application, serial no. _____; filed on _____.
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

EXAMINER'S ACTION

PTOL-326 (Rev 9-88)

SHC 001300

Claim 8 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The pixel defect is not detected by the driving of the pixel electrode but rather by the driving of the pixel electrode and the observation of the effects of the driving.

Claims 10-11, 13-14 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The use of "electrically connected" is confusing. It is not clear whether the structure is a conductive connection or a capacitive connection. The confusion is further compounded by the use of "connected" when referring to the bus line and the pixel electrode being connected. In fact, the scanning line is connected to the TFT which has its drain electrode connected to the pixel electrode.

Claim 12 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As written, the claim appears to indicated two adjacent pixel electrodes with an insulation material between said pixels.

However, the structure is a conductive layer with an insulation layer on top of the conductive layer then the pixels on top of the insulation layer.

Claim 15 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Lines 27-28 indicate "signal lines" and "pixel electrodes" while line 31 refers to "said signal line" and "said pixel electrode". The "said" references should be in the plural sense.

The third indentation indicates detecting a pixel. This should indicate detecting whether a pixel is properly functioning.

Claim 5 is rejected under 35 U.S.C. § 112, fourth paragraph, as being of improper dependent form for failing to further limit the subject matter of a previous claim.

In a device claim, a method of fabrication fails to further limit the scope of the claim. Therefore, the formation of the narrower portion by cutting does not further limit the narrower portion.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (b) the invention was patented or described in a printed

publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-2 and 4-6 are rejected under 35 U.S.C. § 102(b) as being clearly anticipated by Yamashita et al.(4890097).

Lines 40-41 of column 1, column 5 and figure 2.

Claim 1 is rejected under 35 U.S.C. § 102(e) as being clearly anticipated by Yamashita et al.(4936656).

In column 7, the disconnection of electrodes, including the gate electrode, to a defective switching element is taught.

The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 C.F.R. § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 U.S.C. § 102(f) or (g) prior art under 35 U.S.C. § 103.

Claims 1-7 are rejected under 35 U.S.C. § 103 as being unpatentable over Yamashita et al.(4890097) and Okubo et al.(4761058).

Yamashita et al. teaches a device similar to applicants' invention. The only difference is the capacitor parallel to the LC is not specifically stated as being connected to the adjacent scanning bus.

Okubo et al. teaches the use of parallel capacitors to increase the number of pixel elements. Okubo et al. teaches three basic parallel capacitor structures: to the same scanning bus as the TFT, to the scanning bus adjacent the TFT and to a non-scanning bus.

It would have been obvious to one of ordinary skill in the liquid crystal art to have realized the unspecified parallel capacitor of Yamashita et al. as a capacitor connected to the adjacent scanning bus because this realization is one of three conventional configurations which allow for an increased number of pixels as per Okubo et al..

Claim 1 is rejected under 35 U.S.C. § 103 as being

unpatentable over Kawate and Yamashita et al.(4936656).

Kawate teaches the use of multiple transistors to provide redundancy. (This suggests the need to remove defect elements.)

Yamashita et al. teaches in column 7, that to disconnect a pixel from the rest of the display, it is necessary to cut at least two of the switching elements electrodes.

It is extremely well known in the liquid crystal art to remove defective elements by laser cutting as demonstrated by Yamashita et al.. Therefore, it would have been obvious to one of ordinary skill in the liquid crystal art to have provided the scanning line of Kawate far enough from the switching element to allow for laser cutting of the gate electrode. Furthermore, figure 3 of Kawate shows the scanning line to be separate from the switching element which could be understood to be far enough to enable the gate electrode to be severed by a laser.

Claims 2 and 3 are rejected under 35 U.S.C. § 103 as being unpatentable over Kawate and Yamashita et al.('656) as applied to claim 1 above, and further in view of Okubo et al.(4761058).

Okubo et al. teaches the use of supplemental capacitors (capacitors in parallel to the LC) to allow for an increased number of elements. This teaching is extremely old and well known. See columns 2 and 3.

It would have been obvious to one of ordinary skill to provide supplemental capacitors, as taught by Okubo et al., to

the device of Kawate and Yamashita et al. to increase to number of pixels in the liquid crystal display.

Claims 4-5 are rejected under 35 U.S.C. § 103 as being unpatentable over Kawate and Yamashita et al.('656) in view of either of Japanese Patents no. 2-254422 and 2-254423.

2-254422 and 2-254423 both teach the use of a narrow electrode which may be easily cut by a laser to remove a defective pixel from a display.

Kawate teaches the use of multiple transistors to provide redundancy. (This suggests the need to remove defect elements.)

Yamashita et al. teaches in column 7, that to disconnect a pixel from the rest of the display, it is necessary to cut at least two of the switching elements electrodes.

First, it would have been obvious to one of ordinary skill in the liquid crystal art to remove defective elements in the device of Kawate by laser cutting as taught by Yamashita et al.. Second, it would have been obvious to one of ordinary skill in the liquid crystal art to have provided the scanning line of Kawate far enough from the switching element to allow for laser cutting of only the gate electrode. Furthermore, figure 3 of Kawate shows the scanning line to be separate from the switching element which could be understood to be far enough to enable the gate electrode to be severed by a laser. Third, it would have been obvious to one of ordinary skill in the liquid crystal art

to have provided the gate electrode with a narrow portion to allow for easy severing of the electrode of Kawate and Yamashita et al. device as per the Japanese patents.

Claims 6 and 7 are rejected under 35 U.S.C. § 103 as being unpatentable over Kawate and Yamashita et al.('656) in view of either of Japanese Patents no. 2-254422 and 2-254422 as applied to claim 4 above, and further in view of Okubo et al.(4761058).

Okubo et al. teaches the use of supplemental capacitors (capacitors in parallel to the LC) to allow for an increased number of elements. This teaching is extremely old and well known. See columns 2 and 3.

It would have been obvious to one of ordinary skill to provide supplemental capacitors, as taught by Okubo et al., to the device of Kawate to increase to number of pixels in the liquid crystal display.

Claims 9 and 11 are rejected under 35 U.S.C. § 103 as being unpatentable over Castleberry and Okubo et al.(4761058).

Okubo et al. teaches a LCD having TFTs and supplemental capacitance. The supplemental capacitance is formed by a conductive layer over which an insulation layer is formed. The insulation layer may be an oxide layer. See figures 17-19.

Castleberry teaches to provide a conductive piece between the pixel electrode and the drain electrode to facilitate electrical connection between the electrodes. See column 5.

It would have been obvious to one of ordinary skill in the liquid crystal art to provide a conductive piece as per Castleberry in the device of Okubo et al. to facilitate electrical connection between the electrodes.

Claims 12 and 14 are rejected under 35 U.S.C. § 103 as being unpatentable over Yamashita et al.(4890097), Yaniv et al.(4666252), Castleberry and Okubo et al.(4761058) and optionally Takano(62-245222).

Yamashita et al. teaches that a defective pixel may be connected to an adjacent pixel whereby the two pixels are both driven by the same signals. The abnormal function of the pixel is hardly noticeable by human vision. See columns 3 and 5.

Castleberry teaches to provide a conductive piece between the pixel electrode and the drain electrode to facilitate electrical connection between the electrodes. See column 5.

Takano(62-245222) teaches a split pixel connected by a conductor.

Yaniv et al. teaches the use of laser fusible links to provide connection for a redundant element when the primary element is not functioning. See column 10, elements 160 and 162.

It would have been obvious to one of ordinary skill in the liquid crystal art to have provided a means to connect adjacent pixels of Okubo et al. in the event any pixel is defective to reduce the visibility of the defect as per Yamashita et al..

Furthermore, it would have been obvious to one of ordinary skill in the liquid crystal art to have selected to most simple structure for the means to connect which is a simple conductor connected by a laser fusible link such as in Yaniv et al.. Finally, it would have been obvious to one of ordinary skill in the liquid crystal art to provide a conductive piece as per Castleberry in the device of above to facilitate electrical connection between the electrodes.

The selection of the conductor structure is further supported by Takano.

Claim 10 would be allowable if rewritten to overcome the rejection under 35 U.S.C. § 112 and to include all of the limitations of the base claim and any intervening claims.

Claims 8 and 15 would be allowable if rewritten or amended to overcome the rejection under 35 U.S.C. § 112.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tsukada et al.(4955697) shows the inherent parasitic capacitors which are formed by a TFT.

Any inquiry concerning this communication should be directed to Ron Trice at telephone number (703) 308-4868.

Ron Trice
August 11, 1991

JOHN S. HEYMAN
EXAMINER
GROUP ART UNIT 254
SPE (acting)

PTO FORM 948
(REV. 5-90)

U.S. DEPARTMENT OF COMMERCE
Patent and Trademark Office

ATTACHMENT TO PAPER NUMBER 3

APPLICATION NUMBER 656845

NOTICE OF DRAFTSMAN'S PATENT DRAWING REVIEW

THE PTO DRAFTSMEN REVIEW ALL ORIGINALLY FILED DRAWINGS REGARDLESS OF WHETHER THEY WERE DESIGNATED AS INFORMAL OR FORMAL.

The drawings filed 2/19/91

A. ☐ are approved.

B. ☑ are objected to under 37 CFR 1.84 for the reason(s) checked below. The examiner will require submission of new, corrected drawings at the appropriate time. Corrected drawings must be submitted according to the instructions listed on the back of this Notice.

1. Paper and ink. 37 CFR 1.84(a)

☐ Sheet(s)_____ Poor.

2. Size of Sheet and Margins. 37 CFR 1.84(b)

Acceptable Paper Sizes and Margins

Margin	Paper Size: 8 1/2 by 14 inches	8 1/2 by 13 inches	DIN size A4 21 by 29.7 cm.
Top	2 inches	1 inch	2.5 cm.
Left	1/4 inch	1/4 inch	2.5 cm.
Right	1/4 inch	1/4 inch	1.5 cm.
Bottom	1/4 inch	1/4 inch	1.0 cm.

☐ Proper Size Paper Required.
All Sheets Must be Same Size.
Sheet(s) _____

☑ Proper Margins Required.
Sheet(s) Fig 6

☑ TOP ☐ RIGHT

☐ LEFT ☐ BOTTOM

3. Character of Lines. 37 CFR 1.84(c)

☐ Lines Pale or Rough and Blurred.
Fig(s)_____

☐ Solid Black Shading Not Allowed.
Fig(s)_____

4. Hatching and Shading. 37 CFR 1.84(d)

☐ Shade Lines are Required.
Fig(s) _____

☐ Criss-Cross Hatching Not Allowed.
Fig(s) _____

☐ Double Line Hatching Not Allowed.
Fig(s) _____

☐ Parts in Section Must be Hatched.
Fig(s) _____

5. Reference Characters. 37 CFR 1.84(f)

☐ Reference Characters Poor or Incorrectly Sized.
Fig(s) _____

☐ Reference Characters Placed Incorrectly.
Fig(s) _____

6. Views. 37 CFR 1.84(i) & (j)

☐ Figures Must be Numbered Properly.

_____

☐ Figures Must Not be Connected.
Fig(s) _____

7. ☐ Photographs Not Approved.

_____

8. ☑ Other. ① Fig Legend Poor 1-22

Telephone inquires concerning this review should be directed to the Chief Draftsman at telephone number (703) 557-6404.

_____
Reviewing Draftsman

3/1/91
Date

SHC 001310

TO SEPARATE, HOLD TOP AND BOTTOM EDGES, SNAP–APART AND DISCARD CARBON

8/13

FORM PTO-892 (REV. 3-78) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	SERIAL NO.	GROUP ART UNIT	ATTACHMENT TO PAPER NUMBER
NOTICE OF REFERENCES CITED	07/656845	254	3
	APPLICANT(S) KANEMORI et al		

U.S. PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
	A	4890097	12/1989	YAMASHITA et al	350	332X	—
	B	4936656	6/1990	YAMASHITA et al	350	333	3/1988
	C	4761058	8/1988	OKUBO et al	350	331T	—
	D	4368523	1/1983	KAWATE	350	334X	—
	E	4804953	2/1989	CASTLEBERRY	350	333X	—
	F	4666252	5/1987	YANIV et al	350	333	—
	G	4955697	9/1990	TSUKADA et al	350	332	4/1988
	H						
	I						
	J						
	K						

FOREIGN PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHTS. DWG	PERTINENT PP. SPEC.
	L	2254422	10/1990	JAPAN					
	M	2254423	10/1990	JAPAN					
	N	62245220	10/1987	JAPAN	TAKANO				
	O								
	P								
	Q								

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

R	
S	
T	
U	

EXAMINER	DATE
TRICE	8/11/91

* A copy of this reference is not being furnished with this office action.
(See Manual of Patent Examining Procedure, section 707.05 (a).)

SHC 001311

#4

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION of

KANEMORI et al

Atty. Ref: 829-61

Serial No. 07/656,845

Group: 254

Filed: 19 February 1991

Examiner: Trice

For: AN ACTIVE MATRIX DISPLAY DEVICE AND A METHOD OF MANUFACTURING THE SAME

* * * * * * * * * * * * * * * * * *

30 August 1991

Honorable Commissioner of Patents
and Trademarks
Washington, D.C. 20231

SUBMISSION OF PRIORITY DOCUMENTS

Sir:

It is respectfully requested that this application be given the benefit of the foreign filing date under the provisions of 35 U.S.C. 119 of the following, a certified copy of which is submitted herewith:

Application No.	Country of Origin	Filed
2-121787	Japan	11 May 1990
2-121788	Japan	11 May 1990
2-125191	Japan	14 May 1990
2-146857	Japan	4 June 1990

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: Larry S. Nixon
Larry S. Nixon
Reg. No. 25,640

LSN:ak
2200 Clarendon Boulevard
14th Floor
Arlington, Virginia 22201
703/875-0400

#4

(Translation)

PATENT OFFICE
JAPANESE GOVERNMENT

This is to certify that the annexed is a true copy of the following application as filed with this Office.

Date of Application: May 11, 1990

Application Number : Heisei 2
Patent Appln. No. 121787

Applicant(s) : SHARP KABUSHIKI KAISHA

Wafer of the Patent Office

November 14, 1990

Satoshi UEMATSU

Commissioner,
Patent Office

Seal of Commissioner of the Patent Office

Appln. Cert. Hei 2-65545

SHC 001314

PTO 93-2707

Japan, Shutsugan
Hei 2-121787

ACTIVE-MATRIX DISPLAY DEVICE

[Aktibu Matorikusugata Hyōji Sōchi]

Yuzuru Kanamori, et al.

UNITED STATES PATENT AND TRADEMARK OFFICE

Washington, D.C. June 1993

Translated by: Schreiber Translations

Country	:	Japan
Document No.	:	Hei 2-121787
Document Type	:	Shutsugan
Language	:	Japanese
Inventor	:	Yuzuru Kanamori, Mikio Katayama, Kiyoshi Nakazawa, Hiroaki Kato, Kozo Yano, Naobumi Kondo
Applicant	:	Sharp K.K.
IPC	:	G 02 F 1/133
Application Date	:	May 11, 1990
Foreign Language Title	:	Aktibu Matorikusugata Hyōji Sōchi
English Title	:	ACTIVE-MATRIX DISPLAY DEVICE

Specification /1[1]

1. Title: Active-Matrix Display Device

2. Claims

1. An active-matrix display device provided with a pair of insulating substrates at least one of which is translucent, scanning lines arranged on one of said pair of substrates, branch scanning lines diverging from said scanning lines, switching elements formed on the front ends of said branch scanning lines, and picture element electrodes connected to said switching elements; wherein the distance from the scanning-line side of said switching elements to said scanning lines is sufficiently large to permit cutting of said branch scanning lines by irradiation with light energy.

3. Detailed Description of the Invention

Industrial Field of Application

The present invention relates to a display device that operates by applying a drive signal via switching elements to picture-element electrodes used for display; specifically, it /2 relates to an active-matrix driven display device in which picture element electrodes are arrayed in a matrix to achieve a high-density display.

Prior Art

In conventional liquid-crystal, EL, and plasma displays, a display pattern is formed on a screen by selectively driving

[1] Numbers in the margin indicate pagination in the foreign text.

picture element electrodes arrayed in a matrix. Voltage is applied between selected picture element electrodes and counter electrodes to optically modulate a display medium such as liquid crystals positioned between sets of such electrodes. This optical modulation is then viewed in the form of a display pattern. A known method of driving picture element electrodes consists of connecting switching elements to each individual picture element electrode in an array of such picture element electrodes to drive them. Switching elements commonly used to selectively drive picture element electrodes include TFT (thin-film transistor) elements, MIM (metal-insulating layer-metal) elements, MOS transistor elements, diodes, and varistors. Active-matrix driven systems permit high-contrast display, and

/3

have already seen practial application in liquid crystal televisions, word processors, computer terminal displays and the like.

Figures 7 and 8 show plan views of active-matrix substrates used in conventional active-matrix display devices. In the substrate of Figure 7, source bus lines 23 are laid out orthogonally to parallel gate bus lines 21. A picture element electrode 41 is positioned in the area within each of the rectangles delimited by gate bus lines 21 and source bus lines 23. A TFT 31, functioning as a switching element, is formed over gate bus line 21 in close proximity to the intersecting portions of gate bus line 21 and source bus line 23. Part of gate bus

line 21 functions as the gate electrode of TFT 31. The drain electrode of TFT 31 is electrically connected to picture element electrode 41. A branch line from source bus line 23 is electrically connected to the source electrode of TFT 31.

The active-matrix substrate of Figure 8 is similar to that of Figure 7 except for a different configuration in the area of /4 TFT 31, ie, TFT 31 is formed over a gate bus line 22 diverging from gate bus line 21. Part of gate bus branch line 22 functions as the gate electrode of TFT 31.

Problems to Be Solved by the Invention

A high-density display made using such display devices requires an array with an extremely large number of picture element electrodes 41 and TFTs 31. However, defective elements are sometimes formed during fabrication of TFTs 31 on the substrate. Picture element electrodes connected to such defective elements produce point defects in the display. Point defects severely compromise the picture quality of the display device and greatly reduce production yield.

The chief causes of point defects can be roughly divided into two groups. The first group comprises malfunctions occurring due to insufficient charging of the picture element electrodes once picture elements are selected by the scan signal (referred to hereinbelow as "ON malfunctions"). The other group comprises malfunctions in which charged picture element electrodes leak their charges when unselected (referred to

hereinbelow as "OFF malfunctions"). ON malfunctions are caused

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by defective TFTs. OFF malfunctions are produced by leakage of electricity from TFTs or between picture element electrodes and bus lines. In both cases, point defects are produced because insufficient voltage is applied between the picture element electrode and the counter electrode. When the voltage between the picture element electrode and the counter electrode is zero during such malfunctions, a bright spot appears when transmittance is at a maximum in the normally white mode, and a dark spot appears when transmittance is at a minimum in the normally black mode.

Such defects can be corrected by laser trimming and the like. However, such repairs must be made to the active-matrix substrate before assembly of the display device. Although defective picture elements are readily detected once assembled into display devices, it is extremely difficult to detect them on the active-matrix substrate alone. In the case of large display devices having 100,000 to 500,000 or more picture elements,

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extremely high-precision testing instruments must be used to determine the electrical characteristics of all the picture element electrodes and discover malfunctioning TFTs. The inspection process becomes complicated, hindering mass production and raising costs. For such reasons, it is presently not possible to undertake repair of defective picture elements using

the above-mentioned lasers at the substrate stage in large display devices having numerous picture elements.

Such problems have been solved in the present invention, the object of which is to provide an active-matrix display device in which even when defective picture elements are produced, it is possible to effect repairs in assembled display devices in such a way as to render the defective picture elements inconspicuous.

Means of Solving the Problems

The active-matrix display device of the present invention is provided with a pair of insulating substrates at least one of which is translucent, scanning lines arranged on one of the two substrates, branch scanning lines diverging from the scanning lines, switching elements formed on the front ends of the branch

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scanning lines, and picture element electrodes connected to the switching elements. The above-stated object is achieved by providing a distance from the scanning-line side of the switching elements to the scanning lines that is large enough to permit cutting of the branch scanning lines by irradiation with light energy.

A configuration is also possible in which an insulating film is sandwiched between the above-mentioned picture element electrodes and a counter electrode is provided for additional capacitance.

Still another configuration is possible in which the above-mentioned picture element electrode is overlapped by the scanning

line adjacent to the scanning line connected to the picture element electrode, providing additional capacitance between the picture element electrodes and the adjacent scanning lines.

Operation

When ON or OFF malfunctions occur in the active-matrix display device of the present invention due to defective switching elements, weak current leaking between signal lines and picture element electrodes, or the like, it is possible to repair the display device in assembled form. First, the scanning branch lines are cut by a laser or the like. Scanning branch lines can be effectively cut in the display device of the present invention since the distance from the scanning line side of the switching elements to the scanning lines is left large enough to permit

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cutting of the scanning branch lines by irradiation with light energy from a laser or the like. The distance between the electrodes connected to the picture element electrodes of the switching elements and the electrodes connected to the signal lines can then be electrically connected by irradiation with light energy. When TFTs are used as switching elements, such electrical connections are made by irradiating the overlapping portions of the source electrodes and the gate electrodes, as well as the overlapping portions of the drain electrodes and the gate electrodes, with light energy. By using a laser as the source of light energy, spotlike holes are opened in these overlapping portions. The source electrodes and gate electrodes

are electrically connected around these holes, as are the drain electrodes and gate electrodes. In this manner, the source and drain electrodes are electrically connected via the gate electrodes.

The voltage applied to picture element electrodes connected to switching elements repaired in the manner set forth above (referred to hereinbelow as "repaired picture element electrodes") will be explained in reference to Figure 6. In

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Figure 6, G_n shows the relation between the signal voltage of the nth scan line (vertical axis) and time (horizontal axis). S_m shows the relation between the signal voltage of the mth scanning line (vertical axis) and time (horizontal axis). P_{nm} shows the voltage applied to a normal picture element electrode connected to the nth scanning line and the mth signal line. P'_{nm} shows the voltage applied to a repaired picture element electrode connected to the nth scanning line and the mth signal line.

As shown in G_n and G_{n+1}, signal (V_{gh}), which selects the serial switching elements, is output to the scanning line for a selection time of T_{on}. Corresponding to the selection time T_{on} of the scanning line, video signal voltage V_0 is output to the signal line. In a normal picture element electrode as shown in P_{nm}, signal voltage V_0 is maintained during the time the element is unselected, T_{off}. Then, when the next selected signal voltage V_{gh} is applied, video signal $-V_0$ is applied to the signal line.

By comparison, a repaired picture element electrode as shown

in P'_{nm} cannot function normally since the video signal from the signal line is continuously applied. However, a repaired picture

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element electrode displays over a period of one cycle a picture element equivalent to the effective value of the video signal applied to the signal line during the cycle. Such a picture element will thus not display a completely bright or dark spot, but the average brightness of picture elements along the signal line, making the defective picture element extremely hard to detect.

Resistance of portions connected as set forth above must be lower than the resistance of switching elements in a selected state (referred to hereinbelow as "ON resistance"). The reason is as follows. The value of the ON resistance of switching elements is set so that only enough current to effect a complete charge is allowed to flow to the picture element electrodes while the switching elements are selected. Thus, when the resistance of portions connected as set forth above is greater than the ON resistance, the signal voltage changing each time a switching element is selected is not reliably applied to repaired picture element electrodes, and the effective value of the voltage applied to such elements decreases. Under these conditions, the difference in brightness between picture elements displayed by repaired picture element electrodes and normal picture elements

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becomes substantial, and defective picture elements can be visually detected.

Embodiments

Embodiments of the present invention are described below.

Figure 1 shows a plan view of the active-matrix substrate used in an embodiment of the display device of the present invention. Figure 3 shows a portion, indicated by section line III-III in Figure 1, of the display device employing the substrate of Figure 1. The active-matrix display device of the present embodiment will be described according to the manufacturing process. In the present embodiment, transparent glass was employed for the insulating substrates. Gate bus line 21, functioning as a scanning line, and gate bus branch line 22, diverging from gate bus line 21, were formed on glass substrate 1. Gate bus line 21 and gate bus branch line 22 are usually formed as single or multiple layers of metals such as Ta, Ti, Al, and Cr; Ta was employed in the present embodiment. Gate bus line 21 and gate bus branch line 22 were formed by patterning a layer /12 of Ta formed by sputtering. Prior to forming gate bus line 21 and gate bus branch line 22, a base coating can be formed of Ta_2O_5 or the like on glass substrate 1. The length of gate bus branch line 22 will be dealt with further below.

A base insulating film 11 was formed of SiN_x over the entire surface, including gate bus line 21 and gate bus branch line 22.

Gate insulating film 11 was formed to a thickness of 3,000 Å by plasma CVD.

TFT 31, functioning as a switching element, was then formed on the forward end of gate bus branch line 22. Part of gate bus branch line 22 functions as the gate electrode 25 of TFT 31. After forming gate insulating film 11 as described above, an amorphous silicon (a-Si) layer which would become channel layer 12 was deposited, followed by an SiN_x film which would become etching stopper layer 13. The thicknesses of the a-Si film was 300 Å and that of the SiN_x film was 2,000 Å. The SiN_x film was then patterned to form etching stopper film 13. A layer of n^+ type

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a-Si to which P (phosphorus) had been added, later to become contact layers 14, 14, was then deposited by plasma CVD to a thickness of 800 Å over the entire surface of the a-Si and etching stopper 13 layers. The above-mentioned a-Si and n^+ type a-Si layers were then simultaneously patterned to form channel layer 12 and contact layers 14, 14.

Next, a Ti layer was formed which would become a source electrode 32, source bus line 23, functioning as the signal line, and a drain electrode 33. Source bus line 23 and the like are normally formed as single or multiple layers of Ti, Al, Mo, Cr or the like; Ti was employed in the present embodiment. Source electrode 32, source bus line 23, and drain electrode 33 were formed by patterning this Ti layer. Source bus line 23

intersects gate bus line 21; the two sandwich gate insulating film 11 between them.

As shown in Figure 1, picture element electrode 41 is formed /14 of ITO (indium tin oxide) in the square area enclosed by gate bus lines 21 and source bus lines 23. Picture element electrode 41 overlaps the end of drain electrode 33 of TFT 31 and is electrically connected to drain electrode 33.

A protective film 17 was deposited over the entire surface of the substrate on which TFT 31 and picture element electrode 41 were formed. Protective film 17 can also be formed with a removed window-shaped section over the center of picture element 41. An orientation film 19 was formed over protective film 17. A counter electrode 3 and an orientation film 9 were formed on a glass substrate 2 opposite glass substrate 1. A liquid crystal layer 18 was sandwiched between substrates 1 and 2 to complete the active-matrix display device of the present embodiment.

The configuration in the proximity of TFT 31 will now be described. Figure 2 shows an enlarged view of the area around TFT 31. As stated above, TFT 31 is formed over gate bus line 22 branching off gate bus line 21. Drain electrode 33 of TFT 31 is electrically connected to picture element electrode 41, and source electrode 32 is electrically connected to source bus line 23. To permit use of light energy from a laser or the like to cut gate bus branch line 22, the distance X between the gate bus /15