

基板と該対向基板との間に表示媒体を封入する工程と、該走査線及び該信号線から該スイッチング素子を介して該絵素電極に駆動電圧を印加し、絵素欠陥を検出する工程と、該絵素欠陥を生じている欠陥絵素電極に接続されているスイッチング素子に光エネルギーを照射して該欠陥絵素電極と信号線とを電氣的に接続し、且つ、該走査支線に光エネルギーを照射して該走査支線を該走査線から切り離す工程と、を包含しており、そのことによって上記目的が達成される。

また、本発明のアクティブマトリクス型表示装置の製造方法は、絶縁性基板と、該基板上に縦横に配線された走査線及び信号線と、該走査線及び該信号線とにスイッチング素子を介して接続された絵素電極と、該信号線及び該絵素電極の下方に絶縁膜を挟んで重畳された導電層と、該絵素電極と該絶縁膜との間に形成された導電片と、を備えたアクティブマトリクス基板を形成する工程と、該アクティブマトリクス基板と対向基板とを貼り合わせて、該アクティブマトリクス基板と該対向

基板との間に表示媒体を封入する工程と、該走査線及び該信号線から該スイッチング素子を介して該絵素電極に駆動電圧を印加し、絵素欠陥を検出する工程と、該絵素欠陥を生じている欠陥絵素電極に接続された該導電片と該導電層との重畳部に光エネルギーを照射して、該欠陥絵素電極と該導電層とを電気的に接続し、且つ、該信号線と該導電層との重畳部に光エネルギーを照射して該信号線と該導電層とを電気的に接続する工程と、を包含しており、そのことによって上記目的が達成される。

(作用)

本発明のアクティブマトリクス型表示装置の製造方法に於て、スイッチング素子の不良、信号線と絵素電極との間の弱いリーク電流の発生等のオン不良又はオフ不良による絵素欠陥が検出されると、表示装置を組み立てた状態で絵素欠陥の修正が行なわれる。まず、絵素欠陥を生じている絵素電極に接続されている走査支線がレーザ光照射等によって切断される。本発明の表示装置の製造方

法では、スイッチング素子の走査線側の側部から該走査線までの距離が、レーザ光等の光エネルギーを照射して走査支線を切断し得る大きさに設定されているので、走査支線を確実に切断し得る。次に、スイッチング素子の絵素電極に接続された電極と、信号線に接続された電極との間が、光エネルギー照射によって電氣的に接続される。これにより、欠陥絵素電極は信号線に直接接続される。

スイッチング素子がTFTである場合には、この電氣的接続は、ソース電極とゲート電極との重畳部、及びドレイン電極とゲート電極との重畳部にそれぞれ光エネルギーを照射することにより行われる。光エネルギーとしてレーザ光を照射することにより、これらの重畳部にはスポット状に穴が開く。この穴の周囲では、ソース電極とゲート電極とが電氣的に接続され、ドレイン電極とゲート電極とが電氣的に接続される。このように、ソース電極とドレイン電極とは、ゲート電極を介して電氣的に接続される。

本発明の導電層及び導電片が形成されるアクテ

ィブマトリクス型表示装置の製造方法に於ても、オン不良又はオフ不良による絵素欠陥が検出されると、表示装置を組み立てた状態で絵素欠陥の修正が行なわれる。まず、信号線と導電層との重畳部に光エネルギーが照射され、信号線と導電層との間が電氣的に接続される。次に、導電層と導電片との重畳部に光エネルギーが照射され、導電層と導電片との間が電氣的に接続される。これにより、信号線と絵素電極とがスイッチング素子を介することなく直接電氣的に接続される。

以上のようにして信号線に接続された絵素電極（以下では「修正絵素電極」と称する）に印加される電圧について、第10図を参照しながら説明する。第10図に於て、 G_n は n 番目の走査線の信号電圧（縦軸）と時間（横軸）との関係を表わし、 S_m は m 番目の信号線の信号電圧（縦軸）と時間（横軸）との関係を表わす。 P_{nm} は、 n 番目の走査線と m 番目の信号線とに接続された正常な絵素電極に印加される電圧を表す。 P'_{nm} は、 n 番目の走査線と m 番目の信号線とに接続された修正絵素電

極に印加される電圧を表わす。

走査線には G_n 、 G_{n+1} に示すように順次スイッチング素子を選択する信号 (V_{gn}) が選択時間 T_{on} の間出力される。走査線の選択時間 T_{on} に対応して、信号線には映像信号電圧 V_g が出力され、正常な絵素電極では P_{nn} に示すように、この信号電圧 V_g が非選択時間 T_{off} の間保持される。そして、次に選択信号電圧 V_{gn} が印加されると、信号線には、 $-V_g$ の映像信号が印加される。

これに対し、修正絵素電極には、 P'_{nn} に示すように、信号線からの映像信号が常に印加されるため、修正絵素電極は正常には機能し得ない。しかし、この修正絵素電極によって表示される絵素は、1周期を通してみるとこの1周期の間に信号線に印加された映像信号の実効値に相当する表示を行う。従って、この絵素は完全な輝点又は黒点となることはなく、信号線に沿って並ぶ絵素の平均的な明るさの表示を行う。従って、この絵素はきわめて判別し難い絵素欠陥となる。

上述のようにして光エネルギー照射によって接

続された部分に於ける電気抵抗は、スイッチング素子の選択状態での抵抗（以下では「オン抵抗」と称する）よりも小さいことが必要である。その理由は以下のようなものである。スイッチング素子のオン抵抗の値は、スイッチング素子が選択されている時間内に絵素電極に電荷を充電し得るだけの電流が流れるように設定されている。従って、上記の接続を行った部分での抵抗がオン抵抗より大きいと、修正絵素電極にはスイッチング素子の選択時間毎に変化する信号電圧が確実に書き込まれず、修正絵素電極に印加される電圧の実効値が小さくなってしまふ。このような状態では、修正絵素電極によって表示される絵素と他の正常な絵素との間で明るさの違いが大きくなり、絵素欠陥として視覚的に認識されることになる。

（実施例）

本発明の実施例について以下に説明する。

第1図に本発明のアクティブマトリクス型表示装置の製造方法によるアクティブマトリクス基板の平面図を示す。第3図に第1図の基板を用いた

表示装置の第1図に於けるⅢ-Ⅲ線に沿った断面図を示す。本実施例のアクティブマトリクス型表示装置の製造工程について説明する。本実施例では、絶縁性基板として透明のガラス基板を用いた。ガラス基板1上に走査線として機能するゲートバス配線21と、該ゲートバス配線21から分岐するゲートバス支線22とを形成した。ゲートバス配線21及びゲートバス支線22は一般にTa、Ti、Al、Cr等の単層又はこれらの多層金属で形成されるが、本実施例ではTaを使用した。ゲートバス配線21及びゲートバス支線22は、スパッタリング法により形成されたTa金属層をパターンニングすることにより形成される。ゲートバス配線21及びゲートバス支線22を形成する前に、ガラス基板1上にTa₂O₅等から成るベースコート膜を形成してもよい。尚、ゲートバス支線22については後述する。

ゲートバス配線21及びゲートバス支線22上には、SiN_xからなるベース絶縁膜11を全面に形成した。ゲート絶縁膜11は、プラズマCVD

法により3000 Åの厚さに形成されている。

次に、ゲートバス支線22の先端部に、スイッチング素子として機能するTFT31を形成した。ゲートバス支線22の一部がTFT31のゲート電極25として機能する。上述のようにゲート絶縁膜11を形成した後、後にチャンネル層12となるアモルファスシリコン(a-Si)層と、後にエッチングストッパ層13となるSiNx層とを堆積させた。a-Si層の厚さは300 Å、SiNx層の厚さは2000 Åである。次に、SiNx層のパターニングを行い、エッチングストッパ層13を形成した。更に、a-Si層及びエッチングストッパ層13上の全面に、後にコンタクト層14、14となる、P(リン)を添加したn⁺型a-Si層を、プラズマCVD法により800 Åの厚さに堆積させた。次に、上記a-Si層及びn⁺型a-Si層のパターニングを同時に行い、チャンネル層12及びコンタクト層14、14を形成した。

次に、後にソース電極32、信号線として機能するソースバス配線23、及びドレイン電極33

となるTi金属層を形成した。上記ソースバス配線23等は、一般に、Ti、Al、Mo、Cr等の単層又はこれらの多層金属で形成されるが、本実施例ではTiを使用した。Ti金属層はスパッタリング法により形成した。このTi金属層をパターンニングすることにより、ソース電極32、ソースバス配線23、及びドレイン電極33を形成した。ソースバス配線23とゲートバス配線21とは、前述のゲート絶縁膜11を挟んで交差している。

次に、第1図に示すように、ゲートバス配線21とソースバス配線23とに囲まれた矩形の領域に、ITO (Indium tin oxide) から成る絵素電極41を形成した。絵素電極41はTFT31のドレイン電極33の端部に重畳され、ドレイン電極33に電氣的に接続されている。

更に、TFT31及び絵素電極41を形成した基板上の全面に、SiNxからなる保護膜17を堆積した。保護膜17は、絵素電極41の中央部の上で除去した窓状の形状としてもよい。保護膜1

7 上には配向膜 19 を形成した。ガラス基板 1 に対向するガラス基板 2 上には、対向電極 3 及び配向膜 9 を形成した。これらの基板 1 及び 2 上の間には液晶層 18 を封入した。

TFT31 の近傍の構成について説明する。TFT31 付近の拡大図を第 2 図に示す。前述のように TFT31 はゲートバス配線 21 から分岐したゲートバス支線 22 上に形成されている。TFT31 のドレイン電極 33 は絵素電極 41 に電気的に接続され、ソース電極 32 はソースバス配線 23 に電気的に接続されている。TFT31 のゲートバス配線 21 側の側部からゲートバス配線 21 までの距離 X は、前述の第 12 図の従来例のそれよりも大きく、レーザ光等の光エネルギーを用いてゲートバス支線 22 を切断し得る大きさである。距離 X が 10 μ m 以上であれば確実に切断できることを確認した。距離 X が小さいと、TFT31 を損傷することなくゲートバス支線 22 を切断することが不可能であるばかりではなく、照射されるレーザ光がゲートバス配線 21 とソースバ

ス配線 2 3 との交差部に悪影響を及ぼし、これらのバス配線 2 1 及び 2 3 間の絶縁不良を起こす場合が生じる。

前述のように基板 1 及び 2 の間に液晶層 1 8 を封入した後、ゲートバス配線 2 1 及びソースバス配線 2 3 から T F T 3 1 を介して全絵素電極 4 1 に駆動電圧を印加し、絵素欠陥を検出した。T F T 3 1 が不良となったり、ソースバス配線 2 3 と絵素電極 4 1 との間に弱いリーク電流が発生している場合には、絵素欠陥が生じる。生じた絵素欠陥の発生位置を確認した後、次のようにして修正が行われる。まず、第 2 図に破線で示す領域 5 1 に光エネルギーを照射することにより、ゲートバス支線 2 2 を切断した。これにより、ゲートバス支線 2 2 はゲートバス配線 2 1 から電氣的に絶縁される。本実施例では光エネルギーとして、Y A G レーザ光（波長 1 0 6 4 n m）を用いた。前述のように、距離 X は十分大きく設定されているので、ゲートバス支線 2 2 の切断は確実に行われる。レーザ光は基板 1 及び 2 の何れの基板から照射し

でもよいが、基板 2 には遮光膜が形成されている場合が多く、その場合には基板 1 側から照射した。本実施例でも基板 1 側から照射した。次に、第 2 図に破線で示す領域 5 2 及び 5 3、即ち、第 3 図の矢印 2 6 及び 2 7 で示す部分にレーザ光を照射した。これにより、領域 5 2 ではソース電極 3 2 とゲート電極 2 5 とが電氣的に接続され、領域 5 3 ではドレイン電極 3 3 とゲート電極 2 5 とが電氣的に接続される。従って、ソース電極 3 2 とドレイン電極 3 3 とはゲート電極 2 5 を介して電氣的に接続される。

以上のようにして修正された T F T 3 1 に接続された絵素電極 4 1 (修正絵素電極) には、ソースバス配線 2 3 の信号が常に印加されるため、修正絵素電極は正常には機能することはできない。しかし、修正絵素電極によって表示される絵素は、ソースバス配線 2 3 に印加される信号の実効値に相当する表示を行うので、この絵素は完全な輝点又は黒点となることはなく、ソースバス配線 2 3 に沿って並ぶ絵素の平均的な明るさの表示を行う

ことになる。従って、この絵素は、きわめて判別し難い絵素欠陥となる。

上述のようにレーザ光照射を行っても、ゲートバス支線 2 2 及び T F T 3 1 上には保護膜 1 7 が形成されているので、熔融した金属等が表示媒体である液晶層 1 8 に混入することもなく、表示には影響しない。また、レーザ光の照射条件を変えることにより、同じレーザ光を用いて金属層間の熔融接続と金属層の切断とを行うことが可能であることが確認されている。

本発明の構成は、第 4 図に示すように、付加容量 4 2 を有するアクティブマトリクス型表示装置にも適用できる。第 4 図の表示装置は、前述の第 1 図～第 3 図に示す実施例に付加容量 4 2 を設けたものである。付加容量 4 2 は、基板 1 上にゲートバス配線 2 1 と並行して設けられた付加容量用電極 2 4 と、絵素電極 4 1 との重畳部（斜線部）に形成されている。第 4 図の表示装置に於いても前述の第 1 図～第 3 図の実施例と同様に絵素欠陥を修正することができる。

更に、本発明は第5図の構成を有するアクティブマトリクス型表示装置にも適用することができる。この表示装置は、第4図の表示装置に於いて、付加容量42の占める部分による絵素の面積が減少するという欠点を解消したものである。この表示装置では、ゲートバス配線21の幅を広げ、絵素電極41の一部と重畳されている。この構成では、隣接する非選択状態のゲートバス配線21を付加容量用電極として用いることができる。しかも、第4図のようにゲートバス配線21と付加容量用電極24との間に隙間が存在しないので、絵素の面積の減少を抑えることができる。この表示装置に於いても、第1図～第3図の実施例と同様に絵素欠陥が修正される。

第6図に本発明の他の表示装置の製造方法によるアクティブマトリクス基板の平面図を示す。第7A図に第6図の導電層34近傍の拡大図を、第7B図に第6図のVII-VII線に沿った断面図を示す。第6図の基板を用いた表示装置の第6図に於けるIII'-III'線に沿った断面図は、前述の第3図と

同様である。本実施例のアクティブマトリクス型表示装置を製造工程に従って説明する。本実施例でも、絶縁性基板として透明のガラス基板を用いた。ガラス基板 1 上に走査線として機能するゲートバス配線 2 1 と、該ゲートバス配線 2 1 から分岐するゲートバス支線 2 2 と、導電層 3 4 とを形成した。ゲートバス配線 2 1、及びゲートバス支線 2 2 には Ta を使用した。導電層 3 4 もゲートバス配線 2 1 と同じ金属によって形成した。ゲートバス配線 2 1、ゲートバス支線 2 2 及び導電層 3 4 は、スパッタリング法により形成された Ta 金属層をパターニングすることにより形成した。ゲートバス配線 2 1、ゲートバス支線 2 2 及び導電層 3 4 を形成する前に、ガラス基板 1 上に Ta₂O₅ 等から成るベースコート膜を形成してもよい。

ゲートバス配線 2 1、ゲートバス支線 2 2 及び導電層 3 4 上には、SiN_x からなるベース絶縁膜 1 1 を全面に形成した。ゲート絶縁膜 1 1 は、プラズマ CVD 法により 3000 Å の厚さに形成されている。

次に、ゲートバス支線 2 2 の先端部に、スイッチング素子として機能する T F T 3 1 を形成した。T F T 3 1 の断面構成は、前述の第 3 図と同様である。ゲートバス支線 2 2 の一部が T F T 3 1 のゲート電極 2 5 として機能する。上述のようにゲート絶縁膜 1 1 を形成した後、a - S i 層と S i N_x層とを堆積させた。a - S i 層の厚さは 3 0 0 Å、S i N_x層の厚さは 2 0 0 0 Å である。次に、S i N_x層のパターニングを行い、エッチングストップ層 1 3 を形成した。更に、a - S i 層及びエッチングストップ層 1 3 上の全面に、P (リン) を添加した n⁺型 a - S i 層を、プラズマ C V D 法により 8 0 0 Å の厚さに堆積させた。次に、上記 a - S i 層及び n⁺型 a - S i 層のパターニングを同時に行い、チャンネル層 1 2 及びコンタクト層 1 4、1 4 を形成した。

次に、T i 金属層をスパッタリング法により形成した。この T i 金属層をパターニングすることにより、ソース電極 3 2、ソースバス配線 2 3、ドレイン電極 3 3、及び導電片 3 5 を形成した。

ソースバス配線 2 3 はゲートバス配線 2 1 と、前述のゲート絶縁膜 1 1 を挟んで交差している。また、第 7 B 図に示すように、ソースバス配線 2 3 は導電層 3 4 の一方の端部にゲート絶縁膜 1 1 を挟んで重畳されるように形成される。導電片 3 5 は導電層 3 4 のソースバス配線 2 3 とは重畳されていない端部の上にゲート絶縁膜 1 1 を挟んで形成される。

次に、第 6 図に示すように、ゲートバス配線 2 1 とソースバス配線 2 3 とに囲まれた矩形の領域に、ITO (Indium tin oxide) から成る絵素電極 4 1 を形成した。絵素電極 4 1 は TFT 3 1 のドレイン電極 3 3 の端部に重畳されている。また、第 7 B 図に示すように、絵素電極 4 1 は導電片 3 5 上にも重畳され、導電片 3 5 に電氣的に接続されている。

更に、絵素電極 4 1 を形成した基板上の全面に、SiN_xからなる保護膜 1 7 を堆積した。保護膜 1 7 上には配向膜 1 9 を形成した。ガラス基板 1 に対向するガラス基板 2 上には、対向電極 3 及び配

向膜 9 が形成されている。これらの基板 1 及び 2 上の間には液晶層 1 8 を封入した。

次に、ゲートバス配線 2 1 及びソースバス配線 2 3 から T F T 3 1 を介して全絵素電極 4 1 に駆動電圧を印加し、絵素欠陥を検出した。T F T 3 1 が不良となったり、ソースバス配線 2 3 と絵素電極 4 1 との間に弱いリーク電流が発生した場合には、絵素欠陥が生じる。絵素欠陥の発生位置を特定した後、次のようにして修正が行われる。まず、第 7 A 図に破線で示すソースバス配線 2 3 と導電層 3 4 との重畳領域 6 1 (第 7 B 図の矢印 6 5 で示す部分)、及び導電層 3 4 と導電片 3 5 との重畳領域 6 2 (第 7 B 図の矢印 6 4 で示す部分) に光エネルギーを照射する。これにより、ソースバス配線 2 3 と導電層 3 4 と導電片 3 5 とは電氣的に接続される。導電片 3 5 と絵素電極 4 1 とは電氣的に接続されているので、絵素電極 4 1 はソースバス配線 2 3 に電氣的に接続されることになる。

以上のようにしてソースバス配線 2 3 に直接接

続された絵素電極 4 1 (修正絵素電極) には、ソースバス配線 2 3 の信号が常に印加されるため、修正絵素電極によって表示される絵素は、完全な輝点又は黒点となることはなく、ソースバス配線 2 3 に沿って並ぶ絵素の平均的な明るさの表示を行うことになる。従って、この絵素は、きわめて判別し難い絵素欠陥となる。

上述のようにレーザ光照射を行っても、導電層 3 4 とソースバス配線 2 3 との重畳部、及び導電層 3 4 と導電片 3 5 との重畳部の上には保護膜 1 7 が形成されているので、熔融した金属等が表示媒体である液晶層 1 8 に混入することもなく、表示には影響しない。

第 6 図の構成も、第 8 図に示すように、付加容量 4 2 を有するアクティブマトリクス型表示装置に適用できる。第 8 図の基板は、第 4 図の基板と同様に、付加容量 4 2 を設けたアクティブマトリクス基板に、導電層 3 4 及び導電片 3 5 を設けたものである。第 8 図の表示装置に於いても前述の第 6 図の実施例と同様に絵素欠陥を修正すること

ができる。

更に、第6図の構成は、第9図の構成を有するアクティブマトリクス型表示装置にも適用することができる。この表示装置は、第5図の基板と同様に、付加容量42の占める部分による絵素の面積の減少を抑えたものである。この表示装置に於いても、第6図の実施例と同様に絵素欠陥が修正される。

上記何れの実施例に於いても、TFT31のゲート電極の上方に、ソース電極及びドレイン電極が形成されている例を示したが、ゲート電極が上に、ソース電極及びドレイン電極が下に形成されたタイプのTFTを用いることもできる。

また、上記の実施例では何れもスイッチング素子としてTFTを用いたが、レーザー光等の光エネルギー照射によって、信号線側の電極と絵素電極側の電極とを電氣的に接続し得るスイッチング素子であれば本発明に用いることができる。

(発明の効果)

本発明のアクティブマトリクス型表示装置の製

造方法によれば、絵素欠陥を容易に検出することができる表示装置の状態、該絵素欠陥を目立たないように修正した表示装置を得ることができる。従って、本発明によれば、高い歩留りで表示装置を生産することができ、表示装置のコスト低下に寄与することができる。

4. 図面の簡単な説明

第1図は本発明の表示装置の製造方法によるアクティブマトリクス基板の平面図、第2図は第1図のTFT近傍の拡大平面図、第3図は第1図の基板を用いた表示装置の第1図に於けるⅢ-Ⅲ線に沿った断面図、第4図及び第5図はそれぞれ本発明の製造方法による付加容量を有するアクティブマトリクス基板の平面図、第6図は本発明の製造方法による他のアクティブマトリクス基板の平面図、第7A図は第6図の導電層近傍の拡大平面図、第7B図は第6図のⅦ-Ⅶ線に沿った断面図、第8図及び第9図はそれぞれ本発明の製造方法による付加容量を有する基板の平面図、第10図は走査線及び信号線に印加される信号と絵素電極の

ができる。

更に、第6図の構成は、第9図の構成を有するアクティブマトリクス型表示装置にも適用することができる。この表示装置は、第5図の基板と同様に、付加容量42の占める部分による絵素の面積の減少を抑えたものである。この表示装置に於いても、第6図の実施例と同様に絵素欠陥が修正される。

上記何れの実施例に於いても、TF T 3 1のゲート電極の上方に、ソース電極及びドレイン電極が形成されている例を示したが、ゲート電極が上に、ソース電極及びドレイン電極が下に形成されたタイプのTF Tを用いることもできる。

また、上記の実施例では何れもスイッチング素子としてTF Tを用いたが、レーザー光等の光エネルギー照射によって、信号線側の電極と絵素電極側の電極とを電氣的に接続し得るスイッチング素子であれば本発明に用いることができる。

(発明の効果)

本発明のアクティブマトリクス型表示装置の製

電圧との関係を示す図、第11図及び第12図はそれぞれ従来のアクティブマトリクス型表示装置に用いられるアクティブマトリクス基板の平面図である。

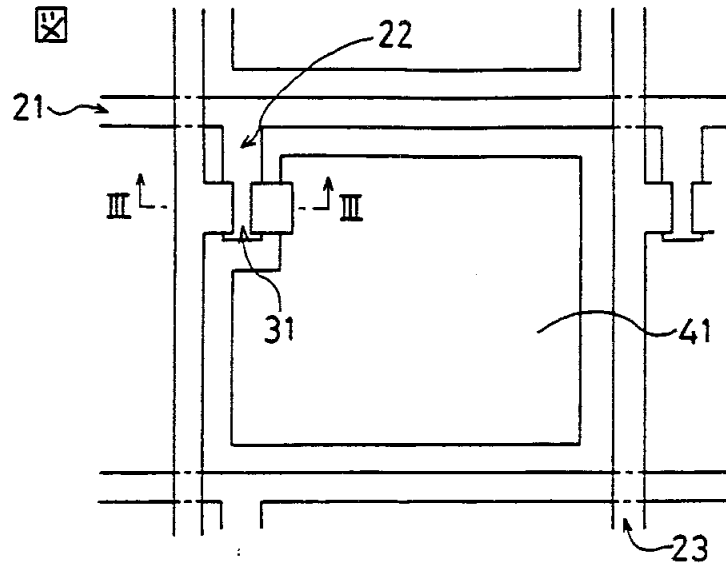
1, 2…ガラス基板、3…対向電極、9, 19…配向膜、11…ゲート絶縁膜、12…チャンネル層、13…エッチングストップ層、14…コンタクト層、18…液晶層、21…ゲートバス配線、22…ゲートバス支線、23…ソースバス配線、24…付加容量用電極、25…ゲート電極、31…TFT、32…ソース電極、33…ドレイン電極、34…導電層、35…導電片、41…絵素電極、42…付加容量。

以 上

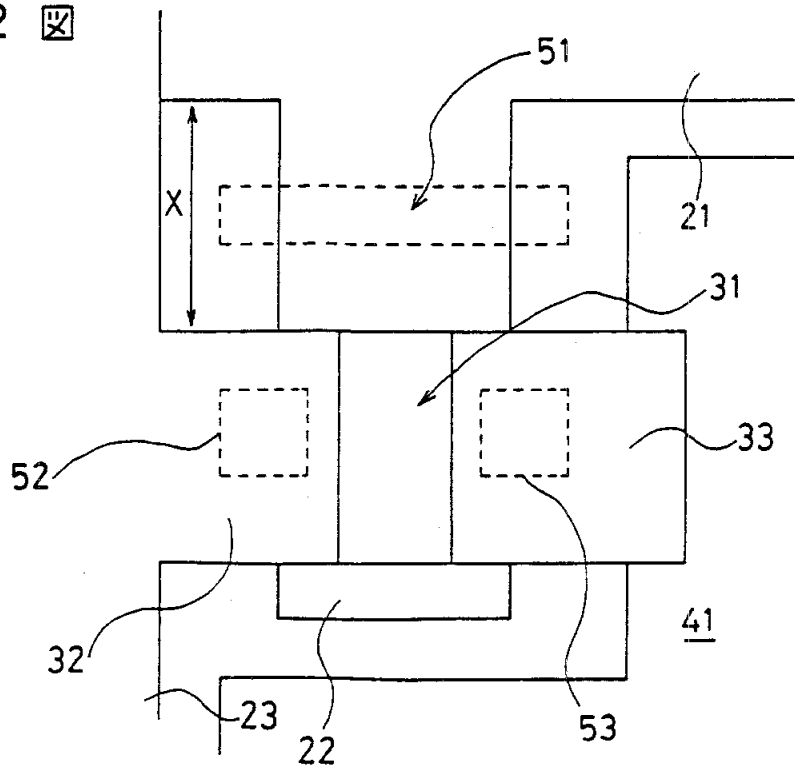
出願人 シャープ株式会社

代理人 弁理士 山本秀策

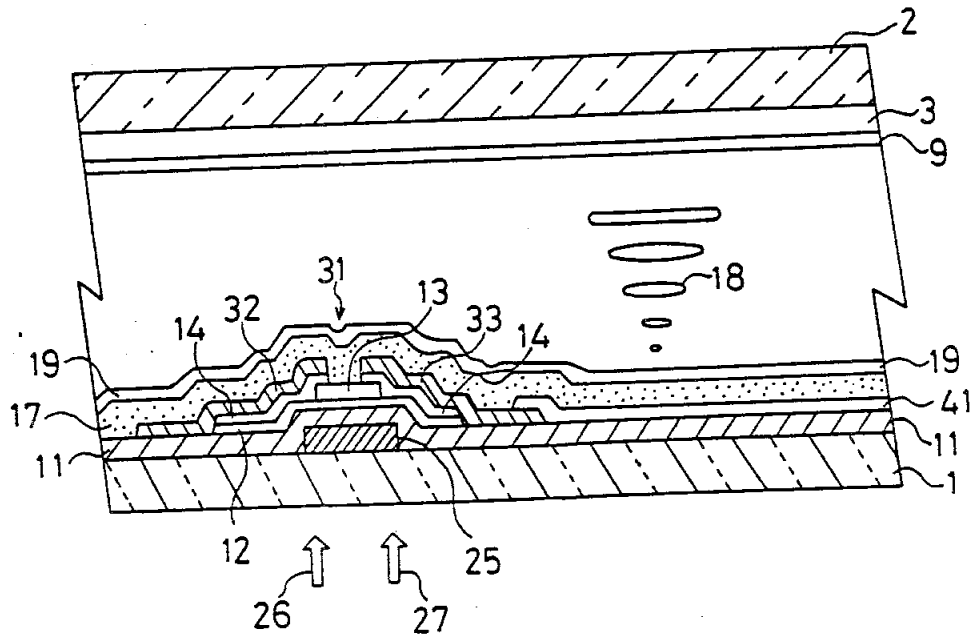
第 1 図



第 2 図

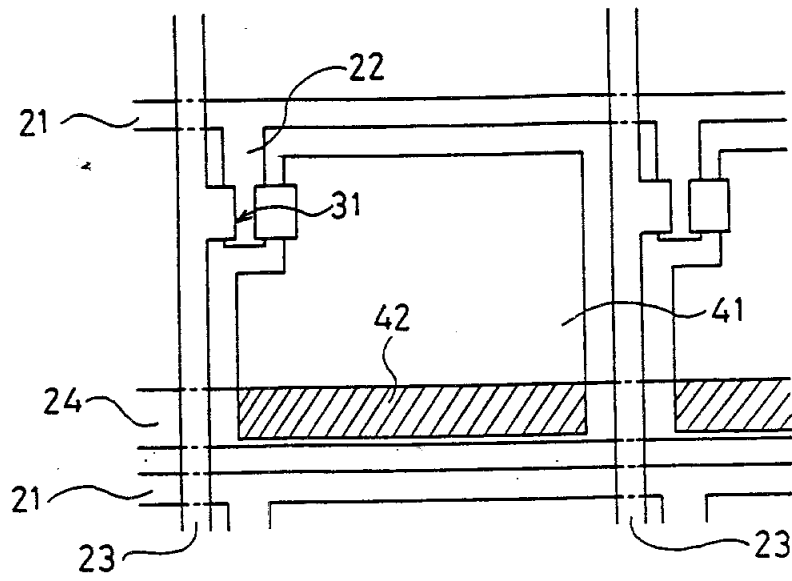


第 3 図

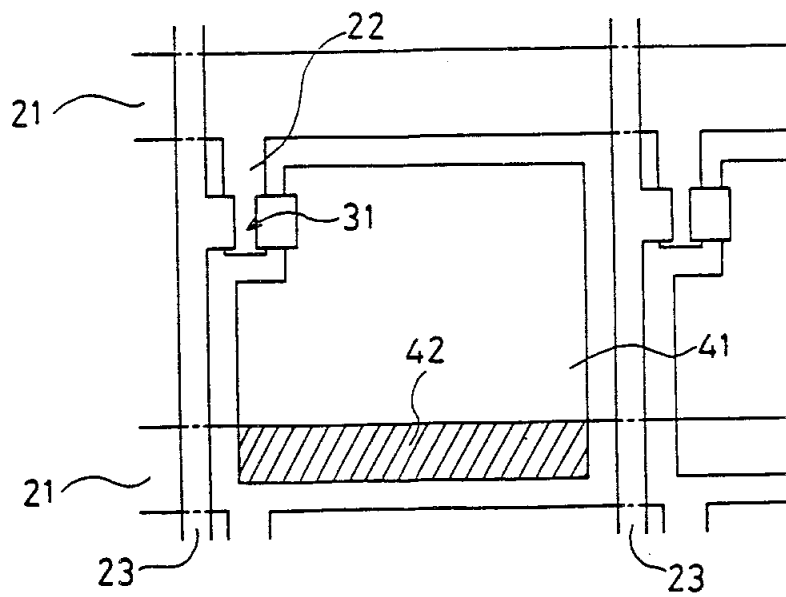


出願人 シャープ株式会社
代理人 弁理士 山本秀策

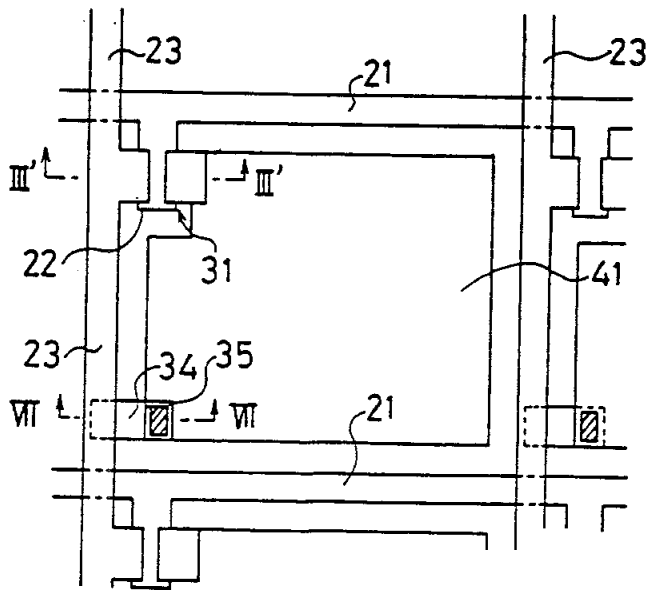
第 4 图



第 5 图

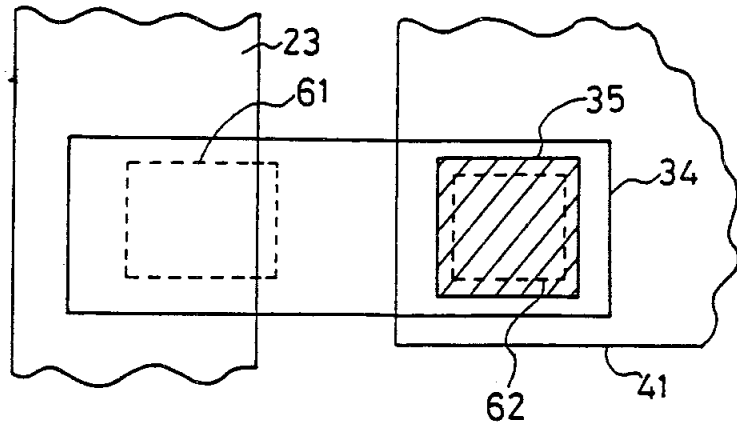


第 6 図

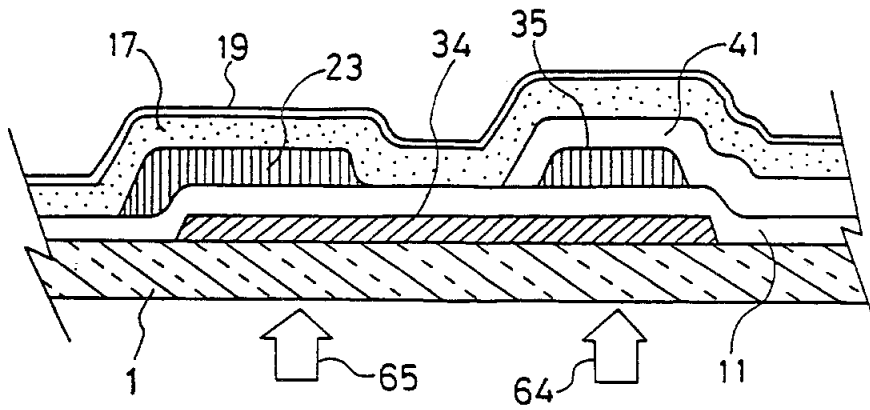


出願人 シャープ株式会社
代理人 弁理士 山本秀策

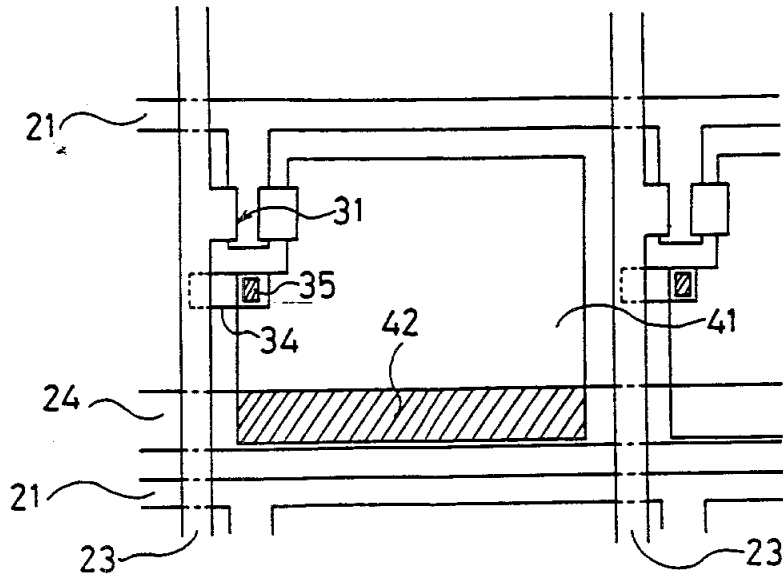
第 7 A 圖



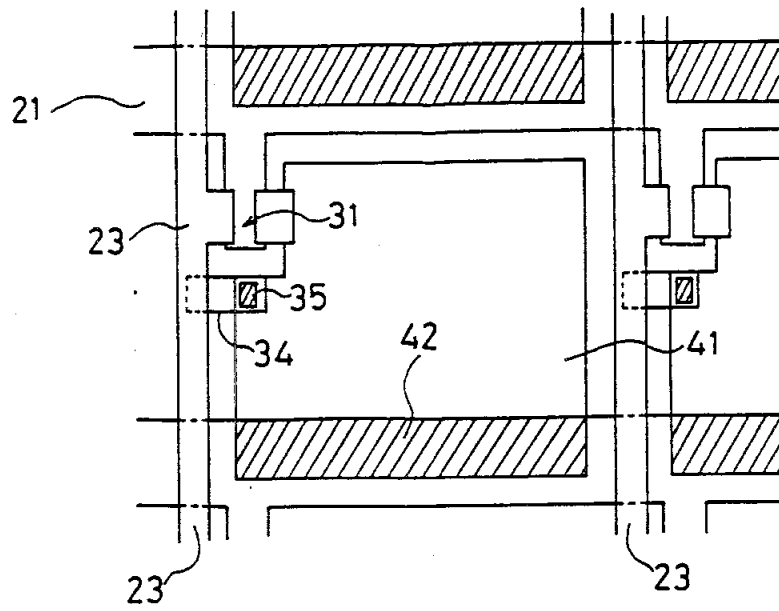
第 7 B 圖



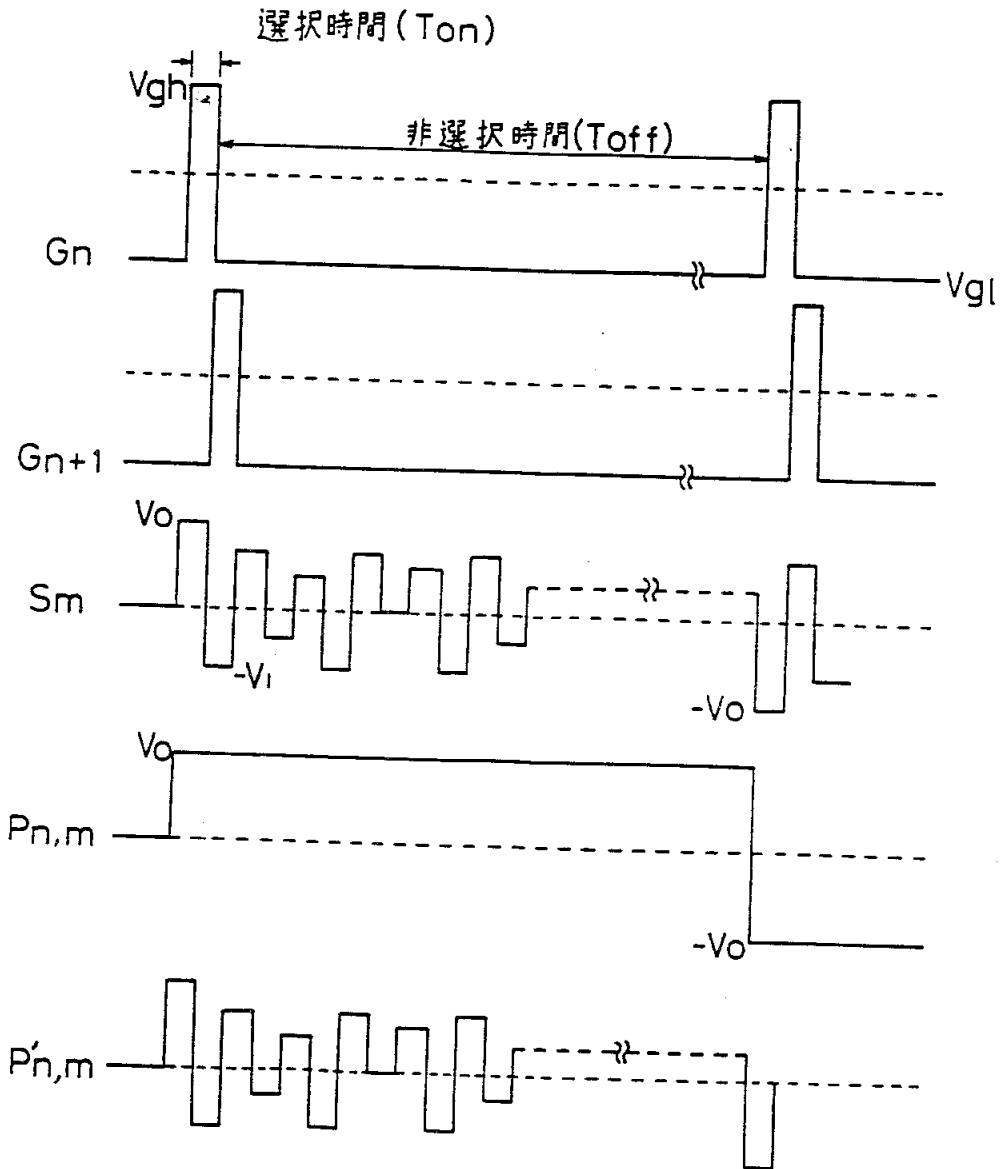
第 8 圖



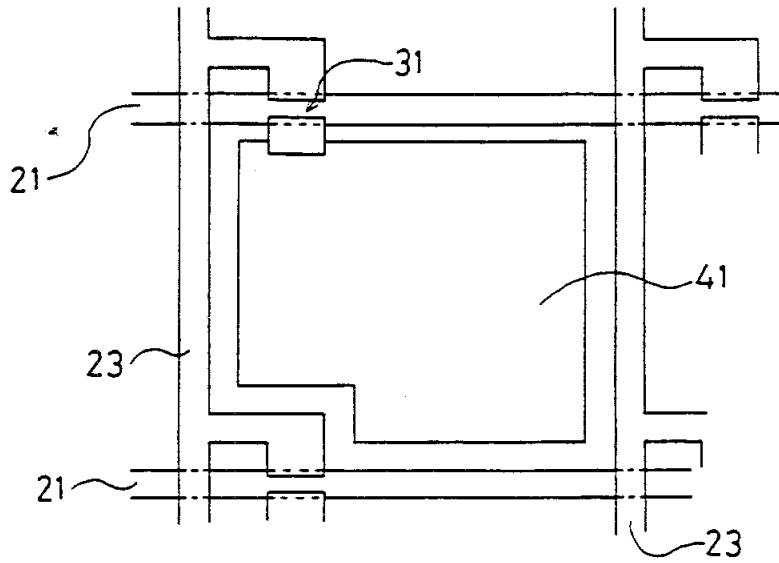
第 9 圖



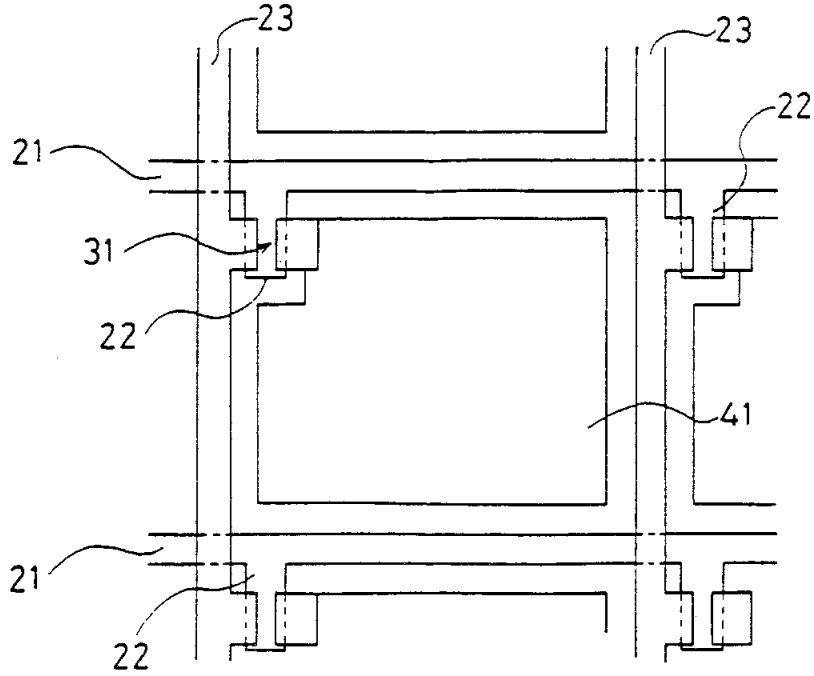
第 10 図



第11 図



第12 図



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

110.00 115 CP 354

5/R. Kemhovef

1/12/92

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JAN 02 1992

Atty Dkt. 829-61
C# M#

Group Art Unit 254

Examiner: R. Trice

Date: December 16, 1991

In re PATENT APPLICATION of:

KANEMORI et al

Serial No. 07/656,845

Filed: February 19, 1991

TITLE: ACTIVE MATRIX DISPLAY DEVICE AND A
METHOD OF MANUFACTURING THE SAME

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

RESPONSE/AMENDMENT/LETTER

This is a response/amendment/letter in the above-identified application and includes an attachment which is hereby incorporated by reference and the signature below serves as the signature to the attachment in the absence of any other signature thereon.

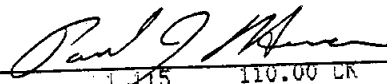
Fees are attached as calculated below:

Total effective claims after amendment () minus highest number previously paid for () (at least 20) = () extra claims x \$20.	\$	
Independent claims after amendment () minus highest number previously paid for () (at least 3) = () extra claims x \$60.	\$	
If proper multiple dependent claims now added for first time, add \$200....	\$	
[X] Petition is hereby made for a 1 month time extension, fee enclosed (\$110 for 1 month; \$350 for 2 months; \$810 for 3 months)	\$	110.00
[] Terminal Disclaimer enclosed, add \$100	\$	
		SUBTOTAL..... \$ 110.00
If "small entity", enter half (1/2) of subtotal and subtract..	-\$ ()	
[] statement filed herewith TOTAL ENCLOSED FEE....	\$	110.00

The Commissioner is hereby authorized to charge any deficiency in the fee(s) filed, or asserted to be filed, or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Account No. 14-1140. A duplicate copy of this sheet is attached.

2200 Clarendon Boulevard
14th Floor
Arlington, Virginia 22201
Telephone: (703) 875-0400

NIXON & VANDERHYTE P.C.
By: Paul J. Henon, Reg. No. 33,626

Signature: 

PJH:lmy 120 RC 12/27/91 07456845

1 115 110.00 LR

SHC 001580

DEC 16 1991

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

*W/A
C.R. Kimbrough
1/2/92*

In re PATENT APPLICATION of

KANEMORI et al

Atty. Ref: 829-61

Serial No. 07/656,845

Group: 254

Filed: February 19, 1991

Examiner: R. Trice

For: ACTIVE MATRIX DISPLAY DEVICE AND
A METHOD OF MANUFACTURING THE
SAME

* * * * *

December 16, 1991

Honorable Commissioner of Patents
and Trademarks
Washington, D.C. 20231

RECEIVED
JAN 02 1992
GROUP 254

AMENDMENT

Sir:

Responsive to the Official Action dated August 15, 1991
(for which petition is hereby made for one (1) month extension
of time), please amend the above-identified application as
follows:

IN THE CLAIMS:

Please amend claims 1, 4, 5, and 8 through 15 as follows:

1. (Amended) An active matrix display device
comprising: a pair of insulating substrates at least one of
which is light transmitting; scanning lines arranged on one of
said pair of substrates; scanning branch lines each branching

all

SHC 001581

from said scanning line, and switching elements each formed on an end portion of said scanning branch line,

wherein the distance between the scanning line side of said switching element and said scanning line is so provided [as to enable said scanning branch line to be cut off by irradiation with light energy] that said scanning line and said switching element are not damaged when said scanning branch line is cut off by the irradiation of light energy.

Contd a1

4. (Amended) An active matrix display device comprising: a pair of insulating substrates at least one of which is light transmitting; scanning lines and signal lines arranged in a vertical and horizontal direction on one of said pair of substrates; scanning branch lines each branching from said scanning line; [and] switching elements each formed on an end portion of said scanning branch line; and pixel electrodes each connected to said switching element, wherein a portion of said scanning branch line other than the portion thereof where said switching element is formed is narrower than that of the portion thereof where said switching element is formed so that said scanning line and said switching element are not damaged when said scanning branch line is cut off by the irradiation of light energy.

a2

5. (Amended) An active matrix display device according to claim 4, wherein said narrower width portion is formed by

[cutting] patterning one or the other side of a portion of said scanning branch line other than the portion thereof where said switching element is formed.

8. (Amended) A method of manufacturing an active matrix display device, comprising the steps of: forming an active matrix substrate which comprises an insulating substrate, scanning lines and signal lines arranged in vertical and horizontal directions on said substrate, scanning branch lines each branching from said scanning line, switching elements each formed on an end portion of said scanning branch line, and pixel electrodes each connected to said switching element, the distance between the scanning line side of said switching element and said scanning line being so provided as to allow said scanning branch line to be cut off by irradiation with light energy;

P1 attaching an opposing substrate to said active matrix substrate with a display medium sandwiched between said active matrix substrate and said opposing substrate;

P1 detecting a pixel defect by observing the brightness at every pixel [by applying] under the condition that a driving voltage is applied to said pixel electrodes from said scanning lines and said signal lines via said switching elements; and

P1 irradiating light energy onto the switching element connected to a defective pixel electrode causing said pixel defect to ~~electrically~~ ^{conductively} connect said defective pixel electrode to

said signal line, and irradiating light energy onto said scanning branch line to disconnect said scanning branch line from said scanning line.

~~Sub E~~

9. (Amended) An active matrix display device comprising: a pair of insulating substrates at least one of which is light transmitting; scanning lines and signal lines arranged in vertical and horizontal directions on one of said pair of substrates; and pixel electrodes each connected to said scanning line and said signal line via a switching element, the active matrix display device further comprising: a conductive layer disposed under said signal line and said pixel electrode; [with] an insulating film interposed between said conductive layer and said signal line, and between said conductive layer and said pixel electrode, respectively [therebetween]; and a conductive piece formed between said pixel electrode and said insulating film.

10. (Amended) An active matrix display device according to claim 9, wherein said conductive layer is [electrically] conductively connected to a scanning line adjacent to said scanning line connected to said pixel electrode and an anodic oxide film is formed on said conductive layer.

11. (Amended) An active matrix display device according to claim 9, further comprising a supplemental capacitor

electrode disposed opposite to said pixel electrode with said insulating film interposed therebetween, wherein said conductive layer is [electrically] conductively connected to said supplemental capacitor electrode and an anodic oxide film is formed on said conductive layer.

Sub C7

Conduct C7

12. (Amended) An active matrix display device comprising: a pair of insulating substrates at least one of which is light transmitting; scanning lines and signal lines arranged in vertical and horizontal directions on one of said pair of substrates; and pixel electrodes each connected to said scanning line and said signal line via a switching element,

the active matrix display device further comprising: a conductive layer disposed under said signal line and a pair of adjacent pixel electrodes, [with] an insulating film interposed between said conductive layer and said signal line, and between said conducting layer and said pixel electrodes, respectively [therebetween]; and conductive pieces each formed between said insulating film and one of said pair of pixel electrodes.

13. (Amended) An active matrix display device according to claim 12, wherein said conductive layer is [electrically] conductively connected to a scanning line adjacent to said scanning line connected to said pixel electrode and an anodic oxide film is formed on said conductive layer.

N
P
K

14. (Amended) An active matrix display device according to claim 12, further comprising a supplemental capacitor electrode disposed opposite to said pixel electrode with said insulating film interposed therebetween, wherein said conductive layer is [electrically] conductively connected to said supplemental capacitor electrode and an anodic oxide film is formed on said conductive layer.

5
15. (Amended) A method of manufacturing an active matrix display device, comprising the steps of:

JA

(1) forming an active matrix substrate which comprises an insulating substrate, scanning lines and signal lines arranged in vertical and horizontal directions on said substrate, pixel electrodes each connected to said scanning line and said signal line via a switching element, conductive layers each disposed under said signal [line] lines and said pixel [electrode] electrodes with an insulating film interposed therebetween, and conductive pieces each formed between said pixel electrode and said insulating film;

(2) attaching an opposing substrate to said active matrix substrate with a display medium sandwiched between said active matrix substrate and said opposing substrate;

(3) detecting a pixel [electrode] defect by observing the brightness at every pixel under the condition that a driving voltage is applied [applying a driving voltage] to said pixel

electrodes from said scanning lines and said signal lines via
said switching elements; and

cont'd a
PI irradiating light energy onto the superimposed portion of
said conductive layer and said conductive piece connected to a
defective pixel electrode causing said pixel defect to
conductively
electrically connect said defective pixel electrode to said
conductive layer, and irradiating light energy onto the
superimposed portion of said signal line and said conductive
layer to *conductively*
electrically connect said signal line to said
conductive layer.

claim 6)

REMARKS

Reconsideration and allowance of all of the claims of record, as presently amended, are respectfully requested.

Applicants appreciate the Examiner's indication that claims 8 and 15 would be allowable if rewritten or amended to overcome the rejection under 35 USC 112, and that claim 10 would also be allowable if rewritten to overcome the rejection of 112, as well as to include all of the limitations of the base claim. In this regard, it will be noted that claims 1, 4, 5 and 8 through 15 have been amended with the Examiner's comments in mind, as well as amending the claims so as to particularly point out and distinctly claim that which applicants consider to be their invention.

In light of such amendments and for the reasons detailed below, it is submitted that all of the claims of record, as presently amended, are in condition for allowance, and action to that end is earnestly solicited.

Claims 8 and 10 through 15 have been rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants consider to be the invention. All of these claims have been amended with the Examiner's criticisms in mind.

For example, claim 8 has been amended to more clearly indicate the manner in which detection is obtained. Moreover, claims 10, 11, 13 and 14 have been amended so as to more clearly specify the nature and manner of the structural connections criticized by the Examiner. Additionally, claim 12 has been modified to more clearly specify the manner in which the insulating film is used in the claimed combination. Furthermore, the terms criticized by the Examiner in claim 15 have been modified in the manner suggested at page 3 of the outstanding Office Action. ---

In light of the noted amendments it is submitted that the claims do in fact set out and circumscribe a particular area with a reasonable degree of precision and particularity when the claims are read in light of the disclosure, as they would be by the artisan. Note In re Johnston, 558 F.2d 1008, 194 USPQ 187 (CCPA 1977) and In re Moore, 439 F.2d 1232, 169 USPQ 236 (CCPA 1971). As such, it is submitted that the cited claims are in full compliance with the second paragraph of Section 112 and that the rejection for indefiniteness should be withdrawn.

Claim 5 stands rejected under 35 USC 112, fourth paragraph, as being of improper dependent form for allegedly failing to further limit the subject matter of a previous claim. In this regard, the Examiner contends that in a device claim a method of fabrication would fail to further limit the scope of the claim

and that, therefore, the formation of the narrower portion by cutting would not further limit the narrower portion.

Applicants respectfully traverse the rejection particularly as presently amended. At the outset, it is noted that whether a claim is directed to an apparatus or a method, the fourth paragraph of 35 USC 112 is merely directed to further limitations on the scope of the "subject matter" of the preceding claim. Thus, even if a pure method step were to be added to a preceding apparatus claim, the scope of the "subject matter" would be limited to the apparatus, further limited by the requirements of the method step.

In any event, claim 4 from which claim 5 depends merely states in pertinent part that the portion of the scanning branch line is narrower than another portion, and claim 5 adds the further limitation that the noted portion is obtained or results in the elimination of one side or the other of the branch line portion in a manner as may be seen in Figures 8A or 8B, for example.

It is submitted that although the manner of obtaining the narrower portion is specified in claim 5, this claim additionally specifies further limitations of a structural nature. Accordingly, it is submitted that such language as is found in claim 5 constitutes a further limitation on the subject

matter recited in claim 4 from which it depends, and is in full compliance with 35 USC 112, fourth paragraph. Note, for example, Ex parte Moelands, 3 USPQ2d 1474 (BPAI 1987).

Claims 1, 2 and 4 through 6 stand rejected under 35 USC 102(b) as being clearly anticipated by Yamashita et al '097 with lines 40-41 of column 1, as well as column 5 and Figure 2, being cited in support thereof.

Additionally, claim 1 stands rejected under 35 USC 102(e) as being clearly anticipated by Yamashita et al '656 with the Examiner indicating that in column 7 the disconnection of electrodes including the gate electrode to a defective switching element is taught.

Alternatively, claims 1 and 4 along with the claims dependent thereon have been rejected for "obviousness" under 35 USC 103 with the teachings of Yamashita et al '097 combined with the Okubo et al patent. It is said that Yamashita et al '097 teaches a device "similar" to applicants' with the only difference being that the capacitor parallel to the LC is not specifically stated as being connected to the adjacent scanning bus. Okubo is said to teach three basic capacitor structures to increase the number of pixel elements and that in light thereof it would have been obvious to the artisan to implement the

unspecified parallel capacitor of Yamashita et al '097 as a capacitor connected to the adjacent scanning bus.

As a still further alternative, claim 1 has been rejected for "obviousness" over Kawate and Yamashita et al '656. In light of the multiple transistor redundancy of Kawate and the disconnection by cutting as demonstrated by Yamashita et al '656, the Examiner concludes that it would have been obvious to have provided the scanning line of Kawate far enough from the switching element to allow for laser cutting of the gate electrode.

As to the rejection of the noted claims for anticipation by that which is taught by either of the Yamashita et al '097 and '656 patent documents, it is submitted that the noted claims, particularly as presently amended, do not "read on" either of these references as would be required for anticipation under 35 USC 102. Note Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983).

Regarding independent claim 1, for example, and the claims dependent thereon, the claimed subject matter specifies that the distance between a scanning line and a scanning line side of a switching element must be sufficiently long such that the scanning line and the switching element are not damaged when the scanning line is cut off by way of irradiating light energy. In

this regard, although Yamashita '097 discloses that a connection 5 is formed so as to be easily cut off as shown by a broken line 50 (column 5, lines 35-37), the reference does not disclose a specific configuration or manner of obtaining the severing without the above noted damage. Yamashita et al '656 is similarly deficient. That is to say, neither of these references discloses specific distances nor do they teach that the severed lines are structured or dimensioned to obtain the results specified in claim 1, for example. In this regard, the paragraph bridging pages 18 and 19 of applicants' disclosure indicates that such dimensioning is important and intentionally included and is distinguishable from the prior art since it has been discovered that where, for example, the line to be cut is less than 10 μm , it is not possible to sever the line without damaging either the switching element, the bus lines, or the insulation between bus lines.

Since these references fail to teach the dimensioning and results specified in independent claim 1, and the claims dependent thereon, it is submitted that the applied references would not fairly place the artisan in possession of that which is claimed, and the claims would not "read on" these references.

Similar observations may be made with regard to independent claim 4 and the claims dependent thereon wherein a pixel electrode can be prevented from being damaged by the inclusion

of the width of a portion of a scanning branch line other than the portion where the switching element is formed being narrower than that portion where the switching element is formed. Neither of the Yamashita et al patent documents teaches such a configuration or the results obtained in these claims, particularly as presently amended.

In light of the above, it is submitted that the rejections for anticipation are inapplicable to the noted claims, particularly as presently amended, and should, therefore, be withdrawn.

Applicants additionally traverse the rejections of claims 1 through 7 under 35 USC 103 based upon Yamashita '097 and Okubo et al or, alternatively, Kawate and Yamashita '656. None of these references including Okubo and Kawate teach or remotely suggest the problem identified by applicants or the claimed solutions thereto. That is to say, neither of the Yamashita et al '097 or '656 references teaches the dimensioning as noted, supra. Moreover, neither Okubo et al nor Kawate disclose the distance of a connection between a scanning line and a switching element or remotely disclose or suggest a construction in which the width of the scanning branch line is made narrow for applicants' purposes or any other. It is, therefore, submitted that any combination of the noted references to obtain that which is specified in the cited claims would require

modifications that are not suggested in any of the references and would appear to require applicants' disclosure and claims as a guide. As succinctly stated by the court in In re Horn, 203 USPQ 969, 971 (CCPA 1979):

"... simplicity and hindsight are not proper criteria for resolving the issue of obviousness."

Claims 2 and 3 stand rejected for obviousness under 35 USC 103 in light of Kawate, Yamashita et al '656 for the reasons noted, supra, as applied to claim 1 when further viewed in light of the teachings of Okubo et al. Claims 4 and 5 also stand further rejected under 35 USC 103 in light of Kawate, Yamashita et al '656 when further viewed in light of either of the Japanese documents '422 and '423. Still further, claims 6 and 7 are rejected for obviousness under 35 USC 103 in light of Kawate, Yamashita et al '656, the Japanese documents '422 and '423 along with the additional citation to the Okubo et al reference.

Applicants respectfully traverse these rejections since even presuming arguendo that it would have been obvious to combine the additional teachings of Okubo and the Japanese documents, as urged by the Examiner, that which is claimed would not result therefrom for the reasons noted, supra, with regard to the rejection of independent claims 1 and 4, for example. That is to say, none of the references discloses nor remotely

suggests the dimensioning of the claimed branch line for any purpose and in particular applicants' claimed purpose. Moreover, the Japanese documents disclose a construction in which the width of a drain electrode of a thin film transistor is made narrow. However, this construction does not have the effect as disclosed and claimed herein. Of more importance, however, it is submitted that neither of these documents can properly be considered as "prior art" under 35 USC 103 since the publication dates of October 1990 are subsequent to applicants' claimed priority dates of May 1990. In this regard it will be noted that certified copies of applicants' priority documents have been submitted (August 30, 1991). Acknowledgment of the safe receipt of these documents is requested.

In light of the above, it is respectfully submitted that the noted rejections of claims 2 through 6 are improper, particularly as presently amended, and the rejections should be withdrawn.

Claims 9 and 11 stand rejected under 35 USC 103 as being unpatentable over Castleberry and Okubo et al. Additionally, claims 12 and 14 stand rejected under 35 USC 103 as being unpatentable over Yamashita et al '097, Yaniv et al, Castleberry, Okubo et al and "optionally" Takano '222.

Applicants respectfully traverse both of these rejections. As to both of the independent claims; namely, 9 and 12, the signal line is adapted to be connected to the pixel electrode, thus voltage is applied to the pixel electrode even when a switching element does not work well. Castleberry, on the other hand, discloses a construction in which a pixel electrode and a drain electrode of a thin film transistor are adapted to be electrically connected to each other through a conductive layer. However, this construction is clearly different from that of the present invention since the signal line and the pixel electrode of the present invention are adapted to be connected to each other without a switching element, such as a thin film transistor. Moreover, Yaniv et al and Takano, along with Yamashita et al '097 and Okubo et al, fail to overcome the noted deficiency.

It is respectfully submitted that if it is indeed possible to combine the references in such a manner as to obtain the claimed subject matter, particularly as presently recited, the elective picking and choosing, along with further modifications which would be necessary, would require applicants' claims as a guide. Under such circumstances, it is submitted that the rejection should be withdrawn.

In light of the applicants' amendments and for the reasons presented, supra, it is submitted that the claims of record as

KANEMORI et al
Serial No. 07/656,845


- 18 -

presently amended are in condition for allowance. If any issues remain to be resolved, the Examiner is urged to contact the attorney for the applicant at the telephone number listed below.

Respectfully submitted,

NIXON & VANDERHYTE P.C.

By:


Paul J. Henon
Reg. No. 33,626

PJH:lmy
2200 Clarendon Boulevard
14th Floor
Arlington, Virginia 22201
703/875-0400

SHC 001598

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION of
KANEMORI et al

Serial No. 56,845

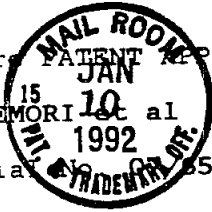
Filed: February 19, 1991

For: ACTIVE MATRIX DEVICE AND A
METHOD OF MANUFACTURING THE SAME

Atty. Ref: 829-61

Group: 254

Examiner: R. Trice



7/B
1-16-92
H. Trice

* * * * *

January 10, 1992

Honorable Commissioner of Patents
and Trademarks
Washington, D.C. 20231

SUPPLEMENTAL AMENDMENT
AND
INFORMATION DISCLOSURE STATEMENT

RECEIVED
JAN 14 1992
GROUP 254

Sir:

In further response to the Official Action dated August 15,
1991, please amend the above-identified application as follows:

IN THE SPECIFICATION:

Page 3, line 9, after "2-254423" and before the period
insert -- and U.S. patent application Serial No. 07/444,732
filed by Katayama et al on December 1, 1989 +.

SHC 001599

INFORMATION DISCLOSURE STATEMENT:

Attached hereto is a listing on Form PTO-1449 of references submitted by applicants in accordance with MPEP Section 609. Copies of the submitted references and translation thereof where available are also attached.

These documents are copies of those documents cited at pages 3 and 4 of the present specification and are considered relevant to the extent succinctly stated in the specification.

Consideration and citation of each of the listed references is requested.

Kanemori et al
Serial No. 07/656,845

- 3 -

REMARKS

The cited documents were recently brought to the attention of the undersigned by the applicants. Consideration of same is requested.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By:



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703/875-0400

SHC 001601

Partial Translation of Japanese Laid-Open Patent Publication

Publication Number : 1-144092

Publication Date : June 6, 1989

Title of the Invention : A PROBE FOR A LIQUID
CRYSTAL PANEL

Application Number : 62-303000

Filing Date : November 30, 1987

Inventor : Y. HIRAI

Applicant : KABUSHIKIKAISYA NIHON MICRONICS

Title: A PROBE FOR A LIQUID CRYSTAL PANEL

A liquid crystal display panel enclosed with liquid crystal is reversely located on a measuring rest having a back-light function. Then, the panel is made to perform display by a probing stick. An image pick-up apparatus judges the display. A laser head provided on the same X-Y stage in which the image pick-up apparatus performs trimming in deficient active matrix elements.

SHC 001603



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#8
2/11/92
K.V.

In re PATENT Application of

KANEMORI et al

Atty. Ref: 829-61

Serial No. 07/656,845

Group 254

Filed: February 19, 1991

Examiner: R. Trice

For: ACTIVE MATRIX DEVICE AND A METHOD OF
MANUFACTURING THE SAME

* * * * *

February 4, 1992

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TRICE
254

Honorable Commissioner of Patents
and Trademarks
Washington, D.C. 20231

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

Further to the Supplemental Amendment and Information Disclosure Statement submitted on January 10, 1992, English Abstracts of Japanese Nos. 2-153324 and 2-294623 are being provided. Consequently, a fresh Form PTO-1449 is submitted herewith indicating the provision of English translations.

The Examiner is requested to initial the attached form PTO-1449 and to return a copy of the initialed document to the undersigned as an indication that the attached references have been considered and made of record.

SHC 001604

Kanemori et al
Serial No. 07/656,845

- 2 -

Respectfully submitted,

NIXON & VANDERHYTE P.C.

By:



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703/875-0400

Attachments (Form PTO-1449)

SHC 001605



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
07/656,845	02/19/91	KANEMORI	Y 029-61

EXAMINER
TRICE, R

NIXON AND VANDERHVE
2200 CLARENDON BLVD. 14TH FLOOR
ARLINGTON, VA 22201

ART UNIT 2504
PAPER NUMBER 9

DATE MAILED: 03/26/92

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

This application has been examined Responsive to communication filed on 12/14/91 + 1/10/92 This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), 7 days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

- 1. Notice of References Cited by Examiner, PTO-892.
- 2. Notice re Patent Drawing, PTO-948.
- 3. Notice of Art Cited by Applicant, PTO-1449. (2)
- 4. Notice of Informal Patent Application, Form PTO-152.
- 5. Information on How to Effect Drawing Changes, PTO-1474.
- 6. 1ST PAGE OF

INVEPIKA

Part II SUMMARY OF ACTION

- 1. Claims 1-15 are pending in the application.
Of the above, claims _____ are withdrawn from consideration.
- 2. Claims _____ have been cancelled.
- 3. Claims _____ are allowed.
- 4. Claims 1-15 are rejected.
- 5. Claims _____ are objected to.
- 6. Claims _____ are subject to restriction or election requirement.
- 7. This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
- 8. Formal drawings are required in response to this Office action.
- 9. The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are acceptable. not acceptable (see explanation or Notice re Patent Drawing, PTO-948).
- 10. The proposed additional or substitute sheet(s) of drawings, filed on _____ has (have) been approved by the examiner. disapproved by the examiner (see explanation).
- 11. The proposed drawing correction, filed on _____, has been approved. disapproved (see explanation).
- 12. Acknowledgment is made of the claim for priority under U.S.C. 119. The certified copy has been received not been received been filed in parent application, serial no. _____; filed on _____.
- 13. Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
- 14. Other

EXAMINER'S ACTION

PTOL-326 (Rev. 9-89)

SHC 001607

Art Unit 2504

The supplemental amendment filed 1-10-92 is objected to under 35 U.S.C. § 132 because it introduces new matter into the specification. 35 U.S.C. § 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: the reference to US application no. 07/444732.

Applicant is required to cancel the new matter in the response to this Office action.

Claim 9 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The word "liens" is misspelled. Applicant has miscopied the word "lines" thereby violating 37 CFR 1.121 (b). Applicant should verify that no other violations exist.

Claims 8 and 15 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The use of the phrase "electrically connect" is not clear. Applicant should amend to comport with the other amended claims. (ie conductively connected)

Claim 5 is rejected under 35 U.S.C. § 112, fourth paragraph, as being of improper dependent form for failing to further limit

Art Unit 2504

the subject matter of a previous claim.

In a device claim, a method of fabrication fails to further limit the scope of the claim. Therefore, the formation of the narrower portion by patterning does not further limit the narrower portion.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --
(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1 and 4-5 are rejected under 35 U.S.C. § 102(e) as being anticipated by Whetten.

Whetten teaches a LCD with TFTs. The gate electrode is connected to the scan line thru a section narrower than the gate electrode within the TFT. Note figure 6a, 8a and 8b.

In the examiner's opinion, and lacking evidence to contrary, the narrower section between the gate electrode and the scan line can be cut without damage to either the scan line or the gate electrode. The reasoning for the examiner's opinion of no damage is as follows:

1. the length of the laser fusible links (66/72 for example) appear to be about the length of the narrower sections;
2. the laser fusible links (66/72) includes 2 laser fusible

Art Unit 2504

link points with some extra length at the edges of each link point and significant extra length between each link point;

3. the length of the link points is equal to the size of the laser beam;

4. if points 1-3 are true then it is evident that the cutting size of the laser beam must be less than length of the narrower section thereby insuring no damage to either the scan line or the gate electrode.

The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 C.F.R. § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order

SHC 001610

Art Unit 2504

for the examiner to consider the applicability of potential 35 U.S.C. § 102(f) or (g) prior art under 35 U.S.C. § 103.

Claims 1-7 are rejected under 35 U.S.C. § 103 as being unpatentable over Yamashita et al. (4090097) and Okubo et al. (4761058).

Yamashita et al. teaches a device similar to applicants' invention. The only differences are the capacitor parallel to the LC is not specifically stated as being connected to the adjacent scanning bus and the amount of space provided between the scanning bus and the TFT for disconnection of the TFT.

It would have been obvious to one of ordinary skill in the liquid crystal art to have provided enough distance from the scan line to the TFT to avoid damaging the scan line and to avoid the possibility of connecting the source and drain of the TFT. Firstly, if the scan line is cut, the width of the line will be decreased which will increase the resistance of the scan line which is known to be disadvantageous. Furthermore, the possibility of severing the scan line is also avoided. Severing the scan line would result in a line defect which is worse than a point defect. Secondly, if the laser cuts into the TFT there is a possibility that the gate will be connected to the source and drain electrodes which will connect the pixel electrode to the source bus resulting in a defective pixel and extra capacitive loading. The capacitive loading would increase the time the pixel electrode requires to charge and requiring the bus to carry

SHC 001611

Serial No. 07/656845

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Art Unit 2504

up to twice the current.

Okubo et al. teaches the use of parallel capacitors to increase the number of pixel elements. Okubo et al. teaches three basic parallel capacitor structures: to the same scanning bus as the TFT, to the scanning bus adjacent the TFT and to a non-scanning bus.

It would have been obvious to one of ordinary skill in the liquid crystal art to have realized the unspecified parallel capacitor of Yamashita et al. as a capacitor connected to the adjacent scanning bus because this realization is one of three conventional configurations which allow for an increased number of pixels as per Okubo et al..

Claims 1-7 are rejected under 35 U.S.C. § 103 as being unpatentable over Whetten and Okubo et al..

Okubo et al. teaches the use of parallel capacitors to increase the number of pixel elements. Okubo et al. teaches three basic parallel capacitor structures: to the same scanning bus as the TFT, to the scanning bus adjacent the TFT and to a non-scanning bus.

It would have been obvious to one of ordinary skill in the liquid crystal art to have included a capacitor connected to the adjacent scanning bus in the device of Whetten to increase number of pixels as per Okubo et al..

Claims 9 and 11 are rejected under 35 U.S.C. § 103 as being

SHC 001612

unpatentable over Castleberry and Okubo et al. (4761058).

Okubo et al. teaches a LCD having TFTs and supplemental capacitance. The supplemental capacitance is formed by a conductive layer over which an insulation layer is formed. The insulation layer may be an oxide layer. See figures 17-19.

Castleberry teaches to provide a conductive piece between the pixel electrode and the drain electrode to facilitate electrical connection between the electrodes. See column 5.

It would have been obvious to one of ordinary skill in the liquid crystal art to provide a conductive piece as per Castleberry in the device of Okubo et al. to facilitate electrical connection between the electrodes.

Claims 12 and 14 are rejected under 35 U.S.C. § 103 as being unpatentable over Yamashita et al. (4890097), Yaniv et al. (4666252), Castleberry and Okubo et al. (4761058) and optionally Takano (62-245222).

Yamashita et al. teaches that a defective pixel may be connected to an adjacent pixel whereby the two pixels are both driven by the same signals. The abnormal function of the pixel is hardly noticeable by human vision. See columns 3 and 5.

Castleberry teaches to provide a conductive piece between the pixel electrode and the drain electrode to facilitate electrical connection between the electrodes. See column 5.

Takano (62-245222) teaches a split pixel connected by a

conductor.

Yaniv et al. teaches the use of laser fusible links to provide connection for a redundant element when the primary element is not functioning. See column 10, elements 160 and 162.

It would have been obvious to one of ordinary skill in the liquid crystal art to have provided a means to connect adjacent pixels of Okubo et al. in the event any pixel is defective to reduce the visibility of the defect as per Yamashita et al.. Furthermore, it would have been obvious to one of ordinary skill in the liquid crystal art to have selected the most simple structure for the means to connect which is a simple conductor connected by a laser fusible link such as in Yaniv et al.. Finally, it would have been obvious to one of ordinary skill in the liquid crystal art to provide a conductive piece as per Castleberry in the device of above to facilitate electrical connection between the electrodes.

The selection of the conductor structure is further supported by Takano.

Claim 10 would be allowable if rewritten to overcome the rejection under 35 U.S.C. § 112 and to include all of the limitations of the base claim and any intervening claims.

Claims 8 and 15 would be allowable if rewritten or amended to overcome the rejection under 35 U.S.C. § 112.

The prior art made of record and not relied upon is

considered pertinent to applicant's disclosure.

Taukađa et al. (4955697) shows the inherent parasitic capacitors which are formed by a TFT.

Ukai et al. shows supplemental capacitors, one of which is laser welded to connect it to the circuit.

Katayama et al. is the prior art improperly inserted into the specification.

Response to Remarks

Applicant is requested to provide copies of cited case law with markings indicating those portions relied upon.

Method claim limitations in a device claim are not further limiting since they cannot impart patentability. See In re Dike 394 f.2d 584, 157 USPQ 581 (CCPA). Accordingly, a 35 USC § 112, fourth paragraph rejection will be maintained until all other rejections and objections are obviated. In other words, no weight will be given to any method limitation and no examination upon the merits of the method limitation will be given since such examination cannot result in patentable subject matter.

With regard to applicants' statement that the foreign documents '422 and '423 are not prior art because applicant has foreign priority dating back before the publication date of the documents is incorrect. These documents can only be removed as prior art by submission of certified copies of the priority documents and by providing a certified translation of at least

Serial No. 07/656845

-10-

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one priority document containing the material relied upon in the foreign documents. Accordingly, the foreign documents are prior art.

In regard to claims 9, 11-12 and 14, the breath of claims 9 and 11 is such that they read upon totally unrelated devices. The selection of a conductor rather than a transistor in claims 12 and 14 would have been obvious to one of ordinary skill in the art because one would realize that the two structures provide substantially the same function. However, the transistor provides an extra level of redundancy since can two transistors provide a signal to the defect pixel.

Any inquiry concerning this communication should be directed to Ron Trice at telephone number (703) 308-4868.

Ron Trice

Ron Trice
Patent Examiner
March 22, 1992

Stanley D. Miller

Stanley D. Miller
Supervisory Patent Examiner
Group Art Unit 2504

SHC 001616

FORM PTO-892 (REV. 3-78)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		SERIAL NO. 07/656845	GROUP/ART UNIT 2504	ATTACHMENT TO PAPER NUMBER 9	
NOTICE OF REFERENCES CITED				APPLICANT(S) KANEMORI et al.			
U.S. PATENT DOCUMENTS							
•	DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE	
A	5042916	8/1991	YKAI et al	359	59	10/1990	
B	5062690	11/1991	Whetten	359	59	6/1989	
C	5076666	12/1991	KATAYAMA et al	359	59	12/1989	
D							
E							
F							
G							
H							
I							
J							
K							
FOREIGN PATENT DOCUMENTS							
•	DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHTS. PP. DWG. SPEC.
L							
M							
N							
O							
P							
Q							
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)							
R							
S							
T							
U							
EXAMINER TRICE				DATE 3/22/92			
* A copy of this reference is not being furnished with this office action. (See Manual of Patent Examining Procedure, section 707.05 (a).)							



2504

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re APPLICATION of

Atty. Ref: 829-61

KANEMORI, Yuzuru

Serial No.: 07/656,845

Filed: FEB 19 91

For: AN ACTIVE MATRIX DISPLAY DEVICE AND A METHOD OF MANUFACTURING THE SAME

#10cp
6/24/92
RECEIVED
JUN 24 1992
GROUP 250

June 5, 1992

CHANGE OF ADDRESS OF ATTORNEY

Honorable Commissioner of Patents and Trademarks
Washington, DC 20231

Sir:

The undersigned attorney of record for the captioned patent has changed his address and requests that all communications and papers related to the captioned patent be directed to the new address as follows:

NIXON & VANDERHYE P.C.
8th Floor
1100 North Glebe Road
Arlington, Virginia 22201-4714
Telephone: 703/816-4000

Respectfully submitted,

NIXON & VANDERHYE P.C.

Larry S. Nixon

Larry S. Nixon, Reg No. 25,640

NIXON & VANDERHYE P.C.
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Tel: 703/816-4000

SHC 001618

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION

KANEMORI et al

Serial No. 07/656,845

Filed: February 19, 1991

For: ACTIVE MATRIX DEVICE AND A
METHOD OF MANUFACTURING THE SAME



Atty. Ref: 829-61

Group: 2504

Examiner: R. Trice

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attach
FS
6-26-92

* * * * *

June 25, 1992

Honorable Commissioner of Patents
and Trademarks
Washington, D.C. 20231

RECEIVED
JUN 26 1992
GROUP 250

AMENDMENT

Sir:

Responsive to the Official Action dated March 26, 1992,
please amend the above-identified application as follows:

IN THE SPECIFICATION:

Page 3, line 9, cancel the amendment made thereto on
January 10, 1992.

IN THE CLAIMS:

Cancel claims 1 through 7.

Please amend claims 8, 9, 12 and 15 as follows:

SHC 001619

Claim 8, line 22, delete "electrically" and insert
-- conductively --.

C¹

9. (Twice Amended) An active matrix display device comprising: a pair of insulating substrates at least one of which is light transmitting; scanning [lines] lines and signal lines arranged [in vertical and horizontal directions] orthogonally on one of said pair of substrates; and pixel electrodes each connected to [said] an adjacent scanning line and [said] an adjacent signal line via a switching element, [the active matrix display device further comprising:] a conductive layer disposed under said adjacent signal line and said pixel electrode and extending therebetween; an insulating film interposed between said conductive layer and said adjacent signal line, and between said conductive layer and said pixel electrode, respectively; and a conductive piece formed between said pixel electrode and said insulating film and partially overlapping said conductive layer for facilitating a conductive connection between said conductive layer of and said pixel electrode.

C²

12. (Twice Amended) An active matrix display device comprising: a pair of insulating substrates at least one of which is light transmitting; scanning lines and signal lines arranged [in vertical and horizontal directions] orthogonally on one of said pair of substrates; and pixel electrodes each

connected to [said] an adjacent scanning line and [said] an adjacent signal line via a switching element,

Cont
[the active matrix display device further comprising:] a conductive layer disposed under said adjacent signal line and extending between a pair of adjacent pixel electrodes; an insulating film interposed between said conductive layer and said adjacent signal line, and between said conducting layer and said pixel electrodes, respectively; and conductive pieces each formed between said insulating film and one of said pair of pixel electrodes and overlapping said conductive layer for facilitating conductive connections between said conductive layer and said pixel electrodes.

Claim 15, in each of lines 23 and 26, delete "electrically" and insert -- conductively --.

REMARKS

Reconsideration and allowance of the claims of record, as presently amended, are respectfully requested.

Applicants appreciate the Examiner's indication that claims 8, 10 and 15 would be allowable if rewritten to overcome the deficiencies noted under 35 USC 112, second paragraph, and/or if rewritten in independent form. In this regard claims 8, 9, 12 and 15 have been amended in order to more particularly and distinctly claim that which applicants consider to be their invention.

Additionally, as required by the Examiner, the Supplemental Amendment of January 10, 1992 at page 3 of the specification which referred to a commonly assigned co-pending application has been cancelled.

Still further, claims 1 through 7 have been cancelled; and, accordingly, the rejections of claim 5 under 35 USC 112, fourth paragraph, the rejection of claims 1, 4 and 5 under 35 USC 102, as well as the rejections of claims 1 through 7 for "obviousness" under 35 USC 103 are moot.

In light of the above noted modifications and for the reasons detailed below, it is submitted that the remaining

claims; namely, claims 8 through 15, as presently amended are in condition for allowance, and action to that end is solicited.

Claims 8, 9 and 15 were rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as their invention. More specifically, as to claims 8 and 15, the Examiner was of the view that the phrase "electrically connect" was unclear and that "conductively" connect should be substituted. Claim 9 was said to be in violation of 37 CFR 1.121(b) and, therefore, indefinite since the word "lines" at line 3 was misspelled.

These claims have been modified in the manner suggested by the Examiner and, accordingly, are considered to be in full compliance with the requirements of the second paragraph of Section 112.

Claims 9 and 11 were rejected under 35 USC 103 as being unpatentable over Castleberry and Okubo et al (hereinafter Okubo).

Applicants respectfully traverse the rejection since independent claim 9, particularly as presently amended, clearly recites a conductive layer which extends from a point under a signal line to a point under a pixel electrode with an

insulating film separating the conductive member from the signal line and the pixel electrode. Moreover, the claim recites that a conductive piece is formed between the pixel electrode and the insulating film overlapping the conductive film so as to facilitate a conductive connection between the conductive layer and the pixel electrode.

The Examiner in his rejection has related the conductive layer of claim 9 to the supplemental capacitance layer 1b of Okubo and has combined the Okubo device with Castleberry so as to supply the conductive piece between the pixel electrode and the supplemental capacitance layer.

Initially, applicants submit that there is no teaching or suggestion in the references which would provide a motivation to make the combination urged by the Examiner. To the contrary, applicants submit that a consideration of the teachings of the references would teach away from such a combination. That is to say, to conductively connect the pixel electrode and the supplemental capacitance layer of Okubo would defeat the purpose of the capacitance layer. Thus, the artisan would not add a conductive piece to "facilitate" such a connection as specified in claim 9. Moreover, claim 11 which depends from claim 9 would not have been obvious for at least the same reasons.

Accordingly, it is submitted that the evidence provided by Okubo and Castleberry would lead away and thus not support the conclusion of obviousness. Therefore, it is submitted that the rejection is improper and should be withdrawn.

Claims 12 and 14 (and presumedly claim 13) stand rejected under 35 USC 103 as being unpatentable over Yamashita et al ('097), Yaniv et al ('252), Castleberry and Okubo et al and optionally Takano ('222).

The rejection is traversed since it is respectfully submitted that the rejection merely represents a selective picking and choosing of bits and pieces of several references using applicants' claims as a guide in order to arrive at the claimed subject matter. Note In re Kamm, 452 F.2d 1052, 172 USPQ 298 (CCPA 1972) and Ex parte Clapp, 227 USPQ 972 (BPAI 1985). For the convenience of the Examiner highlighted portions of these decisions are attached hereto.

A review of the somewhat diverse teachings of the references themselves offer little or no teachings or suggestions in support of the selection and modification of the parts cited by the Examiner. In this regard, it is submitted that if the proposed combination would have been obvious at all, it would only be so by way of hindsight reconstruction. Additionally, the Examiner's rationale would appear to be based

upon frequent reference to the claims for a determination of what bits and pieces are required and how they should be combined. That is to say, the Examiner combines the pixels of Okubo with the teachings of Yamashita to use a transistor to combine adjacent pixels when a switching element is faulty and then replaces the transistor with a conductive layer (which is presumedly the supplemental capacitance layer of Okubo) since a conductor is said to be more simplistic than a transistor. Thereafter, the Examiner adds in the conductive pieces of Castleberry and then fuses the pixels to the conductive layer in accordance with the alleged teachings of Yaniv.

Initially it is noted that if the Examiner is using the supplemental capacitance layer of Okubo to connect the pixels together, then the purpose of the supplemental capacitance layer would defeat the combination. That is to say, the noted purpose; namely, providing additional capacitance, would be eliminated, as indicated, supra, with regard to the rejection of claims 9 and 11. Moreover, Yamashita teaches using a complex transistor scheme to connect adjacent pixels. In this regard, if anything, Yamashita would teach away from the use of a "simple structure" such as a conductor since the artisan would not have used the more complex transistor arrangement if the simple conductor arrangement were indeed obvious. Additionally, if the Examiner did not intend to use the supplemental capacitance layer of Okubo in the combination (which would then

make it unclear why Okubo is used at all), Takano teaches employing a conductor permanently affixed to separate halves of the same pixel without an insulating film located between the conductor and the pixel. Thus, to combine the teachings of Takano with the pixels of Okubo would result in a structure where adjacent pixels are always interconnected regardless of fault in the switching element. Clearly, this is not what is specified in the noted claims.

In light of the above it is respectfully submitted that the artisan viewing only the teachings found in the several applied references would not have found applicants' claimed subject matter obvious without first reading applicants' disclosure. Under such circumstances, it is submitted that the claimed invention when considered as a whole is not directed to obvious subject matter within the meaning of 35 USC 103 in light of the applied references. Accordingly, the rejection should be withdrawn.

In view of the above noted amendments and the reasons detailed, supra, it is submitted that all of the claims of record, as presently amended, are in condition for allowance, and action to that end is solicited.

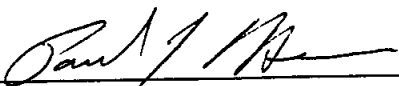
Kanemori et al
Serial No. 07/656,845

- 10 -

If any issues remain to be resolved, the Examiner is urged to contact the attorney for the applicants at the telephone number listed below.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: 
Paul J. Henon
Reg. No. 33,626

PJH:lmy
1100 North Glebe Rd.
8th Floor
Arlington, VA 22201-4714
703-816-4000

SHC 001628



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Atty Dkt. 829-61
C# M#

In re APPLICATION of:

KANEMORI et al

Group Art Unit 2504 ✓

Serial No. 07/656,845

Examiner: R. Trice

Filed: February 19, 1991

Date: June 25, 1992

TITLE: ACTIVE MATRIX DEVICE AND A METHOD OF
MANUFACTURING THE SAME

RECEIVED

JUN 26 1992

GROUP 250

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

RESPONSE/AMENDMENT/LETTER

This is a response/amendment/letter in the above-identified application and includes an attachment which is hereby incorporated by reference and the signature below serves as the signature to the attachment in the absence of any other signature thereon.

Fees are attached as calculated below:

Total effective claims after amendment () minus highest number previously paid for () (at least 20) = () extra claims x \$20. \$

Independent claims after amendment () minus highest number previously paid for () (at least 3) = () extra claims x \$72. \$

If proper multiple dependent claims now added for first time, add \$220.... \$

[] Petition is hereby made for a month time extension, .. \$
fee enclosed (\$110 for 1 month; \$350 for 2 months;
\$810 for 3 months)


[] Terminal Disclaimer enclosed, add \$110 \$
SUBTOTAL..... \$

If "small entity", enter half (1/2) of subtotal and subtract.. -\$()
[] statement filed herewith TOTAL ENCLOSED FEE.... \$ 0.00

The Commissioner is hereby authorized to charge any deficiency in the fee(s) filed, or asserted to be filed, or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Account No. 14-1140. A duplicate copy of this sheet is attached.

1100 North Glebe Road
8th Floor
Arlington, Virginia 22201-4714
Telephone: (703) 816-4000

NIXON & VANDERHYE P.C.
By: Paul J. Henon, Reg. No. 33,626

Signature: 

PJH: lmy

SHC 001629

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#12



In re PATENT Application of

KANEKORI et al

Atty. Ref: 829-61

Serial No. 07/656,845

Group: 2504

Filed February 19, 1991

Examiner: R. Trice

For: ACTIVE MATRIX DEVICE AND A METHOD OF MANUFACTURING THE SAME

August 18, 1992

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2501
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Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

GROUP 250

AUG 20 1992

INFORMATION DISCLOSURE STATEMENT

RECEIVED

Sir:

Consideration of the Information Disclosure Statement submitted herewith pursuant to 37 CFR 1.97(c) is requested. Attention is directed to the attached copy of an EPO Search Report issued June 15, 1992, with respect to this disclosure and to a copy of each reference cited therein along with a listing of said references on a Form PTO-1449.

The references are considered relevant for the reasons succinctly stated in the attached Search Report.

Pursuant to 37 CFR 1.197(e) the undersigned registered attorney hereby certifies that the information contained herein was cited in a communication from a foreign patent office in a counterpart foreign patent application not more than three months prior to the filing of this statement.

SHC 001630

Kanemori et al
Serial No. 07/656,845

- 2 -

Official citation and consideration of the enclosed references are requested.

The Examiner is requested to initial the attached form PTO-1449 and to return a copy of the initialed document to the undersigned as an indication that the attached references have been considered and made of record.

Respectfully submitted,

NIXON & VANDERHYTE P.C.

By: 

Paul J. Henon
Reg. No. 33,626

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Attachments (Form PTO-1449)

SHC 001631



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
07/656,845	02/19/91	KANEMORI	Y 829-61

EXAMINER
TRICE, R

NIXON AND VANDERHYE P.C.
1100 NORTH GLEBE ROAD
8TH FLOOR
ARLINGTON, VA. 22201-4714

ART UNIT 2504
PAPER NUMBER 13

DATE MAILED: 09/02/92

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

This application has been examined Responsive to communication filed on 6/25/92 This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), — days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

- | | |
|---|--|
| 1. <input checked="" type="checkbox"/> Notice of References Cited by Examiner, PTO-892. | 2. <input type="checkbox"/> Notice re Patent Drawing, PTO-948. |
| 3. <input checked="" type="checkbox"/> Notice of Art Cited by Applicant, PTO-1449. | 4. <input type="checkbox"/> Notice of Informal Patent Application, Form PTO-152. |
| 5. <input type="checkbox"/> Information on How to Effect Drawing Changes, PTO-1474. | 6. <input type="checkbox"/> _____ |

Part II SUMMARY OF ACTION

1. Claims 1-15 are pending in the application.
Of the above, claims _____ are withdrawn from consideration.
2. Claims 1-7 have been cancelled.
3. Claims Band 15 are allowed.
4. Claims 9-12 are rejected.
5. Claims 13-14 are objected to.
6. Claims _____ are subject to restriction or election requirement.
7. This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. Formal drawings are required in response to this Office action.
9. The corrected or substitute drawings have been received on _____ Under 37 C.F.R. 1.84 these drawings are acceptable, not acceptable (see explanation or Notice re Patent Drawing, PTO-948).
10. The proposed additional or substitute sheet(s) of drawings, filed on _____ has (have) been approved by the examiner, disapproved by the examiner (see explanation).
11. The proposed drawing correction, filed on _____, has been approved, disapproved (see explanation).
12. Acknowledgment is made of the claim for priority under U.S.C. 119: The certified copy has been received not been received.
 been filed in parent application, serial no. _____; filed on _____
13. Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. Other

EXAMINER'S ACTION

PTOL-326 (Rev. 9-89)

SHC 001632

Art Unit 2504

Claim 9 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The "of" in line 16 should be deleted or another word inserted thereafter.

The phrase "and partially overlapping" is confusing. As written, it sounds as if the conductive piece overlays a portion where the conductive layer is and a portion where the conductive layer is not. As per the figures, the conductive layer is larger than the conductive piece such that the projection, normal to the substrate, of the edges of the conductive piece and the conductive layer do not overlap and the projection of the edge of the conductive piece is wholly inside of the projection of the edge of the conductive layer.

The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102

Art Unit 2504

of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. § 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 C.F.R. § 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 U.S.C. § 102(f) or (g) prior art under 35 U.S.C. § 103.

Claims 9 and 12 are rejected under 35 U.S.C. § 103 as being unpatentable over Takahara (2-55338).

Takahara teaches a LCD having orthogonal gate and signal buses with a TFT connected to each pixel electrode. Horizontally adjacent pixel electrodes are connectable via a laser link. The laser link comprises the pixel electrode, a insulator, a conductive piece and a conductive link between horizontally adjacent pixels. The conductive link goes over the signal bus.

It would have been obvious to one of ordinary skill in the liquid crystal art to placed the conductive link below the signal bus because the two placements are substantial functional equivalents of each other. Note, the TFT goes from a gate down to a gate up structure which is also obvious because the gate up and the gate down structure are substantial functional equivalents.

In regard to claim 9, all that is claimed is that the

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Art Unit 2504

conductive layer is to be connected to the pixel electrode.
Accordingly, this reference meets the claim.

Ukai et al. (5121236) shows devices similar to some of the
claims of the applicants.

The prior art made of record and not relied upon is
considered pertinent to applicant's disclosure.

NEW CITATIONS

2-79026 connection of horizontally adjacent pixels under a
signal line. See element 60.

2-193121 shows TFT connection of horizontally adjacent
pixels.

OLD CITATIONS

Tsukada et al. (4955697) shows the inherent parasitic
capacitors which are formed by a TFT.

Ukai et al. shows supplemental capacitors, one of which is
laser welded to connect it to the circuit.

Katayama et al. is the prior art improperly inserted into
the specification.

Claims 10-11 would be allowable if rewritten to overcome the
rejection under 35 U.S.C. § 112 and to include all of the
limitations of the base claim and any intervening claims.

SHC 001635

Serial No. 07/656845

-5-

Art Unit 2504


Claims 13-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 8 and 15 are allowable over the prior art of record.

Applicant's arguments with respect to claims 9 and 12 have been considered but are deemed to be moot in view of the new grounds of rejection.

Any inquiry concerning this communication should be directed to Ron Trice at telephone number (703) 308-4117.

Ron Trice
Patent Examiner
August 28, 1992


William L. Sikes
Supervisory Patent Examiner
Group Art Unit 2504

SHC 001636

656845

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13

NOTICE OF REFERENCES CITED

APPLICANT(S)

KANEMORI et al

U.S. PATENT DOCUMENTS

• I	DOCUMENT NO.							DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
	A	B	C	D	E	F	G					
	4	6	3	0	8	9	3	12/86	credelle et al	359	87	✓
	5	1	2	1	2	3	6	6/92	yKai et al	359	59	—

FOREIGN PATENT DOCUMENTS

• L	DOCUMENT NO.							DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHTS. DWG. PP. SPEC.	
	M	N	O	P	Q	R	S							
	2	1	9	3	1	2	1	7/90	JAPAN	—	359	59	—	—
	2	0	7	9	0	2	6	3/90	JAPAN	—	359	54	—	—
	2	0	5	5	3	3	8	2/90	JAPAN	—	359	59	—	—

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

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EXAMINER: TRICE DATE: 8/28/92

* A copy of this reference is not being furnished with this office action.
(See Manual of Patent Examining Procedure, section 707.05 (a).)



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Handwritten initials/signature

In re PATENT Application of

KANEMORI et al

Atty. Ref: 829-61

Serial No. 07/656,845

Group: 2504

Filed: February 19, 1991

Examiner: R. Trice

For: ACTIVE MATRIX DEVICE AND A METHOD OF
MANUFACTURING THE SAME

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* * * * *

JAN 11 1993

January 6, 1993 GROUP 2500

Honorable Commissioner of Patents
and Trademarks
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT
PURSUANT TO 37 CFR 1.97(c)

Sir:

Consideration of the Information Disclosure Statement submitted herewith pursuant to 37 CFR 1.97(c) is requested. Attention is directed to the attached copy of an EPO Search Report dated October 13, 1992 with respect to this disclosure and to a copy of each reference cited therein which is not a duplication of that which was previously cited in an Information Disclosure Statement filed on August 18, 1992 in the above-identified application. A listing of these additional newly cited references on a Form PTO-1449 is also provided herewith.

The references are considered relevant for the reasons succinctly stated in the attached Search Report.

SHC 001638



P.B. 2818 - Patentaan 2
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 TX 31851 epo nl
 FAX (070) 3 40 30 18

Europäisches
 Patentamt

Zweigstelle
 in Den Haag
 Recherchen-
 abteilung

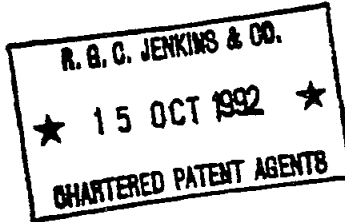
European
 Patent Office

Branch at
 The Hague
 Search
 division

Office européen
 des brevets

Département à
 La Haye
 Division de la
 recherche

Brown, Kenneth Richard
 R.G.C. Jenkins & Co.
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 GRANDE BRETAGNE



Datum/Date 13. 10. 92

Zeichen/Ref./Rif. J. 20540 EP	Anmeldung Nr./Application No./Demande n° // Patent Nr No./Brevet n° 91301303.3- -
Anmelder/Applicant/Demandeur//Patentinhaber/Propriétaire SHARP KABUSHIKI KAISHA	

COMMUNICATION

The European Patent Office herewith transmits

- the European search report
- the declaration under Rule 45 of the European Patent Convention
- the partial European search report under Rule 45 of the European Patent Convention
- the supplementary European search report concerning the international application number

relating to the above-identified European patent application; copies of the documents cited in the search report are enclosed.

The Search Division approved the following items, as submitted by the applicant:

- Abstract
- Title
- Figure
- The abstract was modified by the Search Division and the definitive text is attached to the present communication.
- The following figure will be published with the abstract, since the Search Division considers that it better characterises the invention than the one indicated by the applicant.

Figure:

- Additional copy(ies) of the documents cited in the European search report.



REFUND OF THE SEARCH FEE

If applicable under Art.10 of the Rules relating to fees, a separate communication from the Receiving Section on the refund of the search fee will be sent to you later.

EPO Form 1507 07.90				

SHC 001639



European Patent
Office

EUROPEAN SEARCH REPORT

Application Number

EP 91 30 1303

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. CL.5)
A	PATENT ABSTRACTS OF JAPAN, vol. 8, no. 21 (E-224), 28th January 1984; & JP-A-58 184 758 (SUWA SEIKOSHA) 28-10-1983 * Abstract *	1,8,9, 10,12, 15	G 02 F 1/136
A	PATENT ABSTRACTS OF JAPAN, vol. 13, no. 475 (P-950)[3823], 27th October 1989; & JP-A-1 186 916 (MATSUSHITA) 26-07-1989 * Abstract *	1,4,8	
D, P A	PATENT ABSTRACTS OF JAPAN, vol. 15, no. 5 (P-1149), 8th January 1991; & JP-A ² 254 423 (SHARP) 15-10-1990 * Abstract * & EP-A-372 898	1,4,5	
A	PATENT ABSTRACTS OF JAPAN, vol. 13, no. 245 (P-881), 8th June 1989; & JP-A-1 048 037 (MATSUSHITA ELECTRIC IND. CO) 22-02-1989 * Abstract *	9,10,12, 15	
A	PATENT ABSTRACTS OF JAPAN, vol. 13, no. 245 (P-881), 8th June 1989; & JP-A-1 048 038 (MATSUSHITA ELECTRIC IND. CO.) 22-02-1989 * Abstract *	9,10,12, 15	
The present search report has been drawn up for all claims			TECHNICAL FIELDS SEARCHED (Int. CL5)
Place of search THE HAGUE		Date of completion of the search 15-09-1992	Examiner WONGEL H.
CATEGORY OF CITED DOCUMENTS		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons A : technological background O : non-written disclosure P : intermediate document * : member of the same patent family, corresponding document	
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document			

EPO FORM 1503 (01.92) (P0401)

SHC 001640



CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

- All claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for all claims.
- Only part of the claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid.
- namely claims:
- No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions.

namely:

see sheet -B-

- All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.
- Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid.
- namely claims:
- None of the further search fees has been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims.
- namely claims:



LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims 1-8: An active matrix display device wherein the shape of a scanning branch line is adapted for being cut off by irradiation with light energy.
2. Claims 9-16: An active matrix display device comprising a conductive layer under the signal line and the pixel electrode for making a permanent connection between a defective pixel and the adjacent signal line.

ATTY. DOCKET NO.

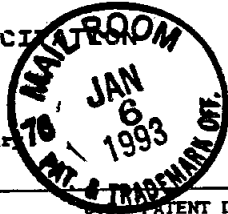
SERIAL NO.

829-61

07/656,845

INFORMATION DISCLOSURE CITE

(Use several sheets if necessary)



APPLICANT

Kanemori et al

FILING DATE

February 19, 1991

GROUP

2504

PATENT DOCUMENTS

*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
						RECEIVED JAN 11 1993 GROUP 2500

FOREIGN PATENT DOCUMENTS

	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
RT	1-048037	2/89	JAPAN				
RT	1-048038	2/89	JAPAN				

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

	PATENT ABSTRACTS OF JAPAN, vol. 13, no. 245 (P-881), 8th June 1989; & JP-A-1 048 037 (MATSUSHITA ELECTRIC IND. CO.) 22-02-1989
	PATENT ABSTRACTS OF JAPAN, vol. 13, no. 245 (P-881), 8th June 1989; & JP-A-1 048 038 (MATSUSHITA ELECTRIC IND. CO.) 22-02-1989

SHC 001643

Examiner

TRICE

Date Considered

4/29/93

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Front Abstracts of Japan

PUBLICATION NUMBER : JP1048037
 PUBLICATION DATE : 22-02-89
 ABSTRACT PUBLICATION DATE: 08-06-89
 ABSTRACT VOLUME : 013245
 APPLICATION DATE : 18-08-87
 APPLICATION NUMBER : JP870204650

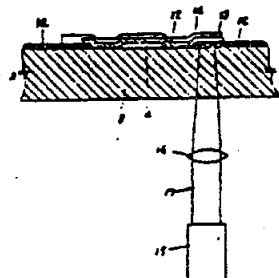
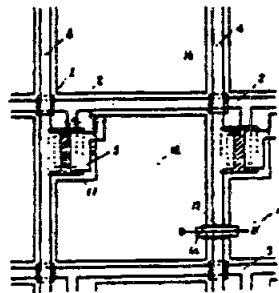
GROUP : P881

APPLICANT : MATSUSHITA ELECTRIC IND CO LTD

INVENTOR : TAKAHARA HIROSHI

INT.CL. : G02F1/133; G09F9/35;
 H01L21/82; H01L27/12

TITLE : ACTIVE MATRIX ARRAY



ABSTRACT : PURPOSE: To connect a picture element electrode and adjacent picture element electrode via a conductive connecting wiring and to correct the defect of an active matrix array by disconnecting a defective thin film TFT from picture element electrodes and projecting light of a UV wavelength to a 2nd insulator film consisting of an org. material thereby chemically decomposing the insulator film.

CONSTITUTION: The active matrix is used for a liquid crystal display panel and the 1st insulator film 12 is formed on gate and source signal lines 3, 4 formed between the 1st picture element electrode 1a and the 2nd picture element electrode 1c. The 2nd insulator film 13 consisting of the org. material is formed between the electrode 1c and the conductive connecting wiring 14 and the drain terminal 5 of the defective TFT is disconnected from the electrode 1a. A beam 17 is projected by a light projecting means 15 to the overlapped part of the electrode 1c and the insulator film 13. The chemical decomposition and thermal decomposition are induced in the insulator film 13 by the high energy of the UV region, by which the insulator film is evaporated or carbonized and the wiring 14 and the electrode 1c are connected.

Patent Abstracts of Japan

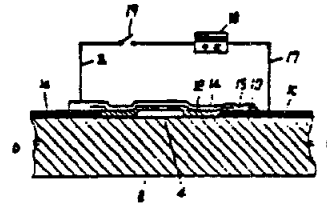
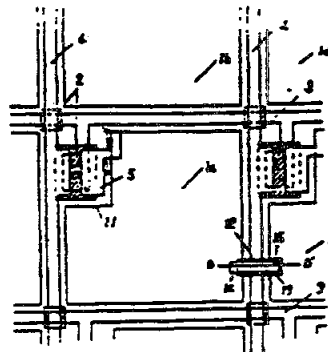
PUBLICATION NUMBER : JP1048038
 PUBLICATION DATE : 22-02-89
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 ABSTRACT VOLUME : 013245
 APPLICATION DATE : 18-08-87
 APPLICATION NUMBER : JP870204651
 GROUP : P881

APPLICANT : MATSUSHITA ELECTRIC IND CO LTD

INVENTOR : TAKAHARA HIROSHI

INT.CL. : G02F1/133; G09F9/35;
 H01L21/82; H01L27/12

TITLE : ACTIVE MATRIX ARRAY



ABSTRACT : PURPOSE:To correct the defect of an active matrix array by disconnecting a defective thin film transistor TFT from picture element electrodes and impressing a voltage between a conductive connecting wiring and the picture element electrode, thereby inducing dielectric breakdown between the insulating wiring and the picture element electrode and electrically connecting the picture element electrode and the adjacent picture element electrode via the connecting wiring.
 CONSTITUTION:The active matrix array is used for a liquid crystal panel and a 1st insulator film 12 is formed on gate and source signal wires 3, 4 formed between the 1st and 2nd picture element electrodes 1a and 1c. A 2nd insulator film 13 consisting of an inorg. material is formed between the electrode 1c and the conductive connecting wiring 14 to maintain electrical insulation. A drain terminal 5 of the defective TFT is disconnected from the electrode 1a and a probe 16 is brought into pressurized contact with the surface of the electrode 1a or the connecting wiring 14 and a probe 17 with the electrode 1c. The prescribed voltage from a voltage impressing means 18 is impressed to the electrodes via a switch 19 to break down the insulation of the insulator film 13 by which the connecting wiring 14 and the electrode 1c are electrically connected.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION of

KANEMORI et al

Atty. Ref: 829-61

Serial No. 07/656,845

Group: 2504

Filed: February 19, 1991

Examiner: R. Trice

2/23/93
A.S.

For: ACTIVE MATRIX DEVICE AND A
METHOD OF MANUFACTURING THE SAME

February 2, 1993

Honorable Commissioner of Patents
and Trademarks
Washington, D.C. 20231

RECEIVED
FEB 23 1993
GROUP 2500

AMENDMENT

Sir:

Responsive to the Official Action dated September 2, 1992
(for which petition is hereby made for two (2) months extension
of time), please amend the above-identified application as
follows:

IN THE CLAIMS:

Please amend claims 9 through 14 to read as follows:

Claim 9. (Thrice-Amended) An active matrix display device
comprising:

1 a pair of insulating substrates at least one of which is

light transmitting;
DS20076 02/23/93 07656845 14-1140 020 102 4.00CH

050 MS 02/22/93 07656845 1 102 144.00 CK

050 NS 02/22/93 07656845 1 116 360.00 CK

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SHC 001646

P1 scanning lines and signal lines arranged orthogonally on one of said pair of substrates; and

P1 pixel electrodes each connected to an adjacent scanning line and an adjacent signal line via a switching element,

P1 a conductive layer disposed under said adjacent signal line and said pixel electrode and extending therebetween;

P1 an insulating film interposed between said conductive layer and said adjacent signal line, and between said conductive layer and said pixel electrode, respectively; and

P1 a conductive piece formed between said pixel electrode and said insulating film and [partially] overlapping said conductive layer for facilitating a conductive connection between said conductive layer [of] and said pixel electrode, said conductive layer facilitating another conductive connection between said conductive layer and said adjacent signal line under a defective condition of said switching element.

²
10. (~~Twice Amended~~) An active matrix display device [according to claim 9,] comprising: a pair of insulating substrates at least one of which is light transmitting; scanning lines and signal lines arranged respectively orthogonally on one of said pair of substrates; and pixel electrodes each connected to an adjacent scanning line and an adjacent signal via a switching element,

1' a conductive layer disposed under said adjacent signal line and said pixel electrode and extending therebetween; an

insulating film interposed between said conductive layer and said adjacent signal line, and between said conductive layer and said pixel electrode, respectively; and a conductive piece formed between said pixel electrode and said insulating film and overlapping said conductive layer for facilitating a conductive connection between said conductive layer and said pixel electrode.

¶1 wherein said conductive layer is conductively connected to a scanning line adjacent to said scanning line connected to said pixel electrode and an anodic oxide film is formed on said conductive layer.

3
1. (~~Twice-Amended~~) An active matrix display device [according to claim 9,] comprising: a pair of insulating substrates at least one of which is light transmitting; scanning lines and signal lines arranged respectively orthogonally on one of said pair of substrates; and pixel electrodes each connected to an adjacent scanning line and an adjacent signal line via a switching element,

¶1 a conductive layer disposed under said adjacent signal line and said pixel electrode and extending therebetween; an insulating film interposed between said conductive layer and said adjacent signal line, and between said conductive layer and said pixel electrode, respectively; and a conductive piece formed between said pixel electrode and said insulating film and overlapping said conductive layer for facilitating a conductive

connection between said conductive layer and said pixel electrode, and

11) further comprising a supplemental capacitor electrode disposed opposite to said pixel electrode with said insulating film interposed therebetween, wherein said conductive layer is conductively connected to said supplemental capacitor electrode and an anodic oxide film is formed on said conductive layer.

12. (Thrice Amended) An active matrix display device comprising: a pair of insulating substrates at least one of which is light transmitting; scanning lines and signal lines arranged orthogonally on one of said pair of substrates; and pixel electrodes each connected to an adjacent scanning line and an adjacent signal line via a switching element,

a conductive layer disposed under said adjacent signal line and extending between a pair of adjacent pixel electrodes and connected to a scanning line adjacent to said scanning line connected to said pixel electrodes; an insulating film interposed between said conductive layer and said adjacent signal line, and between said [conducting] conductive layer and said pixel electrodes, respectively; and conductive pieces each formed between said insulating film and one of said pair of pixel electrodes and overlapping said conductive layer for facilitating conductive connections between said conductive layer and said pixel electrodes and between said conductive layer and said adjacent signal line.

⁷
~~13.~~ (Twice Amended) An active matrix display device
¹
[according to claim 12,] comprising: a pair of insulating substrates at least one of which is light transmitting; scanning lines and signal lines arranged orthogonally on one of said pair of substrates; and pixel electrodes each connected to an adjacent scanning line and an adjacent signal line via a switching element,

nted
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P1 a conductive layer disposed under said adjacent signal line and extending between a pair of adjacent pixel electrodes; an insulating film interposed between said conductive layer and said adjacent signal line, and between said conductive layer and said pixel electrodes, respectively; and conductive pieces each formed between said insulating film and one of said pair of pixel electrodes and overlapping said conductive layer for facilitating conductive connections between said conductive layer and said pixel electrodes, and

P1 wherein said conductive layer is conductively connected to a scanning line adjacent to said scanning line connected to said pixel electrode and an anodic oxide film is formed on said conductive layer.

⁸
~~14.~~ (Twice Amended) An active matrix display device
¹
[according to claim 12,] comprising: a pair of insulating substrates at least one of which is light transmitting; scanning lines and signal lines arranged orthogonally on one of said pair of substrates; and pixel electrodes each connected to an

adjacent scanning line and an adjacent signal line via a switching element,

p1 a conductive layer disposed under said adjacent signal line and extending between a pair of adjacent pixel electrodes; an insulating film interposed between said conductive layer and said adjacent signal line, and between said conductive layer and said pixel electrodes, respectively; and conductive pieces each formed between said insulating film and one of said pair of pixel electrodes and overlapping said conductive layer for facilitating conductive connections between said conductive layer and said pixel electrodes, and

p1 further comprising a supplemental capacitor electrode disposed opposite to said pixel electrode with said insulating film interposed therebetween, wherein said conductive layer is conductively connected to said supplemental capacitor electrode and an anodic oxide film is formed on said conductive layer.

and

REMARKS

Reconsideration and allowance of all of the claims of record, as presently amended, are respectfully requested.

Applicants appreciate the Examiner's indication that claims 8 and 15 are allowed and further indicating that claims 10, 11, 13 and 14 would be allowable if rewritten to overcome the rejection under 35 USC 112, second paragraph and/or rewritten in independent form. In this regard, claims 10 and 11 have been rewritten in independent form, as well as being modified to eliminate the words found objectionable by the Examiner. Additionally, claims 13 and 14 have been rewritten in independent form. In light of the above, it is submitted that these claims are also presently in condition for allowance.

As an additional matter, claims 9 and 12 have been modified to more particularly and distinctly claim that which applicants regard as their invention.

In light of the foregoing amendments and for the reasons detailed below, it is submitted that all of the claims of record, as presently amended, are in condition for allowance, and action to that end is solicited.

Independent claim 9 was rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim that which applicants regard as their invention. More specifically, the Examiner asserted that the superfluous "of" at line 16 should be deleted. Moreover, the Examiner asserted that the phrase "and partially overlapping" was confusing since the term implied that the conductive piece overlapped a portion of the conductive layer, as well as overlapping an area outside the conductive layer.

As will be noted, claim 9 has been amended to eliminate the word "of" which was inadvertently included in the claim as previously amended. As to the phrase "partially overlapping", although it is submitted that as illustrated in Figure 11, for example, the term adequately indicates that the conductive piece 35, for example, overlaps some but not all of element 34, the claim nevertheless has now been amended to eliminate the word "partially" and thus eliminate the interpretation placed on the former term by the Examiner. As presently amended, it is submitted that all of the terms found in independent claim 9 are clearly readable on the disclosure and that the artisan would not be confused by the terms of the claim when the claim is read in light of the disclosure. Note In re Moore, 439 F.2d 1232, 169 USPQ 236 (CCPA 1971).

Accordingly, it is submitted that claim 9 and, therefore, claims 10 and 11, which have been similarly amended, while rewriting them into independent form, are in full compliance with 35 USC 112, second paragraph, and that the rejection pertaining to claim 9 should be withdrawn.

Claims 9 and 12 were rejected under 35 USC 103 as being unpatentable over the Takahara patent document (2-55338). The Examiner was of the apparent view that the reference teaches that which is claimed except for the placement of the conductive link below the signal bus but that such a modification would have been obvious to thus meet the requirements broadly specified in the claims. Applicants respectfully traverse the rejection since even presuming *arguendo* that it would have been obvious to modify the Takahara reference in the manner urged by the Examiner that which is claimed would not result therefrom, particularly as presently amended.

Regarding claim 9, it will be noted that the claim has been amended to define an active matrix display which includes a conductive layer which facilitates not only the connection between the conductive layer and the pixel electrode but also facilitates an additional conductive connection between the conductive layer and an adjacent signal line when the switching element of Figure 11, for example, is defective.

Thus, for example, where an active matrix display device of the prior art included a defective switching element, the affected pixel might appear as a bright spot or a black spot. The beneficial results obtained by the disclosed and claimed exemplary embodiments, however, allows the pixel defect to be corrected to an indiscernible level (page 13, first full paragraph, for example) whereby the pixel may be connected by way of the source bus line 23 to thus exhibit an average brightness of the pixels arrayed along that line (page 29, first full paragraph, for example).

In contrast, Takahara does not teach or suggest an active matrix display device wherein the conductive layer is for the purpose of forming a connection between a pixel electrode and the adjacent signal line. That is to say, Takahara would teach connecting one pixel electrode to another under switch fault conditions whereby one pixel electrode would be electrically connected to another.

It is respectfully submitted that that which is taught or fairly suggested by the Takahara reference is structurally and functionally distinct from that which is specified in claim 9 for example. Moreover, it is submitted that that which is taught by Takahara with respect to the modifications to be performed under fault conditions would teach away from that which is disclosed and claimed herein. Accordingly, applicants

submit that the rejection as applied to claim 9, particularly as presently amended, is improper and should be withdrawn.

Regarding independent claim 12, which as may be seen from a consideration of applicants' Figures 15 and 19, for example, defines an active matrix display device with a conductive layer for facilitating conductive connections between the layer and a pair of pixel electrodes but additionally facilitates another conductive connection between the conductive layer and a scanning line adjacent the scanning line connected to the pixel electrode when a defective condition of the switching element exists. Additionally, it will be noted that claim 12 requires a connection between the conductive layer and a scanning line adjacent to the scanning line connected to the pixel electrodes. Thus, if the switching elements of either of the pixels is found defective, either of the affected pixel electrodes may be connected to the signal line so as to obtain the benefits noted, supra.

In contrast, Takahara does not teach or remotely suggest either the above noted structure or functions but merely teaches facilitating connections between pixel electrodes under fault conditions. Accordingly, it is submitted that the subject matter of claim 12 when considered as a whole, as required by the statute, is also not rendered obvious within the meaning of

Kanemori et al
Serial No. 07/656,845

- 12 -

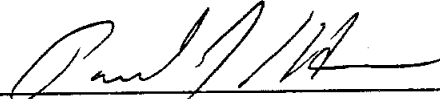
35 USC 103 by the teachings of Takahara. Thus, it is submitted that the rejection with regard to claim 12 should be withdrawn.

In light of the foregoing amendments and for the reasons detailed, supra, it is submitted that all of the claims remaining of record, particularly as presently amended, are in condition for allowance, and action to that end is solicited. If any issues remain to be resolved, the Examiner is urged to contact the attorney for the applicants at the telephone number listed below.

Respectfully submitted,

NIXON & VANDERHYTE P.C.

By:



Paul J. Henon
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SHC 001657



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Atty Dkt. 829-61
C# M#

In re PATENT APPLICATION of:

KANEMORI et al

Group Art Unit 2504

Serial No. 07/656,845

Examiner: R. Trice

Filed: February 19, 1991

Date: February 2, 1993

TITLE: ACTIVE MATRIX DEVICE AND A METHOD OF MANUFACTURING THE SAME

RECEIVED

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231

FEB 23 1993

Sir:

GROUP 2500

RESPONSE/AMENDMENT/LETTER

This is a response/amendment/letter in the above-identified application and includes an attachment which is hereby incorporated by reference and the signature below serves as the signature to the attachment in the absence of any other signature thereon.

Fees are attached as calculated below:

Total effective claims after amendment (8) minus highest number previously paid for (20) (at least 20) = (0) extra claims x \$22.	\$	0.00
Independent claims after amendment (8) minus highest number previously paid for (6) (at least 3) = (2) extra claims x \$74.	\$	144.00
If proper multiple dependent claims now added for first time, add \$230....	\$	
[X] Petition is hereby made for a 2 month time extension, fee enclosed (\$110 for 1 month; \$360 for 2 months; \$840 for 3 months)	\$	360.00
[] Terminal Disclaimer enclosed, add \$110	\$	
		SUBTOTAL..... \$ 504.00
If "small entity", enter half (1/2) of subtotal and subtract..	-\$	()
[] statement filed herewith		
[] Rule 56 Information Disclosure Statement Filing Fee (\$200)	\$	
		TOTAL ENCLOSED FEE... \$ 504.00

The Commissioner is hereby authorized to charge any deficiency in the fee(s) filed, or asserted to be filed, or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Account No. 14-1140. A duplicate copy of this sheet is attached.

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NIXON & VANDERHYE P.C.
By: Paul J. Henon, Reg. No. 33,626

Signature:

PJH:lmy

SHC 001658