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5   IN THE UNITED STATES DISTRICT COURT

6   FOR THE NORTHERN DISTRICT OF CALIFORNIA

7   SAN FRANCISCO DIVISION

8   U.S. Ethernet Innovations, LLC,   NO. C 10-03724 JW
                                                    NO. C 10-05254 JW
9   Plaintiff,   NO. C 10-03481 JW

10   v.   **SECOND CLAIM CONSTRUCTION
                                                    ORDER**
11   Acer, Inc., et al.,

12   _____/

13   AT&T, Inc., et al.,

14
                    Defendants.
15   _____/

16   Zions Bancorporation, et al.,

17   Plaintiffs,

18   v.

19   U.S. Ethernet Innovations, LLC,

20   Defendant.
     _____/
21

22   **I. INTRODUCTION**

23   On January 31, 2012, the Court issued its First Claim Construction Order[1] construing the

24   disputed terms from the Patents-in-Suit[2] that the parties identified as significant to resolving these

25   _____

26   [1] (Docket Item No. 586 in No. C 10-03724 JW.)

27   [2] The Patents-in-Suit are: U.S. Patent Nos. 5,307,459 (the "'459 Patent"); 4,434,872 (the
     "'872 Patent"); 5,732,094 (the "'094 Patent"); and 5,299,313 (the "'313 Patent") (collectively, the
28   "Patents-in-Suit").

1   related cases. In its First Claim Construction Order, the Court directed the parties to file

2   simultaneous supplemental briefs addressing certain terms that were not construed.

3   On May 3, 2012, the Court conducted its second <u>Markman</u> hearing. The parties have

4   tendered for construction three terms relating to the word "task," six means-plus-function terms and

5   ten terms relating to the word "logic." For continuity, the Court groups the terms in three categories

6   and addresses them in order.

7   <div align="center">**II. DISCUSSION**</div>

8   **A.**   <u>Limitations that Use the Word "Task"</u>

9   Claim 1 of the '094 Patent claims:[3]

10   A method for transmitting a frame of data from a host system through a
     network interface device to a network, comprising:

11   executing a frame transfer **task** initiated in the host system to transfer
     a frame to a buffer memory in the network interface device; and

12   executing a frame transmission **task** in the network interface device to
     initiate transmission of the frame from the buffer memory to the network in

13   parallel with the frame transfer **task** before the frame is completely
     transferred to the buffer memory.

14   Claim 39 of the '094 Patent claims:

15   A method for transmitting a frame of data from a host system through a network

16   interface device to a network, comprising:
         initiating a frame transfer **task** in the host system to transfer a frame to a

17   buffer memory in the network interface device;
         monitoring the frame transfer **task** in the network interface device; and

18   executing a medium access **task** in the network interface device to initiate
     access to the network, and upon access transmitting the frame from the buffer

19   memory to the network in parallel with the frame transfer **task** before the frame is
     completely transferred to the buffer memory.

20   **1.**   **"task"**

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22   The word "task" is a broad term, generally understood to mean any undertaking or piece of

23   work.[4] In its First Claim Construction Order, the Court found that the inventors' failure to define or

24   discuss in the words and phrases that include the word "task" arguably rendered the Claims invalid.

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26   [3] Unless otherwise indicated, all bold typeface is added by the Court for emphasis.

27   [4] <u>See, e.g.</u>, WEBSTER'S NEW TWENTIETH CENTURY DICTIONARY 1867 (2d ed. 1983).

28   <div align="center">2</div>

(See First Claim Construction Order at 19-20.) In their supplemental briefing, the parties request that the Court reconsider this finding.

In a section entitled, "Description of the Related Art," the inventors state:

Data communications systems are often based on the transmission of packets or frames of data that are composed by a sender. The packets or frames of data are designed to be compatible with the network protocol involved with the communications system. Thus, the sending system must compose the frames of data according to the network protocol prior to initiation of transmission of data. Often, a sending system will wait for acknowledgment [sic] that a frame of data sent to a network adapter has been transmitted prior to **performing a subsequent task**, such as composing a second frame of data to be transmitted.
* * *
Although transmit data buffers enable a sending system to compose and download a frame into the transmit data buffer, that then **attend to other tasks** while the network adapter attempts to transmit the frame, it suffers the disadvantage that transmission of a frame is delayed until the entire frame has been downloaded into the buffer. Thus transmit data buffer type systems improve host system efficiency at the expense of network throughput. Operations which are communication intensive suffer a performance downgrade.

('094 Patent, Col. 1:23-59.)

Upon reconsideration, the Court finds that a person of ordinary skill in the art would understand that the inventors use the word "task" to mean:

A process[5] that a sending system or an interface between the sending system and a network performs to compose or operate on a frame of data.

The Court turns to the particular "tasks" disclosed in the Claims of the '094 Patent.

2.   "frame transfer task"

Claim 1 of the '094 Patent claims:

A method for transmitting a frame of data from a host system through a network interface device to a network, comprising:
      executing a **frame transfer task** initiated in the host system to transfer a frame to a buffer memory in the network interface device . . .

The phrase "frame transfer task" is not expressly defined in Claim 1, nor is it specifically discussed in the written description. However, Claim 1 recites limitations on a "frame transfer task." According to the Claim, the "frame transfer task" must be initiated "in the host system." In

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[5] In each of the "task" phrases discussed below, the Court does not reach the issue of whether the lack of disclosure of what "process" qualifies as a "task" affects the validity of the Claim under the enablement requirement.

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addition, the "frame transfer task" must be performed to carry out a specific function, namely, "to

transfer a frame to a buffer memory."

In the written description, the inventors discuss an embodiment as follows:

> In operation, the host computer composes a frame of data to be transmitted on the
> network medium 42. The host computer 30 then identifies that frame through the
> host interface 31. The host interface coupled with the identifiers of the frame move
> data from the host computer 30 into the buffer 34 according to the description of the
> frame. The threshold logic 36 monitors the transfer of data into the buffer 34.

('094 Patent, Col. 4:52-59.)

During the prosecution of what was allowed as Claim 1, the inventors discussed the phrase

"frame transfer task."[6] In response to the Examiner's request for clarification, the inventors wrote:

"the frame transfer task includes composing an identifier for the frame to be transferred in the host,

loading the identifier in the network adapter, and then in response to the identifier, using resources

on the adapter card to control movement of the data into the buffer memory."[7] The process of

"composing an identifier for the frame," "loading the identifier in the network adapter," and

controlling "movement of the data into the buffer memory" are consistent with the Court's general

definition of a "task." Further, the Court does not find that the tasks enumerated for the Examiner

are exclusive.

Accordingly, the Court construes the phrase "frame transfer task" to mean:

**A process initiated by the host system to compose a frame of data or to perform
other operations on or with respect to the frame in order to transfer the frame to
the buffer memory in the network interface device.**

3.   "frame transmission task"

Claim 1 of the '094 Patent claims:

> A method for transmitting a frame of data from a host system through a
> network interface device to a network, comprising:

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[6] The Court considers the prosecution history, insofar as the Federal Circuit has instructed
that courts, when doing claim construction, "should also consider the patent's prosecution history, if
it is in evidence." See, e.g., Phillips v. AWH Corp., 415 F.3d 1303, 1317 (Fed. Cir. 2005) (citations
omitted).

[7] Response to Office Action dated April 7, 1997 at 5.

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executing a frame transfer task initiated in the host system to transfer a frame to a buffer memory in the network interface device; and
executing a **frame transmission task** in the network interface device to initiate transmission of the frame from the buffer memory to the network in parallel with the frame transfer task before the frame is completely transferred to the buffer memory.

As is the case with "frame transfer task," the phrase "frame transmission task" is not expressly defined in the claim, nor is it specifically discussed in the written description.

According to the claim language, a "frame transmission task" must be performed "in" the network interface device. It must be performed for a specific function, namely, "to initiate transmission of the frame from the buffer memory to the network in parallel with the frame transfer task."[8] Finally, the task must be performed in a specific sequence: "before the frame is completely transferred to the buffer memory." For convenience, the Court will refer to this sequence as "early transmission."

Although they are not specifically called "tasks," the written description describes processes that can be taken **in** the network interface device to **initiate early transmission**. For example, "processing a transmit descriptor":

According to another aspect of the present invention, the transmit buffer includes a transmit descriptor ring, and a transmit data buffer. The host system composes a frame by storing a transmit descriptor in the adapter managed transmit descriptor ring. The transmit descriptor may remain resident in the transmit descriptor ring for some time prior to an initiation of the data by the adapter, because of other transmit descriptors being processed ahead of a current descriptor, or other reasons. When the adapter begins **processing of a transit descriptor**, it **retrieves immediate data** from the descriptor itself, and **begins a download process** into the transmit data buffer of data identified in the descriptor. The threshold logic **determines the amount of immediate data** from the descriptor, and **monitors the downloading of data** of the frame into the download area. **When the combination meets the threshold, then actual transmission of the frame is initiated.** Thus, transmission of a frame may be initiated before the complete frame has been downloaded into the download area.

('094 Patent, Col. 2:28-46.)

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[8] The Court maintains the conclusion reached in its First Claim Construction Order that because the limitation recites that the step is performed "to initiate transmission of the frame from the buffer memory," the task itself must be completed or at least started before the transmission is begun.

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1   The "frame transmission task" limitation is further limited in dependent Claims 2, 3 and 4.

2   The protocols and conditions disclosed in these dependent Claims are consistent with pre-

3   transmission tasks performed on a frame.[9]

4   Accordingly, the Court construes the phrase "frame transmission task" to mean:

5   **A process that is performed in the network interface device that initiates
     transmission of the frame from the buffer memory to the network in parallel
6   with a frame transfer task and before the frame is completely transferred to the
     buffer memory.**

7   **4.   "medium access task"**

8   Claim 39 of the '094 Patent claims:

9   A method for transmitting a frame of data from a host system through a network
10   interface device to a network, comprising:
        initiating a frame transfer task in the host system to transfer a frame to a
11   buffer memory in the network interface device;
        monitoring the frame transfer task in the network interface device; and
12   executing a **medium access task** in the network interface device to initiate
     access to the network, and upon access transmitting the frame from the buffer
13   memory to the network in parallel with the frame transfer task before the frame is
     completely transferred to the buffer memory.

14   Like the other two "task" phrases, the phrase "medium access task" is not expressly defined

15   in Claim 1 and is not specifically discussed in the written description.

16   In the written description, the inventors discuss Figure 2, which is a functional block

17   diagram. Figure 2 contains a block labeled "Network Medium":

18   FIG 2 illustrates the functional components of the early transmit system according to
19   the present invention.
     * * *
20   The threshold logic makes the threshold determination and generates a signal as
     indicated by line 38 to transmit logic 39 including, for instance, **media access
21   control MAC logic** 31.
     * * *
22   In operation, the host computer composes a frame of date to be transmitted on the
     network medium 42. The host computer 30 then identifies that frame through the
23   host interface 31. The host interface coupled with the identifiers of the frame move
     data from the host computer 30 into the buffer 34 according to the description of the
24   frame. The threshold logic 36 monitors the transfer of data into the buffer 34. The
     threshold logic 36 monitors the transfer of data into the buffer 34, then the transmit

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26   [9] A dependent claim to Claim 1 must perform the function "to initiate [early] transmission."
     The Court leaves for later consideration the question of whether the dependent claims disclose tasks
27   that "initiate" early transmission.

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1 logic 39 is instructed to begin transmission of the frame. The transmit logic 39 then
2 begins retrieving data from buffer 34 to support transmission of the frame on the
   medium 42.

3 ('094 Patent, Col. 4:16-59.)

4 A person of ordinary skill in the art would understand that the inventors use the word

5 "medium" to refer to the carrier used by the network for transmitting data.

6 Further, the language of Claim 39 recites that the "medium access task" must be executed in

7 the network interface device and for a particular function, namely, "to initiate access to the

8 network."[10]

9 Accordingly, the Court construes the phrase "medium access task" to mean:

10 **A process that is performed in the network interface device that initiates access
   to the network based on the particular carrier medium or media of the network.**

11 **B.   Means-Plus-Function Terms**

12 The parties submit for construction six limitations that use a "means-plus-function" format.

13 The parties agree that these limitations are to be governed by 35 U.S.C. § 112 ¶ 6, but they disagree

14 as to the corresponding structures.

15 "[S]tructure disclosed in the specification is 'corresponding' structure only if the

16 specification or prosecution history clearly links or associates that structure to the function recited in

17 the claim." B. Braun Med., Inc. v. Abbott Labs., 124 F.3d 1419, 1424 (Fed. Cir. 1997). In other

18 words, the structure must be necessary to perform the claimed function. See Northrop Grumman

19 Corp. v. Intel Corp., 325 F.3d 1346, 1352 (Fed. Cir. 2003). The relevant structure is that which

20 corresponds to the recited function. See Chiuminatta Concrete Concepts, Inc. v. Cardinal Indus.,

21 Inc., 145 F.3d 1303, 1308-09 (Fed. Cir. 1998). Because the corresponding structure and its

22 equivalent is limiting, any corresponding structure disclosed in the specification should be clearly

23 identified. See Kahn v. General Motors Corp., 135 F.3d 1472, 1476 (Fed. Cir. 1998). However, the

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25 [10] The remainder of the language of Claim 39 recites a "task" that must also be performed in
26 the network interface device, namely, "upon access transmitting the frame from the buffer memory
   to the network in parallel with the frame transfer task before the frame is completely transferred to
27 the buffer memory." However, because the task is performed "upon access," it is not a task that
   "initiates access" and is thus not a "medium access task."

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1 written description need not explicitly describe the corresponding structure. See Atmel Corp. v.

2 Info. Storage Devices, Inc., 198 F.3d 1374, 1381-82 (Fed. Cir. 1999). If the written description

3 contains an implicit description that a person of ordinary skill in the art would recognize as

4 performing the recited function, the statutory requirement is satisfied. Id.

5   **1.**   **"means for comparing the counter to the threshold value in the alterable storage location and generating an indication signal to the host processor responsive to a**

6   **comparison of the counter and the alterable storage location"**

7 Claim 1 of the '459 Patent claims:

8   An apparatus for transferring a data frame between a network
transceiver, coupled with a network, and a host system which includes

9 a host processor and host memory, the apparatus generating an
indication signal to the host processor responsive to the transfer of the

10 data frame, with the host processor responding to the indication signal
after a period of time, comprising:

11   a buffer memory for storing the data frame;
network interface logic for transferring the data frame between the network

12 transceiver and the buffer memory;
host interface logic for transferring the data frame between the host system

13 and the buffer memory;
threshold logic for allowing the period of time for the host processor to

14 respond to the indication signal to occur during the transferring of the data frame,
wherein the threshold logic includes,

15   a counter, coupled to the buffer memory, for counting the amount of
data transferred to or from the buffer memory;

16   an alterable storage location containing a threshold value; and
means for comparing the counter to the threshold value in the

17 **alterable storage location and generating an indication signal to the host
processor responsive to a comparison of the counter and the alterable**

18 **storage location**.

19   The "means for comparing" has two functions: (1) "comparing the counter to the threshold

20 value in the alterable storage location"; and (2) "generating an indication signal to the host

21 processor." When dual functions must be performed by the "means," the patent document must

22 disclose either a single structure that performs both functions or multiple structures, each of which

23 performs one of the functions, but the multiple structures reasonably may be grouped together as

24 subcomponents of a larger component that performs both functions. See, e.g., Cardiac Pacemakers,

25 Inc. v. St. Jude Med., Inc., No. IP 96-1718-C H/G, 2000 WL 1902191, at *3 (S.D. Ind. Dec. 19,

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1 2000). Ungrouped individual components of an apparatus, each of which performs only one of the

2 functions, are not corresponding structure of a means that has dual functions.[11] Id.

3 As a preliminary matter, the Court observes that while the literal language of Claim 1 refers

4 to the function as being "for comparing the **counter** to the threshold value in the alterable storage

5 location," the Court finds that the inventors meant "for comparing **the value generated by** the

6 counter to the threshold value in the alterable storage location." Correspondingly, although the

7 Claim recites as a second function "generating an indication signal to the host processor responsive

8 to a comparison **of the counter** and **the alterable storage location**," the Court finds that the

9 inventors meant "for generating an indication signal to the host processor responsive to a

10 comparison of **the value generated by** the counter and **the value in the** alterable storage location."

11 **a. "the counter"**

12 Since both functions operate on a value generated by "the counter," the Court construes what

13 the inventors meant by "the counter."

14 An antecedent limitation of Claim 1 recites: "a counter coupled to the buffer memory, for

15 counting the amount of data transferred to or from the buffer memory." Thus, in order to serve as a

16 "counter" on which the "means" operates, the counter must be a mechanism for counting the amount

17 of data transferred to or from the buffer memory. The written description discloses at least two

18 types of devices that "count" data:

19 **b. "look-ahead threshold logic"**

20 FIG. 12a graphically show when in the reception of the data frame the look-ahead
threshold logic will generate an early receive indication. As can be seen from FIG.

21 12a, **look-ahead threshold logic determines how many bytes of frame has been
received** before generating an early receive indication. The look-ahead threshold

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25 [11] For example, if one individual component performs one of the dual functions and outputs a
signal to another individual component that performs the other function, this does not necessarily

26 mean that the two components reasonably may be grouped. However, if the two individual
components may reasonably be grouped as subcomponents on a larger individual component, the

27 larger component may serve as a corresponding structure because it would be capable of performing
both functions.

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logic contains an alterable storage location containing the look-ahead threshold number of bytes to be received before generating the early indication signal.

('459 Patent, Col. 29:59-67.)

c. "length-left threshold logic"

Alternatively, the length-left threshold logic will generate an early indication signal to the host depending upon how many bytes of the data frame remains [sic] to be received. FIG. 12b graphically shows the relationship of the generation of the receive complete signal relative to the reception of a data frame. While the look-ahead threshold logic can be implemented by counting the number of bytes received in the data frame and comparing it to a look-ahead threshold value, the length-left threshold logic is more complex because the length of the data frame must be defined before making comparisons to a threshold value. The **length-left threshold logic must determine the length of the data frame in order to determine if the length-left threshold value has been reached** on a real time basis for each data frame received.

('459 Patent, Col. 30:10-26.)

Although both types of logic count data, at this point the Court finds that only the look-ahead threshold logic performs the function of counting the amount of data transferred.[12]

d. "for comparing [the value generated by] the counter to the threshold value in the alterable storage location"

Having determined the "counter" on which the means must operate, the Court proceeds to determine what structure or structures, if any, perform the function of comparing the value generated by the counter to the threshold value in the alterable storage location. The written description and the drawings contain multiple references to a functional components called a "comparator." The Court finds that the block labeled 224 in Fig. 14 and 318 in Fig. 21 performs the function of comparing the first recited function.

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[12] For example, Fig. 23 shows a comparator 341 that performs a comparison between a "BYTES REMAIN" value and one of two threshold values, depending on whether the network adapter is still receiving the frame that is being transferred. ('459 Patent, Col. 37:59-38:8.) The "BYTES REMAIN" value, as its name implies, represents the amount of data remaining to be transferred, rather than "the amount of data transferred." The Court invites the parties to submit supplemental briefing with respect to whether any of these devices, some of which determine data *remaining* to be transferred, perform the function of counting the amount of data *transferred* to or from buffer memory.

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     e.   **"for generating an indication signal to the host processor responsive to a comparison of [the value generated by] the counter and [the value in] the alterable storage location"**

The second function that must be performed by the "means" is "generating an indication signal." Neither of the structures found above by the Court that perform the "comparing" function can perform the "generating an indication signal" function.

The Court finds that the functional components labeled "Interrupt Controller 60" shown in Fig. 4, together with "Early Rcv Control 225" in Fig. 14, perform the "generating an indication signal" function. However, these components cannot perform the "comparing" function. Thus, there is no single structure that is capable of performing the dual functions of the "means." In addition, the Court's attention has not been drawn to any intrinsic evidence that would lead the Court to find that a person of ordinary skill in the art would group these individual functional components into a single component.

Consequently, the Court declines to further construe Claim 1 of the '459 Patent and concludes that the lack of corresponding structure for the subject limitation renders Claim 1 arguably invalid. The Court invites the parties to address this matter in the course of further litigation in this case.

     2.   **"means . . . for monitoring the transferring of data of a frame to the buffer memory to make a threshold determination of an amount of data of the frame transferred to the buffer memory"**

Claim 1 of the '872 Patent claims:

> For a system transmitting frames of data across a communications medium; an apparatus comprising:
> > buffer memory for storing data of frames composed by the host computer for transmission on the communications medium;
> > means, having a host system interface, for transferring data of frames to the buffer memory;
> > **means, coupled with the buffer memory, for monitoring the transferring of data of a frame to the buffer memory to make a threshold determination of an amount of data of the frame transferred to the buffer memory;**
> > means, responsive to the threshold determination of the means for monitoring, for initiating transmission of the frame prior to transfer of all the data of the frame to the buffer memory from the host computer;
> > transmit logic, responsive to the means for initiating transmission, for retrieving data from the buffer memory and supplying retrieved data for transmission on the communications medium; and

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1   underrun control logic, which detects a condition in which the means for
2   transferring falls behind the transmit logic, and supplies a bad frame signal to the
     communications medium in response to the underrun condition.

3   The parties dispute the corresponding structure. In particular, the parties dispute whether

4   structural limitations relating to dependent claims are necessary to perform the recited function of

5   making "a threshold determination of an amount of data of the frame transferred to the buffer

6   memory."

7   Claim 2 recites:

8   The apparatus of claim 1, wherein the transmit buffer includes a transmit descriptor
     ring buffer and a transmit data buffer, the transmit descriptors including data
9   identifying data to be transmitted on the communications medium and **optionally
     immediate data**, and **wherein the means for monitoring includes the immediate
10   data in the threshold determination**.

11   The written description discusses two ways the network adapter transfers data: (1) as

12   "immediate" data in a transfer descriptor; and (2) as downloaded data via Direct Memory Access.

13   The preferred embodiment disclosed in the written description describes a network adapter that

14   monitors both of these data transfers and uses them to make the threshold determination.[13] However,

15   both the language of the claims and the written description make clear that the use of "immediate

16   data" is optional. For example, Claim 2 provides that "the transmit descriptors" include "data

17   identifying data to be transmitted on the communications medium and **optionally immediate data**."

18   Further, the written description provides that "[t]he XMIT AREA register is used by the host to

19   write transmit descriptors into the adapter. The transmit descriptors . . . include data that identifies

20   data to be compiled and transmitted as a frame, and **may include immediate data**."[14] Therefore, the

21   use of "immediate data" is not a required feature of the invention, which means that the monitoring

22   of such data is not a necessary element of Claim 1.

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24   [13] ('872 Patent, Col. 21:12-26 (stating that "XMIT START THRESH provides for an early
     start of transmission," and explaining that the "XMIT START THRESH register is used to specify
     the number of transmit bytes that must reside on the adapter before it will start transmission. . . . The
25   number of bytes considered to be available is the **sum of the immediate data** written to XMIT
     AREA by the host **and** those **bytes transferred** to the transmit data buffers in the adapter **using** bus
26   master **DMA operations**.").)

27   [14] ('872 Patent, Col. 12:49-53.)

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The Court finds that the corresponding structure for the "means . . . for monitoring" includes the following:

The "11bit counter 300" in Fig. 11, the "Start Thresh Reg 320" in Fig. 12, and the "Download Compare 321" in Fig. 12, and the equivalents thereof.

3.   "host interface means, sharing the host address space with the host, for managing data transfers between the host address space and the buffer memory in operations transparent to the host system"

Claim 1 of the '313 Patent claims:

An apparatus for controlling communication between a host system and a network transceiver coupled with a network, wherein the host system includes a host address space, comprising:
        a buffer memory outside of the host address space;
        host interface means, sharing the host address space with the host, for managing data transfers between the host address space and the buffer memory in operations transparent to the host system; and
        network interface means, coupled with the network transceiver, for managing data transfers between the buffer memory and the network transceiver.

The parties dispute the corresponding structure. In particular, the parties dispute whether the function of "managing data transfers between the host address space and the buffer memory in operations transparent to the host system" necessarily includes the function of remapping a section of the host address space in the host system to the buffer memory.

The written description repeatedly and consistently states that the host interface logic manages the transfer of data between the host address space and the buffer memory "in operations transparent to the host system" by mapping a specific range of addresses in the host address space to the buffer memory. For instance, the Abstract refers to "host interface logic emulating memory mapped registers in the host address space, for transferring data between the host address space and the buffer memory." In the Summary of the Invention, the inventors explain that access to the buffer memory is accomplished by automatically remapping the dedicated memory mapped page in the host address space into the buffer memory:

The present invention provides a network interface controller which controls communication between a host system and a network transceiver coupled to a network which comprises a buffer memory outside of the host address space in which receive and transmit buffers are managed, **host interface logic responsive to a prespecified range of host addresses**, like memory mapped registers in the host address space, **for mapping data between the host address space and the buffer**

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memory . . . Because the host interface logic and network interface logic manage accesses to the buffer memory, the host system is able to access the multiple data buffers for transmitting and receiving data through a limited prespecified address range. **The dedicated memory mapped page in host address space is automatically remapped through the host interface logic into the buffer memory in operations that are transparent to the host**.

('313 Patent, Col. 1:61-2:14.)

Moreover, the written description discusses embodiments of the host interface that use this mapping technique to transfer data from host address space to the buffer memory in operations that are transparent to the host. For example, the '313 Patent shows in Fig. 4 the transparent mapping of host address space to the buffer memory:

FIG. 4 provides a simplified map of the adapter interface host address block 101. The addresses within this block appear to the host like memory mapped registers in a continuous 8K block of the host address space in a preferred system. . . . Although the "registers" are memory mapped to an arbitrary prespecified block of host address space, none of the reads or writes performed by the host system to these registers actually directly access the adapter memory. Rather, **the accesses to the memory mapped space are interpreted by the host interface logic 104 transparent to the host system**. Thus, the memory in the adapter is independent of the host address space and of host management. FIG. 4 provides an overview mapping of the adapter interface host address space used for accessing these registers.

('313 Patent, Col. 19-39.)

Therefore, the Court finds that the memory mapping function is essential to the management of data transfer between the host address space and the buffer memory "in operations performed independently of management by the host system," as it is disclosed in the '313 Patent.[15]

Plaintiff contends that since the mapping function is omitted from the "host interface means" of independent Claim 1, and instead is claimed in subsequent dependent claims, the doctrine of claim differentiation[16] dictates that it cannot be a limitation of Claim 1.[17] However, the Court finds

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[15] In its First Claim Construction Order, the Court construed the function "host interface means" as "managing data transfers between address spaces on the host system bus and the buffer memory in operations performed independently of management by the host system." (First Claim Construction Order at 10-11.)

[16] Under the doctrine of claim differentiation, "each claim in a patent is presumptively different in scope." Wenger Mfg., Inc. v. Coating Mach. Sys., Inc., 239 F.3d 1225, 1233 (Fed. Cir. 2001) (citation omitted). However, as the Federal Circuit has explained, claim differentiation is not a "hard and fast rule of construction." Id. (citation omitted). In particular, the doctrine does not

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1 that this contention is misguided. As discussed above, the specification of the '313 Patent clearly

2 and repeatedly indicates that the mapping function is what allows the host interface to transfer data

3 from the host system to the buffer memory "in operations that are transparent to the host." The

4 specification does not disclose any other embodiments that accomplish that task. Therefore, despite

5 the fact that the mapping function is claimed in subsequent dependent claims, the Court finds that it

6 is part of claim 1.

7   Accordingly, the Court finds that the corresponding structures for the "host interface means"

8 in Claim 1 of the '313 Patent are:

9   **"Host descriptor logic 150" and "download DMA logic 151" as shown in Fig. 9, "transmit descriptor 107" as shown in Fig. 3, "transfer descriptor logic 108" and**

10   **"upload DMA logic 108" as shown in Fig. 3, and the equivalents thereof.**

11   **4.   "host interface means, sharing host address space including a prespecified block of host addresses of limited size defining a first area and a second area, and**

12   **coupled with the buffer memory, for mapping data addressed to the first area into the transmit buffer, mapping data in the receive buffer into the second area,**

13   **and uploading data from the receive buffer to the host"**

14 Claim 13 of the '313 Patent provides:

15   An apparatus for controlling communication between a host system and a network transceiver coupled with a network, wherein the host system includes a host address

16   space, comprising:
        a buffer memory outside of the host address space, including a transmit buffer

17   and a receive buffer;
        host interface means, sharing host address space including a prespecified

18   **block of host addresses of limited size defining a first area and a second area, and coupled with the buffer memory, for mapping data addressed to the first**

19   **area into the transmit buffer, mapping data in the receive buffer into the second area, and uploading data from the receive buffer to the host**; and

20   network interface means, coupled with the network transceiver and the buffer memory, for transferring data from the transmit buffer to the network transceiver and

21   mapping data into the receive buffer from the network transceiver.

22 The parties dispute the corresponding structure.

23

24

25

26 necessarily require that "means-plus-function limitations must be interpreted without regard to other claims." Id.

27   [17] (See Docket Item No. 597 at 90-92.)

28   15

1   The "host interface means" performs three functions: (1) "mapping data addressed to the first

2 area into the transmit buffer"; (2) "mapping data in the receive buffer into the second area"; and (3)

3 "uploading data from the receive buffer to the host."

4   With regard to the first function of "mapping data addressed to the first area into the transmit

5 buffer," the written description of the '313 Patent recites an XMIT AREA register that is used by the

6 host to write transmit descriptors into the adapter by mapping:

7   The XMIT AREA register is used by the host to write transmit descriptors into the adapter.
        The transmit descriptors . . . include data that identifies data to be compiled and transmitted
8   as a frame, and may include immediate data. The XMIT AREA at offset 0010 (hex) is
        approximately 2K bytes in size. **This data is mapped into a transmit descriptor ring in**
9   **the independent adapter memory** as described below.[18]

10   With regard to the second function of "mapping data in the receive buffer into the second

11 area," the written description of the '313 Patent recites: "The transfer descriptor logic maps transfer

12 descriptors from the host system to the transfer descriptor buffer." ('313 Patent, Col. 2:46-47.)

13 Also, the written description recites an XFER AREA through which transfer descriptors are written

14 into the buffer memory: "The XFER AREA at offset 0800 (hex) in the adapter interface host address

15 block is a buffer of approximately 1K byte through which transfer descriptors are written into the

16 independent memory of the adapter." ('313 Patent, Col. 10:55-58.)

17   With regard to the third function of "uploading data from the receive buffer to the host," the

18 written description of the '313 Patent recites: "the upload logic is responsive to the transfer

19 descriptors in the transfer descriptor buffer, for transferring data from the receive ring buffer into

20 memory in the host system." ('313 Patent, Col. 2:48-51.) Further, the written description recites:

21 "The upload DMA module 57 performs data transfers from the receive buffer through the RAM

22 interface 50 to the host system." ('313 Patent, Col. 8:65-66.)

23   Thus, there in no single structure that is capable of performing all three functions. The

24 Court's attention has not been drawn to anything in the intrinsic evidence that would lead the Court

25

26

27   [18] ('313 Patent, Col. 10:46-54.)

28
                                    16

1 to find that a person of ordinary skill in the art would group these individual functional components

2 into a single component.

3   Consequently, the Court declines to further construe Claim 13 of the '313 Patent and

4 concludes that the lack of corresponding structure renders Claim 13 of the '313 Patent arguably

5 invalid. The Court invites the parties to address this matter in the course of further litigation in this

6 case.

7   **5.   "network interface means, coupled with the network transceiver, for managing
            data transfers between the buffer memory and the network transceiver"**

8
      Claim 1 of the '313 Patent provides:

9
            An apparatus for controlling communication between a host system and a network
10   transceiver coupled with a network, wherein the host system includes a host address
            space, comprising:
11   a buffer memory outside of the host address space;
                  host interface means, sharing the host address space with the host, for
12   managing data transfers between the host address space and the buffer memory in
            operations transparent to the host system; and
13   **network interface means, coupled with the network transceiver, for
            managing data transfers between the buffer memory and the network
14   transceiver**.

15   The parties dispute the corresponding structure.

16   The written description of the '313 Patent discloses that the "network interface logic 104"

17 shown in Fig. 3 "manages transfers of data from buffers in the independent memory 103 and the

18 network transceiver 105." ('313 Patent, Col. 9:55-59.) The written description further states:

19   The network interface logic 104 includes transmit DMA logic, (generally 109) and receive
            DMA logic (generally 110). The transmit DMA logic 109 is responsive to descriptors stored
20   in the adapter memory 103, as described below, for moving data out of the independent
            adapter memory 103 to the network transceiver 105. Similarly, the receive DMA logic 110
21   is responsible for moving data from the transceiver 105 into the independent adapter memory
            103.[19]

22
      Accordingly, the Court finds that the corresponding structures for the "network interface
23
    means" in Claim 1 of the '313 Patent includes:

24
      In Figure 3, Network interface logic 104, and its equivalents.
25

26 _____

27   [19] ('313 Patent, Col. 10:3-11.)

28   17

6.   **"network interface means, coupled with the network transceiver and the buffer memory, for transferring data from the transmit buffer to the network transceiver and mapping data into the receive buffer from the network transceiver"**

Claim 13 of the '313 Patent provides:

> An apparatus for controlling communication between a host system and a network transceiver coupled with a network, wherein the host system includes a host address space, comprising:
>   a buffer memory outside of the host address space, including a transmit buffer and a receive buffer;
>   host interface means, sharing host address space including a prespecified block of host addresses of limited size defining a first area and a second area, and coupled with the buffer memory, for mapping data addressed to the first area into the transmit buffer, mapping data in the receive buffer into the second area, and uploading data from the receive buffer to the host; and
>   **network interface means, coupled with the network transceiver and the buffer memory, for transferring data from the transmit buffer to the network transceiver and mapping data into the receive buffer from the network transceiver**.

The parties dispute the corresponding structure.

The Court finds that the corresponding structure for "network interface means" in Claim 13 is the same as the corresponding structure identified by the Court for the "network interface means" in Claim 1, as discussed above.[20]

C.   Terms Relating to the Phrase "Logic for"

The parties submit ten "logic for" terms for construction.[21] Here, the parties' primary dispute is whether these "logic for" terms should be governed by 35 U.S.C. § 112 ¶ 6.

Title 35 U.S.C. § 112 ¶ 6 provides that "[a]n element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure,

---

[20] In particular, the Court observes that the recited function for "network interface means" in Claim 13 of the '313 Patent differs only slightly from that of the same term in Claim 1. Moreover, because the '313 Patent discloses only a single embodiment for both recited functions, the Court finds the corresponding structures for "network interface means" in Claim 13 to be the same as in Claim 1.

[21] These terms include such phrases as "**threshold logic for** allowing the period of time for the host processor to respond to the indication signal to occur during the transferring of the data frame"; "**host interface logic for** transferring the data frame between the host system and the buffer memory"; and "**receive logic for** mapping received data from the network transceiver to the buffer memory." For convenience, and because all but one of the terms include the words "logic for," the Court refers to them as the "logic for" terms.

1 material, or acts in support thereof." The use of the word "means" in a claim element creates a

2 presumption that § 112 ¶ 6 applies, while the failure to use the word "means" creates a presumption

3 that § 112 ¶ 6 does not apply. Personalized Media Commc'ns, LLC v. Int'l Trade Comm'n, 161

4 F.3d 696, 703-04 (Fed. Cir. 1998) (citations omitted). A party seeking to overcome the presumption

5 that § 112 ¶ 6 does not apply bears the burden of demonstrating that the claim fails to "recite

6 sufficiently definite structure" or recites a "function without reciting sufficient structure for

7 performing that function." Linear Tech. Corp. v. Impala Linear Corp., 379 F.3d 1311, 1319-20 (Fed.

8 Cir. 2004) (citations omitted). "To help determine whether a claim term recites sufficient structure,"

9 courts examine whether the term "has an understood meaning in the art." Id. at 1320 (citation

10 omitted). In making this determination, the court may look to both intrinsic evidence and relevant

11 extrinsic evidence, such as technical dictionaries. See id.; see also Personalized Media, 161 F.3d at

12 704-05.

13 Here, since the word "means" is not used in the "logic for" terms, there is a rebuttable

14 presumption that § 112 ¶ 6 does not apply. Personalized Media, 161 F.3d at 704. Accordingly, the

15 Court considers whether Defendants meet their burden of demonstrating that the claim elements

16 involving the "logic for" terms fail to recite sufficient structure, and in particular considers whether

17 the "logic for" terms have "understood meaning[s] in the art." Linear Tech., 329 F.3d at 1319-20.

18 Upon review, the Court finds that the ten "logic for" terms have understood meanings in the

19 art. In particular, the Court finds that technical dictionaries, "which are evidence of the

20 understandings of persons of skill in the technical arts,"[22] indicate that the word "logic," as used in

21 the context of the "logic for" terms in dispute here, connotes "circuitry."[23] The Federal Circuit has

22 made clear that "circuit" is a "structure-connoting term," which, when "coupled with a description of

23 the circuit's operation," will generally convey "sufficient structural meaning" to persons of ordinary

24

25 [22] Linear Tech., 379 F.3d at 1320.

26 [23] See, e.g., MCGRAW-HILL DICTIONARY OF ELECTRONICS AND COMPUTER TECHNOLOGY
   308 (3d ed. 1984) (explaining that "logic" is a "[g]eneral term for the various types of . . . circuits
27 used to perform problem-solving functions in a digital computer").

28

1 skill in the art such that § 112 ¶ 6 will not apply. Linear Tech., 379 F.3d at 1320. Likewise, the

2 word "logic," when used as the Court finds it is used here–namely, to connote "circuitry"–is also,

3 and for the same reasons, a structure-connoting term. Moreover, the Court finds that each of the

4 disputed "logic for" terms is associated with a description of the operation of the relevant circuit, and

5 that these descriptions convey sufficient structural meaning to persons of ordinary skill in the art

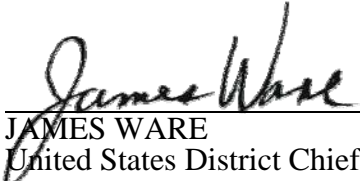6 such that § 112 ¶ 6 does not apply.

7   Accordingly, the Court finds that the disputed "logic for" terms are not governed by 35

8 U.S.C. § 112 ¶ 6.

9   **III. CONCLUSION**

10   The Court has construed the disputed phrases as tendered by the parties in their Supplemental

11 Briefs.

12   Upon the Court's imminent retirement,[24] the case will be reassigned in due course.[25]

15 Dated: August 29, 2012

                                                  JAMES WARE
16   United States District Chief Judge

_____

24 [24] On April 28, 2012, Chief Judge Ware announced that he plans to "retire in August 2012 as
25 the terms of his current law clerks come to an end." See Chief Judge Ware Announces Transition,
    available at http://www.cand.uscourts.gov/news/82.

26 [25] Accordingly, the Court DENIES Intel's Motion to Schedule a Further Case Management
    Conference as premature at this time as the new judge will set up a further conference upon
27 reassignment. (See Docket Item No. 632.)

28   20

THIS IS TO CERTIFY THAT COPIES OF THIS ORDER HAVE BEEN DELIVERED TO:

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Dated: August 29, 2012   **Richard W. Wieking, Clerk**

                                                     **By: /s/ JW Chambers   **
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                                                           Courtroom Deputy