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IN THE UNITED STATES DISTRICT COURT  
FOR THE NORTHERN DISTRICT OF CALIFORNIA  
SAN FRANCISCO DIVISION

U.S. Ethernet Innovations, LLC,  
Plaintiff,

NO. C 10-03724 JW  
NO. C 10-05254 JW  
NO. C 10-03481 JW

v.

**FIRST CLAIM CONSTRUCTION  
ORDER**

Acer, Inc., et al.,

\_\_\_\_\_ /

AT&T, Inc., et al.,

Defendants.

\_\_\_\_\_ /

Zions Bancorporation, et al.,

Plaintiffs,

v.

U.S. Ethernet Innovations, LLC,

Defendant.

\_\_\_\_\_ /

**I. INTRODUCTION**

U.S. Ethernet Innovations, LLC (“Plaintiff”) brings this action against a number of companies<sup>1</sup> (collectively, “Defendants”), alleging infringement of U.S. Patent Nos. 5,307,459 (the

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<sup>1</sup> For ease of reference, the Court divides Defendants into three categories: (1) the companies that supply the semiconductor chips that are incorporated into the accused products (the “Chip Supplier Defendants”), the original equipment manufacturers that make and sell the accused computer products (the “OEM Defendants”), and the companies that use the computer products (the “Retailer Defendants”). The Chip Supplier Defendants include Atheros Communications, Inc. (“Atheros”), Intel Corporation (“Intel”), Marvell Semiconductor, Inc. (“Marvell”) and NVIDIA

1 '459 Patent); 4,434,872 (the '872 Patent); 5,732,094 (the '094 Patent); and 5,299,313 (the '313)  
2 (collectively, the "Patents-in-Suit"). The Patents-in-Suit pertain to network interface adapters.  
3 Plaintiff alleges that Defendants infringe the Patents-in-Suit by manufacturing, using and selling  
4 certain semiconductor chips, motherboards and computer products.

5 On October 21, 2011, the Court conducted a hearing in accordance with Markman v.  
6 Westview Instruments, Inc.,<sup>2</sup> to construe language of the asserted claims over which there is a  
7 dispute. This First Claim Construction Order sets forth the Court's construction of the disputed  
8 words and phrases.

## 9 **II. STANDARDS AND PROCEDURES FOR CLAIM CONSTRUCTION**

### 10 **A. General Principles of Claim Construction**

11 Claim construction is a matter of law, to be decided exclusively by the Court. Markman, 517  
12 U.S. at 387. In accordance with the Patent Local Rules of the Northern District, the parties submit  
13 their joint selection of the ten disputed terms that are significant in resolving the case as well as their  
14 proposed definitions for construction. See Patent L.R. 4-3. After the Markman hearing and upon  
15 consideration of the parties' briefs, the Court issues an order construing the meaning of the disputed  
16 terms. The Court's construction becomes the legally operative meaning of the disputed terms that  
17 governs further proceedings in the case. See Chimie v. PPG Indus., Inc., 402 F.3d 1371, 1377 (Fed.  
18 Cir. 2005). Although greater weight should always be given to the intrinsic evidence,<sup>3</sup> claim  
19 construction is a fluid process in which the Court may consider a number of extrinsic sources of

20 \_\_\_\_\_  
21 Corporation ("NVIDIA"). The OEM Defendants include Acer, Inc.; Acer America Corporation;  
22 Apple, Inc.; ASUS Computer International; ASUSTeK Computer, Inc.; Dell, Inc.; Fujitsu Ltd.;  
23 Fujitsu America, Inc.; Gateway, Inc.; Hewlett Packard Co.; Sony Corporation; Sony Corporation of  
24 America; Sony Electronics Inc.; Toshiba Corporation; Toshiba America, Inc.; and Toshiba America  
25 Information Systems, Inc. The Retailer Defendants include AT&T Mobility, LLC; Barnes & Noble,  
26 Inc.; Claire's Boutiques, Inc.; J.C. Penney Company, Inc.; Sally Beauty Holdings, Inc.; Ann Taylor  
27 Stores Corporation; Ann Taylor Retail, Inc.; Harley-Davidson, Inc.; Harley-Davidson Motor  
28 Company, Inc.; Kirkland's Inc.; Kirkland's Stores, Inc.; Macy's, Inc.; Macy's Retail Holdings, Inc.;  
Macy's West Stores, Inc.; New York & Company, Inc.; Lerner New York, Inc.; Radioshack  
Corporation; Rent-A-Center, Inc.; and The Dress Barn, Inc.

26 <sup>2</sup> 517 U.S. 370 (1996).

27 <sup>3</sup> Phillips v. AWH Corp., 415 F.3d 1303, 1324 (Fed. Cir. 2005).

1 evidence, so long as they do not contradict the intrinsic evidence. See Vitronics Corp. v.  
2 Conceptronic, Inc., 90 F.3d 1576, 1582-83 (Fed. Cir. 1996).

3 **B. Construction from the Viewpoint of an Ordinarily Skilled Artisan**

4 A patent’s claims define the scope of the patent: the invention that the patentee may exclude  
5 others from practicing. Phillips, 415 F.3d at 1312. The Court generally gives the patent’s claims  
6 their ordinary and customary meaning. In construing the ordinary and customary meaning of a  
7 patent claim, the Court does so from the viewpoint of a person of ordinary skill in the art at the time  
8 of the invention, which is considered to be the effective filing date of the patent application. Thus,  
9 the Court seeks to construe the patent claim in accordance with what a person of ordinary skill in the  
10 art would have understood the claim to have meant at the time the patent application was filed. This  
11 inquiry forms an objective baseline from which the Court begins its claim construction. Id. at 1313.

12 The Court proceeds from that baseline under the premise that a person of ordinary skill in the  
13 art would interpret claim language not only in the context of the particular claim in which the  
14 language appears, but also in the context of the entire patent specification of which it is a part.  
15 Phillips, 415 F.3d at 1313. Additionally, the Court considers that a person of ordinary skill in the art  
16 would consult the rest of the intrinsic record, including any surrounding claims, the drawings and the  
17 prosecution history, if it is in evidence. Id.; see also Teleflex, Inc. v. Fiso N. Am. Corp., 299 F.3d  
18 1313, 1324 (Fed. Cir. 2002). In reading the intrinsic evidence, a person of ordinary skill in the art  
19 would give consideration to whether the disputed term is a term commonly used in lay language, a  
20 technical term, or a term defined by the patentee.

21 **C. Commonly Used Terms**

22 In some cases, disputed claim language involves a commonly understood term that is readily  
23 apparent to the Court. In such a case, the Court considers that a person of ordinary skill in the art  
24 would give the term its widely accepted meaning, unless a specialized definition is stated in the  
25 patent specification or was stated by the patentee during prosecution of the patent. In articulating  
26 the widely accepted meaning of such a term, the Court may consult a general purpose dictionary.  
27 Phillips, 415 F.3d at 1314.

1 **D. Technical Terms**

2 If a disputed term is a technical term in the field of the invention, the Court considers that  
3 one of skill in the art would give the term its ordinary and customary meaning in that technical field,  
4 unless a specialized definition is stated in the specification or during prosecution of the patent.  
5 Phillips, 415 F.3d at 1314. In arriving at this definition, the Court may consult a technical art-  
6 specific dictionary or invite the parties to present testimony from experts in the field on the ordinary  
7 and customary definition of the technical term at the time of the invention. Id.

8 **E. Defined Terms**

9 It is well established that a patentee is free to act as his or her own lexicographer. See, e.g.,  
10 Process Control Corp. v. HydReclaim Corp., 190 F.3d 1350, 1357 (Fed. Cir. 1999). Acting as such,  
11 the patentee may use a term differently than a person of ordinary skill in the art would understand it,  
12 without the benefit of the patentee's definition. Vitronics Corp., 90 F.3d at 1582. Thus, the Court  
13 examines the claims and the intrinsic evidence to determine if the patentee used a term with a  
14 specialized meaning.

15 The Court regards a specialized definition of a term stated in the specification as highly  
16 persuasive of the meaning of the term as it is used in a claim. Phillips, 415 F.3d at 1316-17.  
17 However, the definition must be stated in clear words which make it apparent to the Court that the  
18 term has been defined. See id.; Vitronics Corp., 90 F.3d at 1582. If the definition is not clearly  
19 stated or cannot be reasonably inferred, the Court may decline to construe the term pending further  
20 proceedings. Statements made by the patentee in the prosecution of the patent application as to the  
21 scope of the invention may be considered when deciding the meaning of the claims. Microsoft  
22 Corp. v. Multi-Tech Systems, Inc., 357 F.3d 1340, 1349 (Fed. Cir. 2004). Accordingly, the Court  
23 may also examine the prosecution history of the patent when considering whether to construe the  
24 claim term as having a specialized definition.

25 In construing claims, it is for the Court to determine the terms that require construction and  
26 those that do not. See U.S. Surgical Corp. v. Ethicon, Inc., 103 F.3d 1554, 1568 (Fed. Cir. 1997).  
27 Moreover, the Court is not required to adopt a construction of a term, even if the parties have  
28

1 stipulated to it. Pfizer, Inc. v. Teva Pharm. USA, Inc., 429 F.3d 1364, 1376 (Fed. Cir. 2005).

2 Instead, the Court may arrive at its own constructions of claim terms, which may differ from the  
3 constructions proposed by the parties.

4 **III. DISCUSSION**

5 Pursuant to the Patent Local Rules, the parties have tendered ten terms that they have  
6 identified as significant to resolving these cases. The Court will discuss the terms in relation to the  
7 first issued patent in which they appear.<sup>4</sup>

8 **A. The ‘313 Patent**

9 The ‘313 Patent is entitled “Network interface with host independent buffer management.”  
10 The Abstract of the ‘313 Patent describes the invention as follows:

11 A network interface controller controls communication between a host system and a  
12 network transceiver coupled to a network comprises a memory outside of the host  
13 address space in which receive and transmit buffers are managed, host interface logic  
14 emulating memory mapped registers in the host address space, for transferring data  
15 between the host address space and the buffer memory, and network interface logic  
16 coupled with the network transceiver, for transferring data between the buffers in the  
17 buffer memory and the network transceiver. The buffer memory includes a transmit  
18 descriptor ring buffer, transmit data buffer, transfer descriptor buffer, and receive ring  
19 buffer all managed by operations transparent to the host.

16 **1. Claim 1**

17 Claim 1 of the ‘313 Patent claims:<sup>5</sup>

18 An apparatus for controlling communication between a host system and a  
19 network transceiver coupled with a network, wherein the host system includes  
20 a host address space, comprising:  
21 a buffer memory outside of the host address space;  
22 host interface means, sharing the host address space with the host, for  
23 managing data transfers between the host address space and the buffer  
24 memory in operations transparent to the host system; and

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23 <sup>4</sup> Since the parties have identified disputed terms, but have not tied their dispute to particular  
24 claims in which the disputed terms appear, the Court will use independent Claim 1 as the starting  
25 point for its analysis. Subject to further proceedings, the Court’s construction of any particular  
26 disputed term is presumed to apply consistently across all claims in the Patents-in-Suit in which the  
27 term appears. See, e.g., Paragon Solutions, LLC v. Timex Corp., 566 F.3d 1075, 1087 (Fed. Cir.  
28 2009).

27 <sup>5</sup> Unless otherwise indicated, all bold typeface is added by the Court for emphasis.

1 network interface means, coupled with the network transceiver, for  
2 managing data transfers between the buffer memory and the network  
transceiver.

3 **a. “host system”**

4 The parties dispute the meaning of the phrase “host system,” as used in Claim 1. Throughout  
5 the written description of the ‘313 Patent, the inventors use the word “host” and the phrase “host  
6 system.” For example, the inventors describe Figure 1 as follows:

7 The computer system includes a **host system**, including a host processor 10, host  
8 memory 11, and other host devices 12, all communicating through a host system bus  
13 13, such as an EISA bus. The host system bus 13 includes address lines which define  
a host system address space. Typically, for an EISA bus, there are 32 address lines  
9 establishing a host system address space of about 4 Gigabytes.

10 (‘313 Patent, Col. 4:8-15.)

11 A person of ordinary skill in the art would understand that the inventors are using the phrase  
12 “host system” with its commonly understood meaning, i.e., a computer system that provides  
13 connectivity and electronic service to an apparatus that is attached to the system.<sup>6</sup>

14 Accordingly, the Court construes the phrase “host system” to mean:

15 **a computer system to which an apparatus may be connected and which provides system  
16 resources to the apparatus.**

17 **b. “host address space”**

18 The Preamble to Claim 1 provides: “wherein the host system includes **a host address space**  
19 comprising . . . .” The parties dispute the meaning of the phrase “host address space.”

20 In the written description, the inventors use the phrase “host address space” interchangeably  
21 with the phrases “host system address space” and “host address block”:

22 FIG. 4 is a map of **host system address space** used for the  
transmission and reception of data according to the present invention.

23 (‘313 Patent, Col. 3:42-45.)

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24  
25 <sup>6</sup> See, e.g., MICROSOFT COMPUTER DICTIONARY 256 (5th ed. 2002) (defining “host” as: (1)  
26 “[t]he main computer in a mainframe or minicomputer environment—that is, the computer to which  
27 terminals are connected”; (2) “[i]n PC-based networks, a computer that provides access to other  
computers”; and (3) “[o]n the Internet or other large networks, a server computer that has access to  
28 other computers on the network. A host computer provides services, such as news, mail, or data, to  
computers that connect to it.”).

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FIG. 4 provides a simplified map of the adaptor interface **host address block 101**. The addresses within this block appear to the host like memory mapped registers in a continuous 8k block of the **host address space** in the preferred system.

(‘313 Patent, Col. 10:19-23.)

A person of ordinary skill in the art would understand that the inventors use the phrase “host address space” to refer to components of the host system that can be used by embodiments of the apparatus in various ways. For example, it is used by the inventors to refer to addresses on the host system bus that can be used by the apparatus as if it were memory.<sup>7</sup> The inventors also use the phrase to refer to a pre-specified range of addresses on the host system bus that can be used as if it were memory mapped registers.<sup>8</sup>

Accordingly, the Court construes “host address space” to mean:

**addresses on the host system bus that can be used as space for data.**

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<sup>7</sup> “As mentioned above, **the host system will include a host memory space** (generally 100) **defined by the addresses on the host bus**. A pre-specified block 101 of the host memory space is set aside for the adapter interface addresses.” (‘313 Patent, Col. 9:44-48.) “The host system bus 13 includes address lines which define a **host system address space**. Typically, for an EISA bus, there are 32 address lines establishing a **host system address space** of about 4 Gigabytes.” (‘313 Patent, Col. 4:11-15.)

<sup>8</sup> “FIG. 4 provides a simplified map of the adapter interface **host address block 101**. **The addresses within this block appear to the host like memory mapped registers** in a continuous 8K block of the **host address space** in a preferred system.” (‘313 Patent, Col. 10:19-23.)

“The present invention provides a network interface controller which controls communication between a host system and a network transceiver coupled to a network which comprises a buffer memory outside of the host address space in which receive and transmit buffers are managed, host interface logic responsive to **a prespecified range of host addresses, like memory mapped registers in the host address space, for mapping data between the host address space and the buffer memory . . .**” (‘313 Patent, Col. 1:61-2:2.)

“Because the host interface logic and network interface logic manage accesses to the buffer memory, the host system is able to access the multiple data buffers for transmitting and receiving data **through a limited prespecified address range**. The **dedicated memory mapped page in host address space** is automatically remapped through the host interface logic into the buffer memory in operations that are transparent to the host.” (‘313 Patent, Col. 2:6-14.)

“Although the ‘registers’ are **memory mapped to an arbitrary prespecified block of host address space**, none of the reads or writes performed by the host system to these registers actually directly access the adapter memory. Rather, the accesses to **the memory mapped space** are interpreted by the host interface logic 104 transparent to the host system. Thus, the memory in the adapter is independent of the host address space and of host management.” (‘313 Patent, Col. 10:29-37.)

1                    **c.        “host interface means”**

2                    The parties dispute whether the “host interface means” limitation should be construed as a  
3 means-plus-function limitation, and also dispute the meaning of the phrase “for managing data  
4 transfers between the host address space and the buffer memory in operations transparent to the host  
5 system.”

6                    **i.        Applicability of means-plus-function construction**

7                    Title 35 U.S.C. § 112 ¶ 6 provides:

8                    An element in a claim for a combination may be expressed as a means  
9 or step for performing a specified function without the recital of  
10 structure, material, or acts in support thereof, and such claim shall be  
11 construed to cover the corresponding structure, material, or acts  
12 described in the specification and equivalents thereof.

13                    A claim limitation that actually uses the word “means” invokes a rebuttable presumption that  
14 § 112 ¶ 6 applies. The presumption may be rebutted if the claim: (1) recites no function  
15 corresponding to the means; or (2) also recites “sufficient structure or material for performing that  
16 function.” Rodime PLC v. Seagate Tech., Inc., 174 F.3d 1294, 1302 (Fed. Cir. 1999). “Sufficient  
17 structure exists when the claim language specifies the exact structure that performs the functions in  
18 question without need to resort to other portions of the specification or extrinsic evidence for an  
19 adequate understanding of the structure.” TriMed, Inc. v. Stryker Corp., 514 F.3d 1256, 1259-60  
20 (Fed. Cir. 2008) (citations omitted). A proper recitation of specific structure need not include “every  
21 last detail of structure disclosed in the specification for performing the claimed . . . function.”  
22 Rodime, 174 F.3d at 1304. Further, sufficient structure may be disclosed when a “term, as the name  
23 for structure, has a reasonably well understood meaning in the art.” Watts v. XL Sys., Inc., 232 F.3d  
24 877, 880-81 (Fed. Cir. 2000) (citing Greenberg v. Ethicon Endo-Surgery, Inc., 91 F.3d 1580, 1583  
25 (Fed. Cir. 1996)). Also, a court may look to the written description for support of the structure  
26 recited in the claims. See, e.g., TI Grp. Auto. Sys. (N. Am.), Inc. v. VDO N. Am., L.L.C., 375 F.3d  
27 1126, 1135 (Fed. Cir. 2004).

28                    In this case, the inventors’ use of the tag word “means” raises a rebuttable presumption that §  
112 ¶ 6 applies. Thus, the issue becomes whether the presumption is rebutted by the lack of



1 recitation of a function or by a sufficient recitation of structure. As to the first of these questions, the  
2 Court finds that the inventors clearly recite a function, namely, “for managing data transfers.” As to  
3 the second of these questions, in addition to the tag word “means,” the limitation includes the  
4 modifier “host interface.” Thus, the issue becomes whether a person of ordinary skill in the art  
5 would understand “host interface means” to be a recitation of structure. Here, the inventors use the  
6 word “interface” to refer to a point where two things meet or interact. For example, in the  
7 “Summary of the Invention” section of the written description, the inventors use the phrase “network  
8 interface controller.” From the written description, a person of ordinary skill would understand that  
9 the “controller” is an apparatus that controls communication between a host system and a network  
10 transceiver. (‘313 Patent, Col. 2:61-65.) Further, the modifier “interface” is used to disclose *the*  
11 *location* of the controller as being between a host system and a network transceiver. As such, the  
12 Court finds that the inventors do not use the word “interface” to denote structure. Rather,  
13 throughout the written description, the word “interface” is used with its commonly understood  
14 meaning, i.e., the point or location where two or more separate elements come in contact with one  
15 another.<sup>9</sup>

16 The Court finds that “host interface means” is not a structure that has “a reasonably well  
17 understood meaning in the art.” Watts, 232 F.3d at 880-81.<sup>10</sup> Consequently, the Court finds that  
18 “host interface means” is not a recitation of structure sufficient to rebut the applicability of § 112 ¶  
19 6. Thus, the Court finds that § 112 ¶ 6 applies. Accordingly, the Court must decide the function of  
20 the host interface means and identify any “corresponding structure in the written description that is  
21 necessary to perform that function.” Altiris, Inc. v. Symantec Corp., 318 F.3d 1363, 1375 (Fed. Cir.  
22 2003).

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23  
24 <sup>9</sup> See, e.g., WEBSTER’S NINTH NEW COLLEGIATE DICTIONARY 631 (1990) (defining  
25 “interface” as “the place at which independent systems meet and act on or communicate with each  
26 other” or “an area in which diverse things interact”).

26 <sup>10</sup> The Federal Circuit has suggested that the rebuttable presumption may apply even though  
27 the word “means” was modified by a term that normally connotes structure. See DESA IP, LLC v.  
28 EML Tech., LLC, 211 Fed. Appx. 932, 936-37 (Fed. Cir. 2007).

1                                   ii.     **“for managing data transfers between the host**  
2                                           **address space and the buffer memory in operations**  
3                                           **transparent to the host system”**

4           The parties do not dispute that the function of “host interface means” is “for managing data  
5 transfers between the host address space and the buffer memory in operations transparent to the host  
6 system.” However, the parties dispute the meaning of “host address space” and “operations  
7 transparent to the host system.”

8           As discussed earlier, the Court has construed the phrase “host address space” with respect to  
9 the Preamble. The same definition applies to the use of that phrase in this limitation.

10                                   iii.    **“in operations transparent to the host system”**

11           The phrase “in operations transparent to the host system” is a limitation on how the function  
12 is performed. If a means-plus-function limitation contains a limitation on how the disclosed  
13 function is performed, the corresponding structure must be capable of performing the function with  
14 that additional limitation. Therefore, if there is a dispute over the words and phrases used in  
15 disclosing an additional limitation, the Court must construe the meaning of the words and phrases  
16 used in the additional limitation before examining the written description for corresponding  
17 structure.

18           In the written description, in a discussion of Figure 4, the inventors use the word  
19 “transparent” to refer to an operation that can be performed independent of, and without  
20 management by, the host system:

21                                   Although the ‘registers’ are memory mapped to an arbitrary  
22 prespecified block of host address space, none of the reads or writes  
23 performed by the host system to these registers actually directly access  
24 the adapter memory. Rather, the accesses to the memory mapped  
25 space are interpreted by the host interface logic 104 **transparent to**  
26 **the host system**. Thus, the memory in the adapter is **independent of**  
27 **the host address space and of host management**.

28           (‘313 Patent, Col. 10:29-39.)

          Accordingly, the Court construes “in operations transparent to the host system” to mean:

**in operations performed independently of management by the host system.**

          Consequently, the Court construes the function of “host interface means” as:

1           **for managing data transfers between address spaces on the host system bus and the**  
2           **buffer memory in operations performed independently of management by the host**  
3           **system.**

4                                   **iv.       corresponding structure**

5           As a preliminary matter, the parties dispute the appropriate degree of specificity that the  
6           Court should use in identifying the corresponding structure.

7           “[S]tructure disclosed in the specification is ‘corresponding’ structure only if the  
8           specification or prosecution history clearly links or associates that structure to the function recited in  
9           the claim.” B. Braun Med., Inc. v. Abbott Labs., 124 F.3d 1419, 1424 (Fed. Cir. 1997). In other  
10          words, the structure must be necessary to perform the claimed function. See Northrop Grumman  
11          Corp. v. Intel Corp., 325 F.3d 1346, 1352 (Fed. Cir. 2003). The relevant structure is that which  
12          corresponds to the recited function. See Chiuminatta Concrete Concepts, Inc. v. Cardinal Indus.  
13          Inc., 145 F.3d 1303, 1308-09 (Fed. Cir. 1998). Because the corresponding structure and its  
14          equivalent is limiting, any corresponding structure disclosed in the specification should be clearly  
15          identified. See Kahn v. General Motors Corp., 135 F.3d 1472, 1476 (Fed. Cir. 1998). However, the  
16          written description need not explicitly describe the corresponding structure. See Atmel Corp. v.  
17          Info. Storage Devices, Inc., 198 F.3d 1374, 1381-82 (Fed. Cir. 1999). If the written description  
18          contains an implicit description that a person of ordinary skill in the art would recognize as  
19          performing the recited function, the statutory requirement is satisfied. Id.

20          In this case, the parties’ respective contentions with respect to corresponding structures were  
21          asserted prior to the Court’s construction the function. As such, the Court finds that it would benefit  
22          from further briefing on the issue of corresponding structures. In their supplemental briefs, the  
23          parties shall address the level of specificity that should be used in identifying the corresponding  
24          structure as follows:

- 25                   (1)       The parties shall identify each structure in the written description that the  
26                   party contends is necessary to perform the function identified by the Court  
27                   and that is linked to that function by the disclosure (drawings or language) in  
28                   the specification.

1 (2) As to each structure, the parties shall explain why the structure is necessary  
2 and linked, and must cite the passage of the specification upon which the  
3 party relies.

4 (3) To the extent a party contends that a particular level of detail is required in  
5 order for a structure to qualify as corresponding, the party must explain why  
6 that level of detail is required.

7 **d. “network interface means”**

8 Claim 1 of the ‘313 Patent discloses that the apparatus comprises “network interface means,  
9 coupled with the network transceiver, for managing data transfers between the buffer memory and  
10 the network transceiver.” For convenience, the Court will refer to this as the “network interface  
11 means limitation.” The parties dispute whether § 112 ¶ 6 applies to this limitation.

12 For the same reasons discussed with respect to the “host interface means” limitation, the  
13 Court finds that the “network interface means” limitation is governed by § 112 ¶ 6.<sup>11</sup> Undisputedly,  
14 the function of the “network interface means” is “for managing data transfers between the buffer  
15 memory and the network transceiver.” Further, as discussed above, the Court finds that it would  
16 benefit from further briefing on the issue of corresponding structures as to this function. In doing so,  
17 the parties shall adhere to the same directions regarding the level of specificity for identifying and  
18 explaining such corresponding structures that is outlined above.

19 **2. Claim 3**

20 Claim 3 of the ‘313 Patent claims:

21 The apparatus of claim 1, wherein the host interface means includes:  
22 transmit descriptor **logic** for mapping transmit descriptors identifying  
23 data to be transmitted from the host system to the buffer memory; and  
24 download **logic**, responsive to transmit descriptors in the buffer  
25 memory, for retrieving data from memory in the host address space and  
26 storing retrieved data in the buffer memory.

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27 <sup>11</sup> The inventors disclose a “network interface means, coupled with the network transceiver”  
28 for performing a recited function. This raises the question of whether the function is performed by  
the means alone, or is performed jointly by the “coupled” means and the network transceiver. The  
Court adopts the former construction.

1 The parties dispute the meaning of the word “logic” as used in Claim 3 of the ‘313 Patent.  
2 The word logic is widely used by the inventors in the Claims of the ‘313 Patent and in the written  
3 description.<sup>12</sup> The Court finds that a person of ordinary skill in the art would understand that with  
4 respect to computer systems, the word “logic” can be used to mean a wide range of things,  
5 depending on how the word is used.<sup>13</sup> For example, “logic” may denote hardware structures, as in  
6 “logic gates” and “logic circuits”; it may denote software routines, as in “programming logic” and  
7 “logic algorithm”; or it may have abstract meanings, as in “mathematical logic” and “symbolic  
8 logic.”

9 In neither the claim nor the written description do the inventors disclose whether the  
10 “transmit descriptor **logic**” or the “download **logic**” as used in Claim 3 of the ‘313 Patent is  
11 hardware, software or a combination of both. Without reaching the issue of whether it would be  
12 permissible to leave its implementation unspecified, at this time the Court declines to construe the  
13 word “logic” on the ground that the lack of specificity renders Claim 3 arguably ambiguous. The  
14 Court invites the parties to address this issue. The parties are ordered to meet and confer with  
15 respect to ten phrases that includes the word “logic” and that are in dispute, and to file a joint  
16 submission regarding their respective constructions of those phrases.

17 **3. Claim 13**

18 Claim 13 of the ‘313 Patent claims:

19 An apparatus for controlling communication between a host system  
20 and a network transceiver coupled with a network, wherein the host  
21 system includes a host address space, comprising:  
22 a buffer memory outside of the host address space, including a  
23 transmit buffer and a receive buffer;  
24 host interface means, sharing host address space including a  
25 prespecified block of host addresses of limited size defining a first

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23 <sup>12</sup> For example, the word “logic” is used in at least the following phrases: “host interface  
24 **logic**,” “network interface **logic**,” “DMA **logic**,” “download **logic**,” “upload **logic**,” “transmit  
25 descriptor **logic**,” “transfer descriptor **logic**,” “view **logic**,” “receive **logic**,” “transmit **logic**,”  
26 “transmit ring pointer **logic**,” “receive ring pointer **logic**,” “conversion **logic**,” and “adaptor mode  
27 **logic**.”

28 <sup>13</sup> See, e.g., WEBSTER’S NEW WORLD COMPUTER DICTIONARY 218 (10th ed. 2003) (defining,  
29 *inter alia*, such terms as “logical address,” “logical network,” “logic bomb” and “logic gate”).

1 area and a second area, and coupled with the buffer memory, for  
2 mapping data addressed to the first area into the transmit buffer,  
3 mapping data in the receive buffer into the second area, and uploading  
4 data from the receive buffer to the host; and

5 **network interface means**, coupled with the network  
6 transceiver and the buffer memory, for transferring data from the  
7 transmit buffer to the network transceiver and mapping data into the  
8 receive buffer from the network transceiver.

9 With respect to Claim 13 of the ‘313 Patent, the only dispute tendered to the Court for  
10 resolution is whether § 112 ¶ 6 applies to the “network interface means” limitation. For the same  
11 reasons discussed with respect to the “network interface means” limitation disclosed in Claim 1, the  
12 Court finds that the “network interface means” limitation in Claim 13 is governed by § 112 ¶ 6, and  
13 has the same meaning as it has in Claim 1, and should be addressed similarly in supplemental  
14 briefing.

15 **B. The ‘459 Patent**

16 The ‘459 Patent is entitled “Network adapter with host indication optimization.” The  
17 Abstract of the ‘459 Patent describes the invention as follows:

18 Optimized indication signals of a completed data frame transfer are generated by a  
19 network adapter which reduces host processor interrupt latency. The network adapter  
20 comprises network interface logic for transferring the data frame between the  
21 network and a buffer memory and host interface logic for transferring the data frame  
22 between the buffer memory and the host system. The network adapter further  
23 includes threshold logic where a threshold value in an alterable storage location is  
24 compared to a data transfer counter in order to generate an early indication signal.  
25 The early indication signal may be used to generate an early interrupt signal to a host  
26 processor before a transfer of a data frame is completed. The network adapter also  
27 posts status information status registers which may be used by the host processor to  
28 tune the timing of the generation of the network adapter interrupt signal.

1 **1. Claim 1**

2 Claim 1 of the ‘459 Patent claims:

3 An apparatus for transferring a data frame between a network transceiver,  
4 coupled with a network, and a host system which includes a host processor  
5 and host memory, the apparatus generating an indication signal to the host  
6 processor responsive to the transfer of the data frame, with the host processor  
7 responding to the indication signal after a period of time, comprising:  
8 a buffer memory for storing the data frame;  
9 network interface logic for transferring the data frame between the  
10 network transceiver and the buffer memory;  
11 host interface logic for transferring the data frame between the host  
12 system and the buffer memory;

1 threshold logic for allowing the period of time for the host processor  
2 to respond to the indication signal to occur during the transferring of the data  
3 frame, wherein the threshold logic includes,  
4 a counter, coupled to the buffer memory, for counting the  
5 amount of data transferred to or from the buffer memory;  
6 an alterable storage location containing a threshold value; and  
7 **means for comparing the counter to the threshold value in**  
8 **the alterable storage location and generating an indication signal**  
9 **to the host processor responsive to a comparison of the counter**  
10 **and the alterable storage location.**

11 The parties dispute the construction of the “means for comparing” limitation. The parties  
12 agree that this limitation should be construed under § 112 ¶ 6, and that the function performed by the  
13 claimed “means” is “comparing the counter to the threshold value in the alterable storage location  
14 and generating an indication signal to the host processor responsive to a comparison of the counter  
15 and the alterable storage location.” However, the parties dispute what structure or structures  
16 disclosed in the written description qualify as corresponding structure. As discussed above, the  
17 Court finds that it would benefit from further briefing on the issue of corresponding structures. In  
18 doing so, the parties shall adhere to the directions outlined above regarding the level of specificity  
19 for identifying and explaining such corresponding structures.

20 **2. Claim 22**

21 Claim 22 of the ‘459 Patent claims:

22 A network adapter for receiving a data frame from a network transceiver,  
23 coupled with a network and a host system which includes an interruptable  
24 host processor with **interrupt latency** and host memory, comprising:  
25 a buffer memory for storing the data frame;  
26 receive logic for receiving the data frame from the network transceiver  
27 to the buffer memory;  
28 receive threshold logic for generating an indication signal during the  
receiving of the data frame, wherein the receive threshold logic includes,  
a counter, coupled to the buffer memory, for counting the  
amount of data received by the buffer memory;  
an alterable storage location containing a receive threshold  
value;  
means for comparing the counter to the receive threshold value  
in the alterable storage location and generating an indication signal  
responsive to a comparison of the counter and the alterable storage  
location; and  
host interface logic for transferring the data frame from the  
buffer memory to the host system, wherein host interface logic  
includes,

1 control means for generating an interrupt signal to the  
2 host processor, responsive to the indication signal,  
3 which reduces host processor **interrupt latency**.

4 The parties dispute the meaning of the phrase “interrupt latency.” A person of ordinary skill  
5 in the art would understand that Claim 22 claims the invention of an apparatus “which reduces host  
6 processor interrupt latency.” The disputed phrase is included in two longer phrases in Claim 22.  
7 First, the phrase “host processor with **interrupt latency**” appears in the Preamble. Second, the  
8 disputed phrase also appears in a longer phrase in the “control means” limitation: “control means for  
9 generating an interrupt signal to the host processor, responsive to the indication signal, which  
10 reduces host processor **interrupt latency**.”

11 **a. “host processor with interrupt latency”**

12 Claim 22 claims an apparatus coupled with a host system. In their first use of the phrase  
13 “interrupt latency,” the inventors use it to describe an inherent feature of the host system, i.e., a host  
14 system that includes an interruptable host processor “with interrupt latency.” From the Background  
15 section of the written description, it is clear that when the inventors use the phrase “host processor  
16 with interrupt latency,” they are describing a feature of prior art:

17 In prior art systems, such as the National Semiconductor DP83932B, a systems-  
18 oriented network interface controller (SONIC) and the Intel 82586 local area network  
19 co-processor, **an interrupt** is generated by the network adapter to the host processor  
20 on the completion of a data transfer. The host processor then must determine the  
21 cause of the interrupt by examining the appropriate network adapter status registers  
22 and take the appropriate action. However, **before the host processor services the  
interrupt, the host processor must save its current environment or system  
parameters**. This routine of saving the host processor’s current environment **may  
take as long as 30ms** for a OS/2 operating system. The period of time necessary for  
saving the host processor’s environment depends upon the type of host processor  
used, the host computer system configuration and when the interrupt /ccurred [sic].

(‘459 Patent, Col. 1:46-62.)

23 Thus, the Court finds that in using the phrase “host processor with interrupt latency,” the  
24 inventors are describing the inherent delay that takes place between the point in time when the  
25 processor receives an “interrupt” and when the processor is able to service the interrupt.



1                   b.       **“control means for generating an interrupt signal to the host processor,  
2                                           responsive to the indication signal, which reduces host processor  
3                                           interrupt latency”**

4                   The parties’ dispute over the proper construction of “interrupt latency” raises an issue with  
5                   respect to whether the phrase should be given a different construction when it is used in the “control  
6                   means” limitation.<sup>14</sup> As discussed above, processor interrupt latency is an inherent part of the host  
7                   processor and, as such, cannot be “reduced.” Although Claim 22 uses the phrase “reduces host  
8                   processor interrupt latency,” a person of ordinary skill in the art would understand that the inventors  
9                   are *not* using the word “reduce” to mean an *actual* reduction in the host processor’s inherent  
10                  interrupt latency, but instead are using it to mean an *apparent or effective* reduction in delay. This  
11                  *apparent or effective* reduction in delay is achieved because the invention sends an “interrupt” while  
12                  the data transfer is in process. The remainder of the transfer occurs during the interrupt latency time  
13                  period. Thus, the delay that was experienced in prior art systems that waited for the transfer to be  
14                  completed before sending an “interrupt” is effectively reduced or eliminated in the invention. By  
15                  sending an interrupt signal before the full data frame has been transferred, and timing the sending in  
16                  such a manner that the full data frame will have been transferred by the time the processor turns its  
17                  attention to servicing the interrupt, an efficiency in time is gained over a system that waits for full  
18                  data frame transfer before sending the interrupt.

19                  In discussing an embodiment that practices this invention, the inventors state:

20                  **Threshold logic 10 in network adapter 3 is designed for eliminating or reducing**  
21                  **interrupt latency.** Threshold logic 10 makes a determination of how much of a data  
22                  frame is transferred before generating an early indication signal. The early indication  
23                  signal may then cause an early interrupt signal to be generated during the transfer of a  
24                  data frame. Moreover, threshold logic 10 is designed such that the time required for  
25                  transferring the remainder of the data frame should approximately equal the time  
26                  required for host processor 5 save its system parameters. Therefore, **interrupt**  
27                  **latency is eliminated or reduced** by allowing host processor 5's interrupt routine to  
28                  coincide with the transfer of the remainder of the data frame.

(‘459 Patent, Col. 6:9-22.)

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<sup>14</sup> In construing the disputed language, the Court leaves for later consideration the question of whether the phrase is: (1) limiting or (2) effectively a “whereby” clause, i.e., words of the Claim that are merely a recitation of the necessary result of the functioning of the previously recited apparatus, and which add nothing to the substance of the Claim.

1 In the “Conclusion” section of the written description, the inventors state:

2 Therefore, the present invention reduces host processor interrupt latency by  
3 generating early indications of data frame transfers. These early indications then may  
4 be used to generate an early interrupt to the host processor before the data frame is  
transferred which allows the host processor to save its current environment during a  
data frame transfer.

5 (‘459 Patent, Col. 41:44-50.)

6 Accordingly, in the limitation, “control means for generating an interrupt signal to the host  
7 processor, responsive to the indication signal, which reduces host processor interrupt latency,” the  
8 Court construes “which reduces host processor interrupt latency” to mean:

9 **an apparent reduction in interrupt latency achieved by sending an interrupt signal  
10 before the data frame transfer has been completed.**<sup>15</sup>

11 **C. The ‘094 Patent**

12 The ‘094 Patent is entitled “Method for automatic initiation of data transmission.” The  
13 Abstract of the ‘094 Patent describes the invention as follows:

14 Early initiation of transmission of data in a network interface that includes a  
dedicated transmit buffer is provided in a system which includes logic for transferring  
15 frames of data composed by the host computer into the transmit buffer. The amount  
of data of a frame which is downloaded by the host to the transmit buffer is  
16 monitored to make a threshold determination of an amount of data of the frame  
resident in the transmit data buffer. The network interface controller includes logic  
17 for initiating transmission of the frame when the threshold determination indicates  
that a sufficient portion of the frame is resident in the transmit buffer, and prior to  
18 transfer of all of the data of the frame into the transmit buffer. The monitoring logic  
includes a threshold store, which is programmable by the host computer for storing a  
19 threshold value. Thus, the threshold value may be set by the host system to optimize  
performance in a given setting.

20 Claim 1 of the ‘094 Patent claims:

21 A method for transmitting a frame of data from a host system through a  
network interface device to a network, comprising:  
22 executing a frame transfer task initiated in the host system to transfer a  
frame to a buffer memory in the network interface device; and  
23 **executing a frame transmission task** in the network interface device  
to initiate transmission of the frame from the buffer memory to the network in  
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25 <sup>15</sup> The Court reserves for later consideration the question of whether it is appropriate for the  
26 Court to include an explanation of *how* the invention effectively reduces interrupt latency. In  
27 particular, although the inventors discuss an effective reduction in interrupt latency, the Court  
declines to consider at this time whether effective reduction in interrupt latency is claimed.

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parallel with the frame transfer task before the frame is completely transferred to the buffer memory.

The parties dispute whether the phrase “executing a frame transmission task” is so ambiguous as to render Claim 1 indefinite and also to cause Claim 1 to fail to satisfy the written description requirements of 35 U.S.C. § 112 ¶¶ 1-2.

The purpose of the definiteness requirement is to “ensure that the claims delineate the scope of the invention using language that adequately notifies the public of the patentee’s right to exclude.” Datamize, LLC v. Plumtree Software, Inc., 417 F.3d 1342, 1347 (Fed. Cir. 2005). Claims are considered indefinite when they are “not amenable to construction” or are “insolubly ambiguous.” Id. Thus, the “definiteness of claim terms depends on whether those terms can be given any reasonable meaning.” Id. However, a claim is not indefinite “merely because it poses a difficult issue of claim construction.” Exxon Research & Eng’g Co. v. United States, 265 F.3d 1371, 1375 (Fed. Cir. 2001). Rather, if the “meaning of the claim is discernible, even though the task may be formidable and the conclusion may be one over which reasonable persons will disagree,” the claim is “sufficiently clear to avoid invalidity on indefiniteness grounds.” Id.

Here, the phrase “executing a frame transmission task” is not defined in Claim 1. Further, the phrase is not used in the written description. Moreover, the phrase has no plain meaning. With respect to transmission of data, the general word “transmission” does have a plain meaning, namely, sending data from one place to another. However, for at least three reasons, the general meaning is not useful in making a determination of the meaning of “executing a frame transmission task.”

First, by definition, any “transmission” is a self-contained act, namely, “an act of transmitting.”<sup>16</sup> Thus, by their use of the word “executing,” the inventors must have meant something that required execution. Second, Claim 1 states that “executing a frame transmission task” is “to initiate transmission of the frame from the buffer memory.” In general, to “initiate” a transmission means to cause that transmission to begin. Thus, if the “transmission task” causes transmission to begin, the task is not the transmission, and the task itself must be completed or at

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<sup>16</sup> WEBSTER’S NEW COLLEGIATE DICTIONARY 1241 (1975).

1 least started before the transmission is begun. Third, the dependent claims make clear that  
2 “transmission task” is something specific, albeit undefined. For example, dependent Claim 2 claims:

3 The method of claim 1, wherein **the frame transmission task** includes  
4 executing a carrier sense, multiple access protocol.

5 Further, dependent Claim 5 provides:

6 The method as in<sup>17</sup> Claim 1, wherein **the frame transmission task** includes:  
7 appending an error detection code to the frame of data to be transmitted to the  
8 network.

9 The phrase was added to Claim 1 during its prosecution. However, there was no discussion  
10 of it during the prosecution. The step is an essential limitation of Claim 1. Insofar as the patent  
11 claims an essential step that has no plain meaning, and that is not defined or referred to elsewhere in  
12 the specification, Claim 1 is arguably indefinite. However, for the Court to determine that Claim 1  
13 is indefinite, it would have to consider whether one skilled in the art would understand the bounds of  
14 the Claim when read in light of the specification. See Miles Labs., Inc. v. Shandon Inc., 997 F.2d  
15 870, 875 (Fed. Cir. 1993). Further, the Court does not reach the issue of whether Claim 1 is  
16 rendered invalid for lack of a written description.

17 Accordingly, the parties shall address this issue in supplemental briefing to be submitted as  
18 part of a further Case Management Conference set at the conclusion of this Order.<sup>18</sup>

19 **D. The ‘872 Patent**

20 The ‘872 Patent is entitled “Apparatus for automatic initiation of data transmission.” The  
21 Abstract of the ‘872 Patent describes the invention as follows:

22 Early initiation of transmission of data in a network interface that includes a  
23 dedicated transmit buffer is provided in a system which includes logic for transferring  
24 frames of data composed by the host computer into the transmit buffer. The amount  
25 of data of a frame which is downloaded by the host to the transmit buffer is  
26 monitored to make a threshold determination of an amount of data of the frame

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27 <sup>17</sup> The Court notes that Claim 5 uses the wording “The method **as in** Claim 1,” instead of the  
28 more common “The method in Claim 1.”

<sup>18</sup> The Court’s conclusion applies to all other Claims of the ‘094 Patent that include the  
phrase “executing a frame transmission task.” However, the Court does not reach the issue of the  
ambiguity of this phrase in other claims of the ‘094 Patent because those claims were not tendered to  
the Court for construction.

1 resident in the transmit data buffer. The network interface controller includes logic  
2 for initiating transmission of the frame when the threshold determination indicates  
3 that a sufficient portion of the frame is resident in the transmit buffer, and prior to  
4 transfer of all of the data of the frame into the transmit buffer. The monitoring logic  
includes a threshold store, which is programmable by the host computer for storing a  
threshold value. Thus, the threshold value may be set by the host system to optimize  
performance in a given setting.

5 **1. Claim 1**

6 Claim 1 of the '872 Patent provides:

7 For a system transmitting frames of data across a communications medium;  
8 an apparatus comprising:

9 **buffer memory for storing data of frames composed by the host  
10 computer for transmission on the communications medium;**

11 means, having a host system interface, for transferring data of frames  
12 to the buffer memory;

13 means, coupled with the buffer memory, for monitoring the  
14 transferring of data of a frame to the buffer memory to make a threshold  
15 determination of an amount of data of the frame transferred to the buffer  
16 memory;

17 means, responsive to the threshold determination of the means for  
18 monitoring, for initiating transmission of the frame prior to transfer of all the  
19 data of the frame to the buffer memory from the host computer;

20 transmit logic, responsive to the means for initiating transmission, for  
21 retrieving data from the buffer memory and supplying retrieved data for  
22 transmission on the communications medium; and

23 underrun control logic, which detects a condition in which the means  
24 for transferring falls behind the transmit logic, and supplies a bad frame signal  
25 to the communications medium in response to the underrun condition.

26 **a. "buffer memory for storing data of frames composed by the host  
27 computer for transmission on the communications medium"**

28 The parties agree that "buffer memory" means "a memory for temporary storage of data."

However, Plaintiff requests the Court to add the limitation "wherein the buffer memory is able to  
retain a frame of data that has been transmitted" to the disputed phrases.<sup>19</sup> Because the additional  
language would add a limitation that is not required by the specification, the Court declines  
Plaintiff's request.

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<sup>19</sup> (See Plaintiff's Reply Claim Construction Brief at 15, Docket Item No. 565.)

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b. “means . . . for monitoring the transferring of data of a frame to the buffer memory”

Claim 1 of the ‘872 Patent discloses an apparatus comprising: “means, coupled with the buffer memory, for monitoring the transferring of data of a frame to the buffer memory to make a threshold determination of an amount of data of the frame transferred to the buffer memory.” The parties agree that the “means . . . for monitoring” limitation should be construed under § 112 ¶ 6. However, the parties dispute whether the function performed by the claimed means includes the phrase “to make a threshold determination of an amount of data of the frame transferred to the buffer memory.”

The “means for initiating transmission” limitation that follows the “means for monitoring” provides: “means, responsive to the threshold determination of the means for monitoring.” Thus, the function of making a “threshold determination” by the “means for monitoring” is a necessary antecedent to the “means for initiating transmission.” Therefore, the Court finds that the subject language is part of the claimed function.

c. “host computer”

The term “host computer” is also used in Claim 1 of the ‘872 Patent. Upon review, the Court finds that the inventors use the phrase “host computer” synonymously with the phrase “host system” as it appears in the ‘313 patent. Accordingly, the Court construes the phrase “host computer” identically with its construal of the phrase “host system” in the context of the ‘313 patent.

2. Claim 21

Claim 21 of the ‘872 Patent claims:

A network interface adapter for a carrier sense, multiple access network with collision detection (CSMA/CD), comprising:

**buffer memory which stores data of frames composed by a host computer for transmission on the network;**

data transfer circuitry, having a host system interface, for transferring data of frames to the buffer memory;

**logic**, coupled to the buffer memory, which monitors the transferring of data of a frame to the buffer memory to make a threshold determination of an amount of data of the frame transferred to the buffer memory;

a medium access controller for the CSMA/CD network coupled to the buffer memory for managing transmission of frames of data from the buffer memory to the network; and

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logic, responsive to the threshold determination of the logic which monitors the transferring of data to the buffer memory, which initiates transmission of the frame from the buffer memory to the medium access controller prior to transfer of all of the data of the frame to the buffer memory, including logic which initiates transmission of the frame when no complete frame of data is present in the buffer memory.

As with Claim 1, the parties agree that “buffer memory” means “a memory for temporary storage of data.” However, Plaintiff requests the Court to add the limitation “wherein the buffer memory is able to retain a frame of data that has been transmitted” to the disputed phrases.<sup>20</sup> For the same reasons stated above, the Court declines Plaintiff’s request.

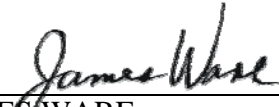
Further, the parties dispute whether the “logic . . . which monitors” in Claim 21 should be construed under § 112 ¶ 6. However, the Court declines to consider this matter pending a response by the parties to the matters discussed above.

**IV. CONCLUSION**

The Court has construed the disputed phrases as tendered by the parties. Consistent with the terms of this Order, on or before **February 21, 2012**, the parties shall meet and confer and file supplemental briefs as directed. These briefs shall be filed simultaneously. On or before **February 24, 2012**, the parties shall deliver two Chambers’ copies of the supplemental briefs in three ring binders.

The Court sets **March 12, 2012 at 11 a.m.** for a Further Case Management Conference. On or before **March 2, 2012**, the parties shall file a Joint Case Management Statement. The Statement shall include, among other things, how this case should proceed in light of this Order.

Dated: January 31, 2012

  
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JAMES WARE  
United States District Chief Judge

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<sup>20</sup> (See Plaintiff’s Reply Claim Construction Brief at 15, Docket Item No. 565.)

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**Dated: January 31, 2012**

**Richard W. Wieking, Clerk**

By:     /s/ JW Chambers      
**Susan Imbriani**  
**Courtroom Deputy**