EXHIBIT D

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ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 668 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (571)-272-4200.

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Regarding new Claim 59, new Claim 59 recites, "an apparatus for generating scrambling codes in mobile communication system having a scrambling code generator", "a first m-sequence generator to generate a first m-sequence", and "a second m-sequence generator to generate a second m-sequence". In this context, the description on page 7 discloses in lines 14 and 15 that a Gold code used herein as a scrambling code is generated through binary adding of two distinct m-sequences.

Moreover, new Claim 59 recites, "at least one adder for generating a ((K-1)*M+K)-th gold code as a K-th primary scrambling code by adding a ((K-1)*M+K-1)-times shifted first m-sequence and the second m-sequence". The description on page 12, lines 24 to 26 discloses, referring to Fig. 9, that when M secondary scrambling codes correspond to one primary scrambling code, the first, (M+2)'th, (2M+3)'th, ... , ((K-1)*M+K)'th, ..., and (511M+512)'th Gold codes are used as primary scrambling codes. The description also discloses on page 7, lines 23 to 25, that for the purpose of the present invention, the sum of the m-sequence m1(t) cyclically shifted time and the m-sequence m2(t) will be designated as a Gold code g, that is, g (t) = m1(t +)+m2(t).

Finally, new Claim 59 recites, "wherein K is a natural number and M is a total number of secondary scrambling codes per one primary scrambling code". The description on page 12, lines 26 to 29 discloses that the secondary scrambling codes corresponding to the (((K-1)*M+K)'th Gold code used as the (K)'th primary scrambling code are composed of M Gold codes, i.e., ((K-1)*M+(K+1)), ((K-1)*M+(K+2))..., and (K*M+K)'th Gold codes.

Regarding new Claim 65, new Claim 65 recites, "a method for generating scrambling codes in mobile communication system having a scrambling code generator", "generating a first m-sequence" and "generating a second m-sequence", and "generating a ((K-1)*M+K)-th Gold code as a K-th primary scrambling code by adding the ((K-1)*M+K-1)-times shifted first m-sequence and the second m-sequence". The description on page 12, lines 24 to 26 discloses, referring to Fig. 9, that when M secondary scrambling codes correspond to one primary scrambling code, the first, (M+2)'th, (2M+3)'th, ..., ((K-1)*M+K)'th, ..., and (511M+512)'th Gold codes are used as primary scrambling codes. Further, the description on page 7, lines 23 to 25

This means that a small number of connections with variable bit-rate connection might allocate all available spreading codes even if they do not have to use all of them simultaneous.

Another example of a scheme to assign spreading codes to a connection is the dynamic allocation.

A dynamic allocation means that all connections share a common pool of spreading codes that are continuously redistributed by a base station, according to the instantaneous need of each connection.

Each time the bit-rate at a connection is to be increased the base station has to inform the radio unit what new spreading codes to receive. This will require a significant overhead in the communication between the base station and radio unit.

The US patent US 5 533 013 describes a method and a system for assigning complete orthogonal spreading codes and radio channels in a combined CDMA/TDMA or TDMA/CDMA communication system. Said method comprises the step of assigning an orthogonal spreading code selected from a set of complete orthogonal spreading codes. Said system comprises means for assigning orthogonal spreading codes selected from at least one code set of complete orthogonal spreading codes. If more than one set, the code sets of complete orthogonal spreading codes have been selected so that they are completely orthogonal in relation to each other.

The US patent US 5 452 328 describes a method for assigning disjoint sets of binary spreading-code sequences to different nodes in a multi-node communication network.
Each node in the network is allotted spreading-code sequences which are selected from a family of "almost orthogonal" binary sequences. The patent also describes an apparatus and a method

for generating said family of sequences by combining a first and a second multi-stage shift register.

As will be seen herein, each of the methods disclosed in these patents is of a different construction than the method of the present invention.

The name radio unit includes all portable and non-portable equipment intended for radio communication, like mobile phones, pagers, telex, electronic notebooks and communicators. These equipment's can be used in any type of radio communication system, such as cellular networks, satellite or small local networks.

SUMMARY

The present invention meets problems related to how a forward-link connection is assigned specific spreading codes in a DS-CDMA communication system where only a finite number of orthogonal spreading codes are available.

One problem occurs when the system is using static allocation for variable bit-rate connections. The system may run out of spreading codes even if only a small number of spreading codes are actually used simultaneous. Each connection has allocated the amount of spreading codes that is needed for the maximum bit-rate irrespective of if the maximum bit-rate is needed for only a short time.

Another problem occurs when the system is using dynamic allocation for variable bit-rate connections. A significant overhead in the communication between the base station and the radio unit is needed to inform the radio unit what new spreading codes to receive each time the bit-rate is increased.

despread at the multipliers 320, 322, 324 and 326 and output to corresponding demultiplexers 330 and 350. The demultiplexers 330 and 350 demultiplex the despread I- and Q-channel components, respectively .

Fig. 4 is a schematic block diagram of the scrambling code group generator 300 shown in Fig. 3, which concurrently generates multiple scrambling code groups . Although the scrambling code group generator 300 is to use primary scrambling codes for common control channels in fact, it can also use secondary scrambling codes for channels used depending on the users, such as data channels, in case of a lack of available orthogonal codes. Thus the mobile station has to be capable of generating multiple scrambling code groups.

Referring to Fig. 4, the scrambling code group generator 300 of the receiver includes a plurality of gold sequence generators 401 and a plurality of delays 403 corresponding to the gold sequence generators 401. Upon receiving control information about the scrambling codes for multiple channels from an upper layer, the gold sequence generators 401 generate gold sequence codes corresponding to the control information and output the generated gold sequence codes to have an I-channel component. The delays 403 delay the gold sequence codes with the I-channel component for a predetermined number of chips to generate the gold sequence codes of a Q-channel component.

Fig. 5 is a schematic diagram illustrating the structure of the gold sequence generators shown in Figs. 2 and 4 .

Referring to Fig. 5, a gold sequence is normally generated through binary adding of two distinct m-sequences. A shift register that generates the upper m-sequence is implemented with a generator polynomial defined as $f(x) = x^{18} + x^7 + 1$, and a shift register generating the lower m-sequence is implemented with a generator polynomial defined as $f(x) = x^{18} + x^{10} + x^7 + x^5 + 1$.

downlink receiver in the general UMTS mobile communication system;

Fig. 4 is a schematic block diagram of a known scrambling code group generator shown in Fig. 3;

Fig. 5 is a detailed diagram showing the structure of a known scrambling gold group generator in the general UMTS mobile communication system;

Fig. 6 is a diagram showing the structure of a scrambling code in accordance with a first embodiment of the present invention;

Fig. 7 is a detailed diagram showing the structure of a scrambling code group generator of a downlink transmitter in a UMTS mobile communication system in accordance with the first embodiment of the present invention;

Fig. 8 is a detailed diagram showing the structure of a scrambling code group generator of a downlink receiver in a UMTS mobile communication system in accordance with the first embodiment of the present invention;

Fig. 9 is a diagram showing the structure of a scrambling code in accordance with a second embodiment of the present invention;

Fig. 10 is a detailed diagram showing the structure of a scrambling code group generator of a downlink transmitter in a UMTS mobile communication system in accordance with the second embodiment of the present invention; and

Fig. 11 is a detailed diagram showing the structure of a scrambling code group generator of a downlink receiver in a UMTS mobile communication system in accordance with the second embodiment of the present invention;

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A preferred embodiment of the present invention will be described below with reference to the accompanying drawings. In the following description, well-known functions or constructions are not described in detail since they would obscure the invention in unnecessary detail.

A gold code used herein as a scrambling code is generated through binary

adding of two distinct m-sequences. Assuming that the two m-sequences each having a length L are defined as m1(t) and m2(t), respectively, a set of gold codes may comprise L distinct gold sequences with good correlation characteristic with one another. The set of gold codes can be expressed by Equation 1.

[Equation 1]

$G = \langle m_1(t+\tau) + m_2(t) | 0 \le \tau \le L-1 \rangle$ where, t is a time variable number and τ is shift value. As understood from Equation 1, the set of gold codes is a set of all sequences that comprises the sum of the m-sequence $m_1(t)$ cyclically shifted τ times and the m-sequence $m_2(t)$. Thus, for the purpose of the present invention, the sum of the m-sequence $m_1(t)$ cyclically shifted τ time and the m-sequence $m_2(t)$ will be designated as a gold code g_τ. That is, $g_\tau(t) = m_1(t+\tau) + m_2(t)$. If the period of the gold code is 2^{18}-1, then the individual m-sequences constituting the gold code also have a period of 2^{18}-1. Thus the m-sequence $m_1(t)$ can be cyclically shifted a maximum of 2^{18}-1 times and the number of elements in the set of the gold codes is equal to 2^{18}-1, which is the maximum value of the cyclic shift.

The set of gold codes used in the embodiments of the present invention has 2^{18}-1 gold codes as elements each of which comprises an m-sequence $m_1(t)$ having a generator polynomial defined as $f(x) = x^{18} + x^7 + 1$ and an m-sequence $m_2(t)$ with a generator polynomial defined as $f(x) = x^{18} + x^{10} + x^7 + x^5 + 1$.

A second m-sequence $m_1(t)$ cyclically shifted τ times can be obtained by applying mask functions to the memory values of a shift register generating the original m-sequence.

The embodiments of the present invention provide a generator for concurrently generating multiple gold sequences using the mask functions, and a method for efficiently dividing the set of gold sequences into a primary

also includes the primary scrambling code.. Here, the secondary scrambling codes are generated through application of mask functions to the primary scrambling codes. This method is adapted to a scrambling code group generator of a transmitter as illustrated in Fig. 7, which concurrently generates one primary scrambling code and multiple secondary scrambling codes.

Referring to Fig. 7 , the scrambling code group generator 701 comprises a first m-sequence generator 750 including: an upper shift register memory (hereinafter, referred to as "first shift register memory") 700(with registers 0 to 17) and an adder 730. a second m-sequence generator 760 including; a lower shift register memory (hereinafter, referred to as "second shift register memory") 705 (with registers 0 to 17) and an adder 735, a plurality of masking sections 710 to 712, 714 to 716, a plurality of adders 742 to 744 and 740, and a plurality of delays 722 to 724 and 720. The first shift register memory 700 stores a predetermined register initial value "a_0" and the second shift register memory 705 stores a predetermined register initial value "b_0". The values stored in each of the registers in the memory 700 and the memory 705 may change during every period of an input clock (not shown). The register memory 700 and 705 store 18 bit (or symbol) binary values "a_i" and "b_i", respectively (i = 0 to c-1 where c = the total number of registers in the register memories 700 and 705).

The first m-sequence generator 750 generates a first m-sequece using the register memory 700 and the adder 730 which is a binary adder that adds the binary values from the registers 0 and 7 of the register memory 700 and outputs the sum into the register 17. The register 0 of the register memory 700 sequentially outputs binary values that form the first m-sequence during every period of the input clock. The masking sections 710 to 712 store mask code values(k^1_i to k^N_i) for generating cyclical shifts of the first m-sequence by a predetermined number of chips., The cyclical shifts are achieved by multiplying