# Mueller Exhibit 35

**TSG-RAN Working Group 1 #24** ***Tdoc R1-02-0444***
**Orlando, Florida**
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**Source:** **Siemens, Motorola, Samsung**

**Title:** **Text Proposal for Bit Distribution unit for HS-DSCH**

**Agenda Item:** **AH32 (HSDPA)**

**Document for:** **Discussion and Decision**

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# 1.0 Text Proposal

## *4.5 Coding for HS-DSCH*

Data arrives to the coding/multiplexing unit in form of a maximum of one transport block once every transmission time interval. . The transmission time interval is 2 ms.

The following coding/multiplexing steps can be identified:

- add CRC to each transport block (see subclause 4.5.1);
- code block segmentation (see subclause 4.5.2);
- channel coding (see subclause 4.5.3);
- hybrid ARQ (see subclause 4.5.4);
- Bit Distribution Unit (see subclause 4.5.5);
- physical channel segmentation (see subclause 4.5.6~~5~~);
- interleaving for HS-DSCH (see subclause 4.5.7~~6~~);
- mapping to physical channels (see subclause 4.5.8~~7~~).

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The HS-DSCH always uses one CCTrCH. <Editor's note: to be clarified if this makes sense.>

The coding/multiplexing steps for HS-DSCH is shown in the figure below.

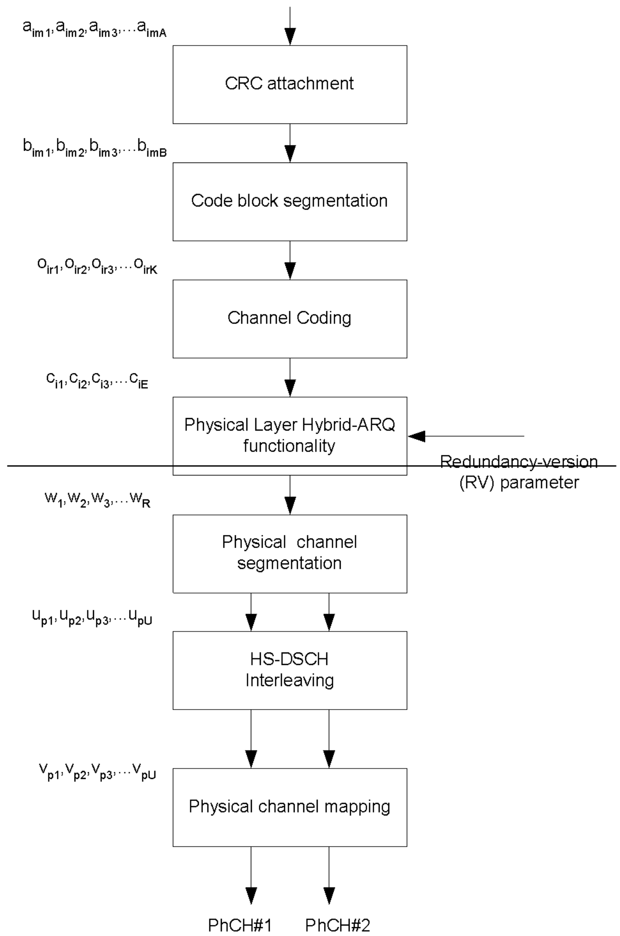
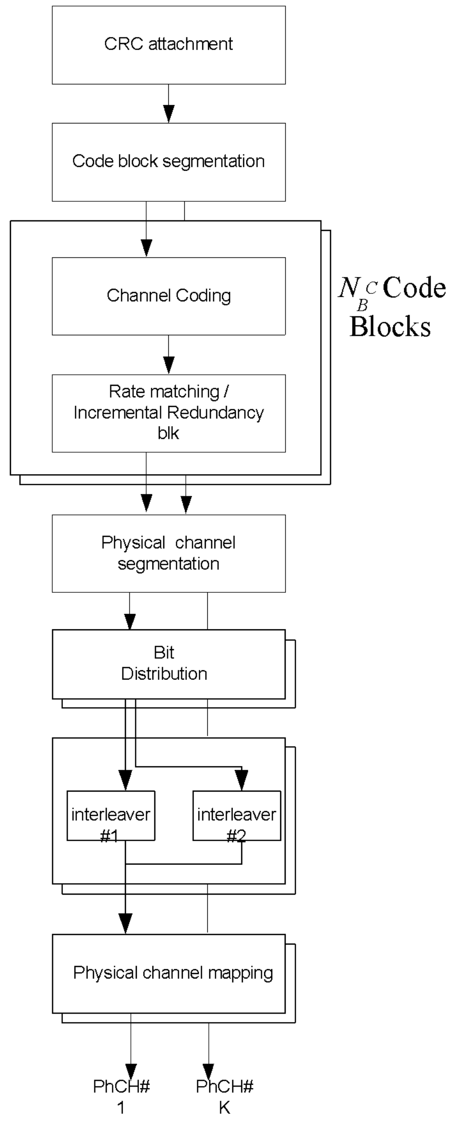



Figure 16 - Transport channel multiplexing structure for HS-DSCH


CRC attachment
Code block segmentation
Channel Coding
Rate matching / Incremental Redundancy blk
$N_B^C$ Code Blocks
Physical channel segmentation
Bit Distribution
interleaver #1
interleaver #2
Physical channel mapping
PhCH# 1
PhCH# K

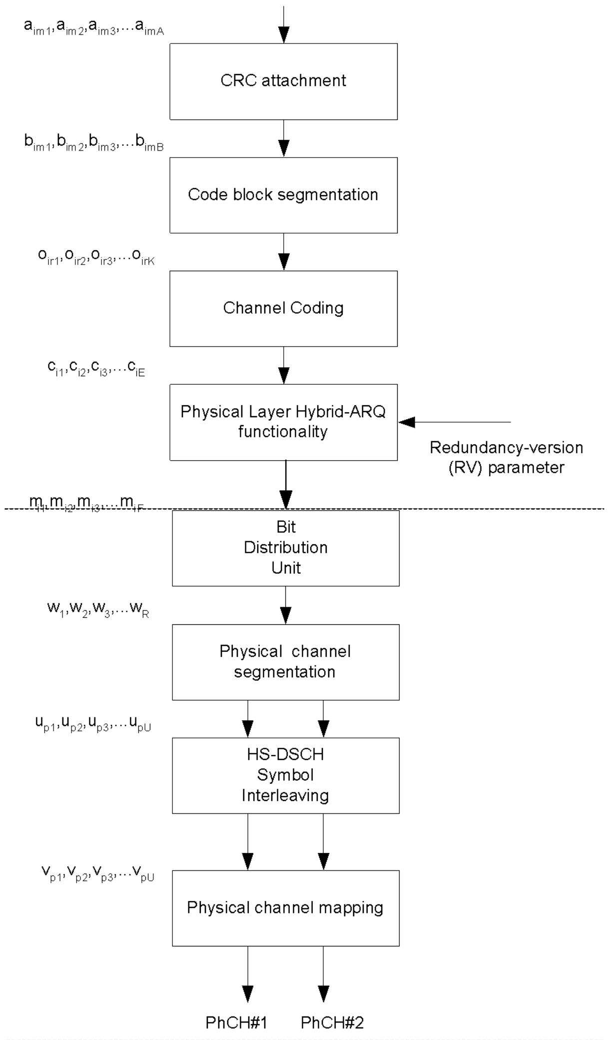



**Figure 17 - Transport channel multiplexing structure for HS-DSCH**

## 4.5.5 Bit Distribution Unit

The Bit Distribution Unit performs priority mapping by ensuring systematic bits are assigned to positions of higher reliability in the constellation during the Physical channel mapping of section 4.5.7. To achieve this an interleaver of size $N_{row} \times N_{col}$ is used. The number of rows and columns are determined from:

$$N_{row} = \log_2(M)$$
$$N_{col} = F / N_{row}$$

where $M$ is the modulation size and $F$ is the number of coded and rate-matched bits to be transmitted. Data is written into the interleaver column by column, and read out of the interleaver column by column. ~~In the first $N_c$ columns, systematic bits are written into row one to $N_r$+1, subsequently they are written into row one to $N_r$.~~

~~where~~ If $N_c$=0, the systematic bits are written into row one to $N_r$ otherwise in the first $N_c$ columns, systematic bits are written into row one to $N_r+1$ and row one to $N_r$ in the remaining $N_c$ columns.

$$N_r = \left\lfloor \frac{N_{t,sys}}{N_{col}} \right\rfloor \text{ and}$$

$$N_c = \left( \frac{N_{t,sys}}{N_{col}} - N_r \right) \cdot N_{col}.$$

$N_{t,sys}$ is the number of transmitted systematic bits. The remaining space is filled with parity bits, again the bits are written column wise into the remaining rows of the respective columns. Parity 1 and 2 bits are written alternatingly.

It may be noted that in case of ~~For~~ 16QAM that for each column the bits are read out of the interleaver in the order row 1, row 3, row 2, row 4. For QPSK the bits are read out of the interleaver in the order row1, row2.