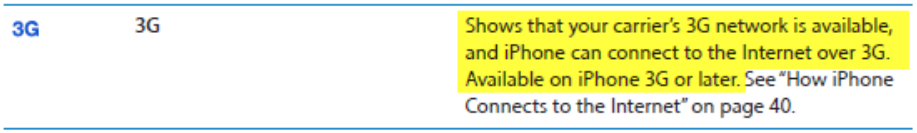
Mueller Exhibit 59

EXHIBIT E

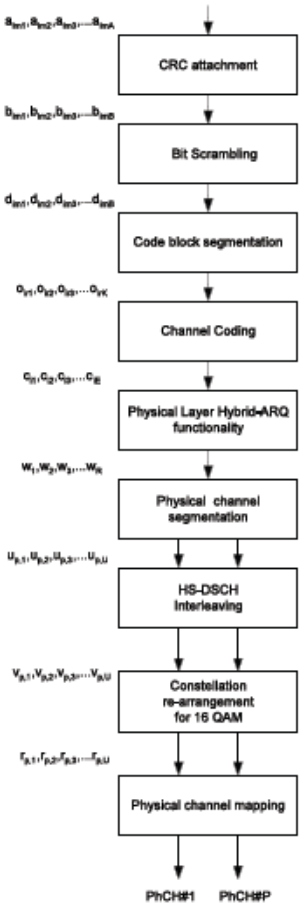
SAMSUNG'S PATENT L.R. 3-1(A)-(D) DISCLOSURES FOR U.S. PATENT NO. 7,200,792

ASSERTED CLAIM (PATENT L.R. 3-1(A))	ACCUSED INSTRUMENTALITY AND HOW EACH ELEMENT IS MET BY ACCUSED INSTRUMENTALITY (PATENT L.R. 3-1(B)-(D))
11. An apparatus for receiving data in a communication system, comprising:	Apple's 3G Products[1] include an apparatus for receiving data in a communication system. *See, e.g.*: Apple iPhone user guide re iOS 3.1: (iPhone 3G or later, p. 21): 

[1] "Apple's 3G Products" include iPhone 3G, iPhone 3GS, iPhone4, iPad 3G, iPad2 3G and any other products compliant with 3GPP UMTS standard.

	http://www.apple.com/iphone/specs.html (iPhone 4) **Cellular and wireless** ■ GSM model: UMTS/HSDPA/HSUPA (850, 900, 1900, 2100 MHz); GSM/EDGE (850, 900, 1800, 1900 MHz) ■ CDMA model: CDMA EV-DO Rev. A (800, 1900 MHz) ■ 802.11b/g/n Wi-Fi (802.11n 2.4GHz only) ■ Bluetooth 2.1 + EDR wireless technology **Location** ■ Assisted GPS ■ Digital compass ■ Wi-Fi ■ Cellular

	iPad iOS 3.2 user guide: (iPad) **Cellular Data** Use Cellular Data settings (on iPad Wi-Fi + 3G only) to turn Data Roaming on or off, change your account information, or add a Personal Identification Number (PIN) to lock the micro-SIM card. **Turn the cellular data network on or off:** Choose Cellular Data, then turn Cellular Data on or off. **Turn data roaming on or off:** Choose Data Roaming, then turn data roaming on or off. **View your account information:** To see or change your account information, tap View Account. **Chapter 17** Settings http://www.apple.com/ipad/specs/ (iPad 2) 

[a] a demodulator for demodulating a received symbol into a plurality of systematic bits and parity bits;	Apple's 3G Products include a demodulator for demodulating a received symbol into a plurality of systematic bits and parity bits. The 3GPP Technical Specification 25.212 v6.0.0 ("TS 25.212 v6.0.0") describe a turbo encoder for coding data bits to generate systematic bits and parity bits. The coded data bits are received by Apple's 3G products and decoded. *See, e.g.*, TS 25.212 v6.0.0 §4.5:  **Figure 16: Coding chain for HS-DSCH**

TS 25.212 v6.0.0. § 4.5.3:

4.5.3 Channel coding for HS-DSCH

Channel coding for the HS-DSCH transport channel shall be done with the general method described in 4.2.3 above with the following specific parameters.

There will be a maximum of one transport block, i=1. The rate 1/3 turbo coding shall be used.

TS 25.212 v6.0.0 § 4.5.7 and Figure 17:

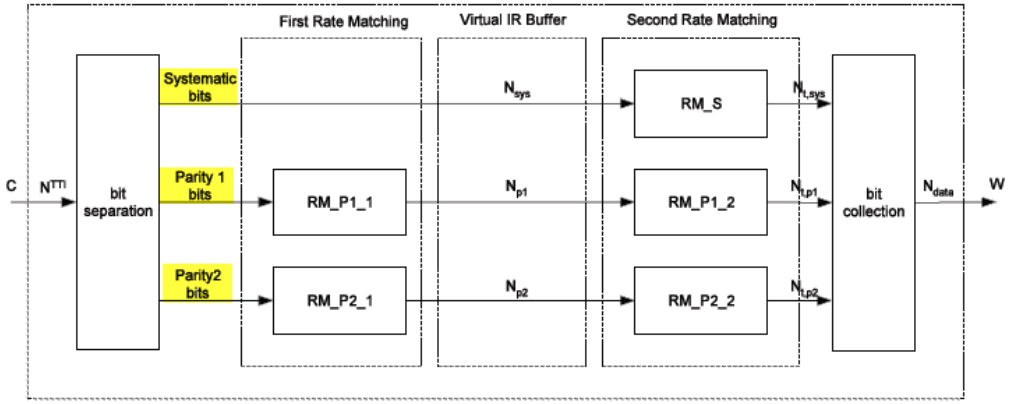


Figure 17: HS-DSCH hybrid ARQ functionality

4.5.4.1 HARQ bit separation

The HARQ bit separation function shall be performed in the same way as bit separation for turbo encoded TrCHs in 4.2.7.4 above.

TS 25.212 v6.0.0 § 4.2.3:

4.2.3 Channel coding

Code blocks are delivered to the channel coding block. They are denoted by $o_{ir1}, o_{ir2}, o_{ir3}, \ldots, o_{irK_i}$, where i is the TrCH number, r is the code block number, and K_i is the number of bits in each code block. The number of code blocks on TrCH i is denoted by C_i. After encoding the bits are denoted by $y_{ir1}, y_{ir2}, y_{ir3}, \ldots, y_{irY_i}$, where Y_i is the number of encoded bits. The relation between o_{irk} and y_{irk} and between K_i and Y_i is dependent on the channel coding scheme.

The following channel coding schemes can be applied to TrCHs:

- convolutional coding;
- turbo coding.

Usage of coding scheme and coding rate for the different types of TrCH is shown in table 1.

The values of Y_i in connection with each coding scheme:

- convolutional coding with rate 1/2: $Y_i = 2*K_i + 16$; rate 1/3: $Y_i = 3*K_i + 24$;
- turbo coding with rate 1/3: $Y_i = 3*K_i + 12$.

Table 1: Usage of channel coding scheme and coding rate

Type of TrCH	Coding scheme	Coding rate
BCH	Convolutional coding	1/2
PCH		
RACH		
CPCH, DCH, DSCH, FACH		1/3, 1/2
	Turbo coding	1/3

TS 25.212 v6.0.0 § 4.2.3.2, Figure 4:

4.2.3.2 Turbo coding

4.2.3.2.1 Turbo coder

The scheme of Turbo coder is a Parallel Concatenated Convolutional Code (PCCC) with two 8-state constituent encoders and one Turbo code internal interleaver. The coding rate of Turbo coder is 1/3. The structure of Turbo coder is illustrated in figure 4.

The transfer function of the 8-state constituent code for PCCC is:

$$G(D) = \left[1, \frac{g_1(D)}{g_0(D)}\right],$$

where

$$g_0(D) = 1 + D^2 + D^3,$$

$$g_1(D) = 1 + D + D^3.$$

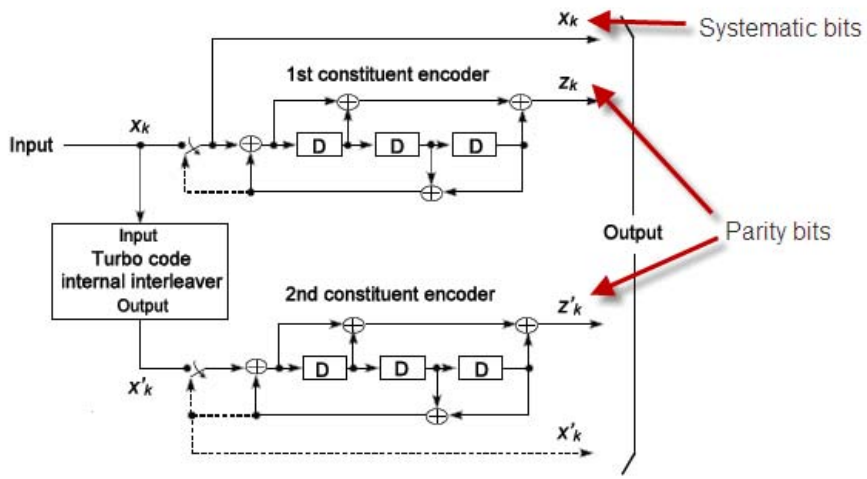
The initial value of the shift registers of the 8-state constituent encoders shall be all zeros when starting to encode the input bits.

Output from the Turbo coder is

$$x_1, z_1, z'_1, x_2, z_2, z'_2, \ldots, x_K, z_K, z'_K,$$

where $x_1, x_2, \ldots, x_K$ are the bits input to the Turbo coder i.e. both first 8-state constituent encoder and Turbo code internal interleaver, and K is the number of bits, and $z_1, z_2, \ldots, z_K$ and $z'_1, z'_2, \ldots, z'_K$ are the bits output from first and second 8-state constituent encoders, respectively.

The bits output from Turbo code internal interleaver are denoted by $x'_1, x'_2, \ldots, x'_K$, and these bits are to be input to the second 8-state constituent encoder.

	 **Figure 4: Structure of rate 1/3 Turbo coder (dotted lines apply for trellis termination only)**
[b] a first deinterleaver for writing the plurality of systematic bits on a column by column basis and performing inter-column permutation;	Apple's 3G Products include a first deinterleaver for writing the plurality of systematic bits on a column by column basis and performing inter-column permutation. *See, e.g.*,

TS 25.212 v6.0.0 § 4.5.4.4:

4.5.4.4 HARQ bit collection

The HARQ bit collection is achieved using a rectangular interleaver of size $N_{row} \times N_{col}$.

The number of rows and columns are determined from:

$$N_{row} = 4 \text{ for 16QAM and } N_{row} = 2 \text{ for QPSK}$$

$$N_{col} = N_{data} / N_{row}$$

where N_{data} is used as defined in 4.5.4.3.

Data is written into the interleaver column by column, and read out of the interleaver column by column starting from the first column.

$N_{t,sys}$ is the number of transmitted systematic bits. Intermediate values N_r and N_c are calculated using:

$$N_r = \left\lfloor \frac{N_{t,sys}}{N_{col}} \right\rfloor \text{ and } N_c = N_{t,sys} - N_r \cdot N_{col}.$$

If N_c=0 and N_r > 0, the systematic bits are written into rows 1…N_r.

Otherwise systematic bits are written into rows 1…N_r+1 in the first N_c columns and, if N_r > 0, also into rows 1…N_r in the remaining N_{col}-N_c columns.

The remaining space is filled with parity bits. The parity bits are written column wise into the remaining rows of the respective columns. Parity 1 and 2 bits are written in alternating order, starting with a parity 2 bit in the first available column with the lowest index number.

In the case of 16QAM for each column the bits are read out of the interleaver in the order row 1, row 2, row 3, row 4. In the case of QPSK for each column the bits are read out of the interleaver in the order row1, row2.

TS 25.212 v6.0.0 § 4.5.5:

4.5.5 Physical channel segmentation for HS-DSCH

When more than one HS-PDSCH is used, physical channel segmentation divides the bits among the different physical channels. The bits input to the physical channel segmentation are denoted by $w_1, w_2, w_3, \ldots w_R$, where R is the number of bits input to the physical channel segmentation block. The number of PhCHs is denoted by P.

The bits after physical channel segmentation are denoted $u_{p1}, u_{p2}, u_{p3}, \ldots, u_{pU}$, where p is PhCH number and U is the number of bits in one radio sub-frame for each HS-PDSCH, i.e. $U = \frac{R}{P}$. The relation between w_k and $u_{p,k}$ is given below.

For all modes, some bits of the input flow are mapped to each code until the number of bits on the code is U.

Bits on first PhCH after physical channel segmentation:

$u_{1,k} = w_k \quad k = 1, 2, \ldots, U$

Bits on second PhCH after physical channel segmentation:

$u_{2,k} = w_{k+U} \quad k = 1, 2, \ldots, U$

…

Bits on the P^{th} PhCH after physical channel segmentation:

$u_{P,k} = w_{k+(P-1)\cdot U} \quad k = 1, 2, \ldots, U$

TS 25.212 v6.0.0 § 4.5.6, Figure 18:

4.5.6 Interleaving for HS-DSCH

The interleaving for FDD is done as shown in figure 18 below, separately for each physical channel. The bits input to the block interleaver are denoted by $u_{p,1}, u_{p,2}, u_{p,3}, \ldots, u_{p,U}$, where p is PhCH number and U is the number of bits in one TTI for one PhCH. For QPSK $U = 960$ and for 16QAM $U = 1920$. The basic interleaver is as the 2nd interleaver described in Section 4.2.11. The interleaver is of fixed size: R2=32 rows and C2=30 columns.

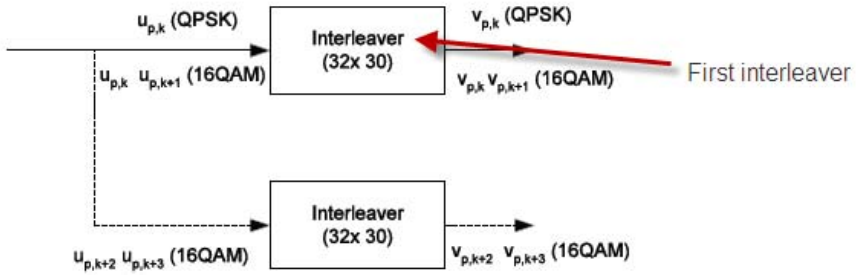


Figure 18: Interleaver structure for HS-DSCH

For 16QAM, there are two identical interleavers of the same fixed size R2×C2 = 32×30. The output bits from the physical channel segmentation are divided two by two between the interleavers: bits $u_{p,k}$ and $u_{p,k+1}$ go to the first interleaver and bits $u_{p,k+2}$ and $u_{p,k+3}$ go to the second interleaver. Bits are collected two by two from the interleavers: bits $v_{p,k}$ and $v_{p,k+1}$ are obtained from the first interleaver and bits $v_{p,k+2}$ and $v_{p,k+3}$ are obtained from the second interleaver, where k mod 4=1.

TS 25.212 v6.0.0 §4.2.11:

4.2.11 2nd interleaving

The 2nd interleaving is a block interleaver and consists of bits input to a matrix with padding, the inter-column permutation for the matrix and bits output from the matrix with pruning. The bits input to the block interleaver are denoted by $u_{p,1}, u_{p,2}, u_{p,3}, \ldots, u_{p,U}$, where p is PhCH number and U is the number of bits in one radio frame for one PhCH. The output bit sequence from the block interleaver is derived as follows:

…

(3) Write the input bit sequence $u_{p,1}, u_{p,2}, u_{p,3}, \ldots, u_{p,U}$ into the R2 × C2 matrix row by row starting with bit $y_{p,1}$ in column 0 of row 0:

$$\begin{bmatrix} y_{p,1} & y_{p,2} & y_{p,3} & \cdots & y_{p,C2} \\ y_{p,(C2+1)} & y_{p,(C2+2)} & y_{p,(C2+3)} & \cdots & y_{p,(2\times C2)} \\ \vdots & \vdots & \vdots & \cdots & \vdots \\ y_{p,((R2-1)\times C2+1)} & y_{p,((R2-1)\times C2+2)} & y_{p,((R2-1)\times C2+3)} & \cdots & y_{p,(R2\times C2)} \end{bmatrix}$$

where $y_{p,k} = u_{p,k}$ for $k = 1, 2, \ldots, U$ and if $R2 \times C2 > U$, the dummy bits are padded such that $y_{p,k} = 0$ or 1 for $k = U+1, U+2, \ldots, R2 \times C2$. These dummy bits are pruned away from the output of the matrix after the inter-column permutation.

(4) Perform the inter-column permutation for the matrix based on the pattern $\langle P2(j) \rangle_{j \in \{0,1,\ldots,C2-1\}}$ that is shown in table 7, where $P2(j)$ is the original column position of the j-th permuted column. After permutation of the columns, the bits are denoted by $y'_{p,k}$.

$$\begin{bmatrix} y'_{p,1} & y'_{p,(R2+1)} & y'_{p,(2\times R2+1)} & \cdots & y'_{p,((C2-1)\times R2+1)} \\ y'_{p,2} & y'_{p,(R2+2)} & y'_{p,(2\times R2+2)} & \cdots & y'_{p,((C2-1)\times R2+2)} \\ \vdots & \vdots & \vdots & \cdots & \vdots \\ y'_{p,R2} & y'_{p,(2\times R2)} & y'_{p,(3\times R2)} & \cdots & y'_{p,(C2\times R2)} \end{bmatrix}$$

(5) The output of the block interleaver is the bit sequence read out column by column from the inter-column permuted R2 × C2 matrix. The output is pruned by deleting dummy bits that were padded to the input of the matrix before the inter-column permutation, i.e. bits $y'_{p,k}$ that corresponds to bits $y_{p,k}$ with $k > U$ are removed from the output. The bits after 2nd interleaving are denoted by $v_{p,1}, v_{p,2}, \ldots, v_{p,U}$, where $v_{p,1}$ corresponds to the bit $y'_{p,k}$ with smallest index k after pruning, $v_{p,2}$ to the bit $y'_{p,k}$ with second smallest index k after pruning, and so on.

Table 7 Inter-column permutation pattern for 2nd interleaving

Number of columns C2	Inter-column permutation pattern < P2(0), P2(1), ..., P2(C2-1) >
30	<0, 20, 10, 5, 15, 25, 3, 13, 23, 8, 18, 28, 1, 11, 21, 6, 16, 26, 4, 14, 24, 19, 9, 29, 12, 2, 7, 22, 27, 17>

[c] a second deinterleaver for writing the plurality of parity bits on a column by column basis and performing inter-column permutation;	Apple's 3G Products include a second deinterleaver for writing the plurality of parity bits on a column-by-column basis, and performing inter-column permutation. *See*, *e.g.*, TS 25.212 v6.0.0 § 4.5.4.4: **4.5.4.4 HARQ bit collection** The HARQ bit collection is achieved using a rectangular interleaver of size $N_{row} \times N_{col}$. The number of rows and columns are determined from: $N_{row} = 4$ for 16QAM and $N_{row} = 2$ for QPSK $N_{col} = N_{data} / N_{row}$ where N_{data} is used as defined in 4.5.4.3.

Data is written into the interleaver column by column, and read out of the interleaver column by column starting from the first column.

$N_{t,sys}$ is the number of transmitted systematic bits. Intermediate values N_r and N_c are calculated using:

$$N_r = \left\lfloor \frac{N_{t,sys}}{N_{col}} \right\rfloor \text{ and } N_c = N_{t,sys} - N_r \cdot N_{col} .$$

If N_c=0 and N_r > 0, the systematic bits are written into rows 1…N_r.

Otherwise systematic bits are written into rows 1…N_r+*1* in the first N_c columns and, if N_r > 0, also into rows 1…N_r in the remaining N_{col}-N_c columns.

The remaining space is filled with parity bits. The parity bits are written column wise into the remaining rows of the respective columns. Parity 1 and 2 bits are written in alternating order, starting with a parity 2 bit in the first available column with the lowest index number.

In the case of 16QAM for each column the bits are read out of the interleaver in the order row 1, row 2, row 3, row 4. In the case of QPSK for each column the bits are read out of the interleaver in the order row1, row2.

TS 25.212 v6.0.0 § 4.5.5:

4.5.5 Physical channel segmentation for HS-DSCH

When more than one HS-PDSCH is used, physical channel segmentation divides the bits among the different physical channels. The bits input to the physical channel segmentation are denoted by $w_1, w_2, w_3, \ldots w_R$, where R is the number of bits input to the physical channel segmentation block. The number of PhCHs is denoted by P.

The bits after physical channel segmentation are denoted $u_{p1}, u_{p2}, u_{p3}, \ldots, u_{pU}$, where p is PhCH number and U is the number of bits in one radio sub-frame for each HS-PDSCH, i.e. $U = \frac{R}{P}$. The relation between w_k and $u_{p,k}$ is given below.

For all modes, some bits of the input flow are mapped to each code until the number of bits on the code is U.

Bits on first PhCH after physical channel segmentation:

$u_{1,k} = w_k \quad k = 1, 2, \ldots, U$

Bits on second PhCH after physical channel segmentation:

$u_{2,k} = w_{k+U} \quad k = 1, 2, \ldots, U$

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Bits on the P^{th} PhCH after physical channel segmentation:

$u_{P,k} = w_{k+(P-1)\cdot U} \quad k = 1, 2, \ldots, U$

TS 25.212 v6.0.0 § 4.5.6, Figure 18:

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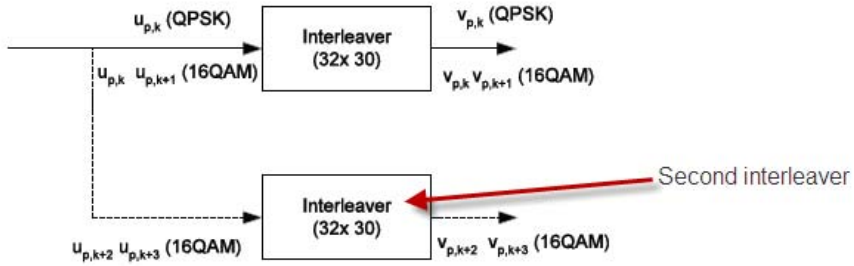

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TS 25.212 v6.0.0 §4.2.11:

4.2.11 2nd interleaving

The 2nd interleaving is a block interleaver and consists of bits input to a matrix with padding, the inter-column permutation for the matrix and bits output from the matrix with pruning. The bits input to the block interleaver are denoted by $u_{p,1}, u_{p,2}, u_{p,3}, \ldots, u_{p,U}$, where p is PhCH number and U is the number of bits in one radio frame for one PhCH. The output bit sequence from the block interleaver is derived as follows:

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(3) Write the input bit sequence $u_{p,1}, u_{p,2}, u_{p,3}, \ldots, u_{p,U}$ into the R2 × C2 matrix row by row starting with bit $y_{p,1}$ in column 0 of row 0:

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where $y_{p,k} = u_{p,k}$ for $k = 1, 2, \ldots, U$ and if $R2 \times C2 > U$, the dummy bits are padded such that $y_{p,k} = 0$ or 1 for $k = U+1, U+2, \ldots, R2 \times C2$. These dummy bits are pruned away from the output of the matrix after the inter-column permutation.

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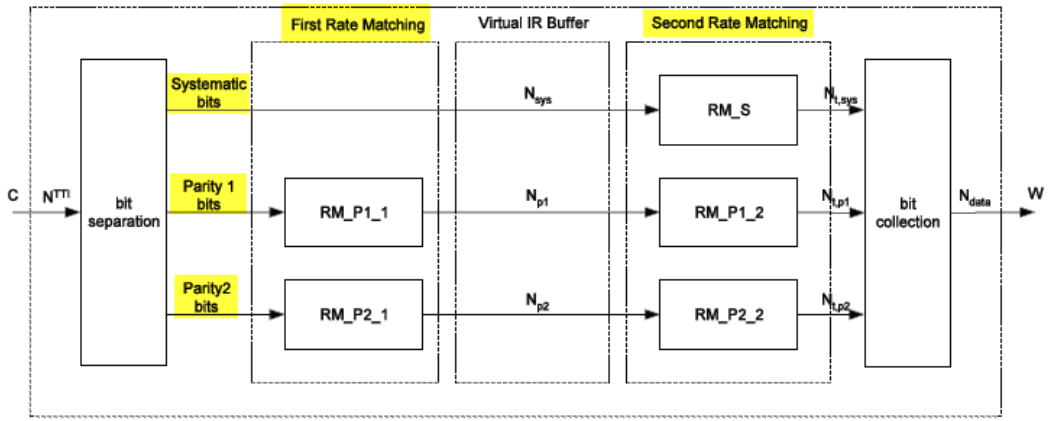
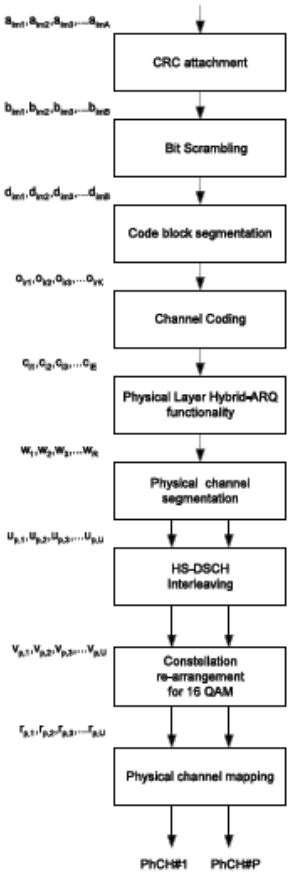
$$\begin{bmatrix} y'_{p,1} & y'_{p,(R2+1)} & y'_{p,(2\times R2+1)} & \cdots & y'_{p,((C2-1)\times R2+1)} \\ y'_{p,2} & y'_{p,(R2+2)} & y'_{p,(2\times R2+2)} & \cdots & y'_{p,((C2-1)\times R2+2)} \\ \vdots & \vdots & \vdots & \cdots & \vdots \\ y'_{p,R2} & y'_{p,(2\times R2)} & y'_{p,(3\times R2)} & \cdots & y'_{p,(C2\times R2)} \end{bmatrix}$$

(5) The output of the block interleaver is the bit sequence read out column by column from the inter-column permuted R2 × C2 matrix. The output is pruned by deleting dummy bits that were padded to the input of the matrix before the inter-column permutation, i.e. bits $y'_{p,k}$ that corresponds to bits $y_{p,k}$ with $k > U$ are removed from the output. The bits after 2nd interleaving are denoted by $v_{p,1}, v_{p,2}, \ldots, v_{p,U}$, where $v_{p,1}$ corresponds to the bit $y'_{p,k}$ with smallest index k after pruning, $v_{p,2}$ to the bit $y'_{p,k}$ with second smallest index k after pruning, and so on.

Table 7 Inter-column permutation pattern for 2nd interleaving

Number of columns C2	Inter-column permutation pattern < P2(0), P2(1), ..., P2(C2-1) >
30	<0, 20, 10, 5, 15, 25, 3, 13, 23, 8, 18, 28, 1, 11, 21, 6, 16, 26, 4, 14, 24, 19, 9, 29, 12, 2, 7, 22, 27, 17>

[d] a rate matcher for rate matching the de-interleaved systematic bits and parity bits; and	Apple's 3G Products include a rate matcher for rate matching the de-interleaved systematic bits and parity bits. *See, e.g.*, TS 25.212 v6.0.0. § 4.5.4 and Figure 17: 4.5.4 Hybrid ARQ for HS-DSCH The hybrid ARQ functionality matches the number of bits at the output of the channel coder to the total number of bits of the HS-PDSCH set to which the HS-DSCH is mapped. The hybrid ARQ functionality is controlled by the redundancy version (RV) parameters. The exact set of bits at the output of the hybrid ARQ functionality depends on the number of input bits, the number of output bits, and the RV parameters. The hybrid ARQ functionality consists of two rate-matching stages and a virtual buffer as shown in the figure below. The first rate matching stage matches the number of input bits to the virtual IR buffer, information about which is provided by higher layers. Note that, if the number of input bits does not exceed the virtual IR buffering capability, the first rate-matching stage is transparent. The second rate matching stage matches the number of bits after first rate matching stage to the number of physical channel bits available in the HS-PDSCH set in the TTI.  **Figure 17: HS-DSCH hybrid ARQ functionality**

[e] a decoder for decoding the rate matched systematic bits and parity bits,	Apple's 3G Products include a decoder for decoding the rate matched systematic bits and parity bits. TS 25.212 v6.0.0 discloses a turbo encoder for coding data bits to generate systematic bits and parity bits. *See, e.g.,* 3GPP Technical Specification 25.212 v6.0.0 ("TS 25.212 v6.0.0") §4.5:  **Figure 16: Coding chain for HS-DSCH**

TS 25.212 v6.0.0. § 4.5.3:

4.5.3 Channel coding for HS-DSCH

Channel coding for the HS-DSCH transport channel shall be done with the general method described in 4.2.3 above with the following specific parameters.

There will be a maximum of one transport block, i=1. The rate 1/3 turbo coding shall be used.

TS 25.212 v6.0.0 § 4.5.7 and Figure 17:

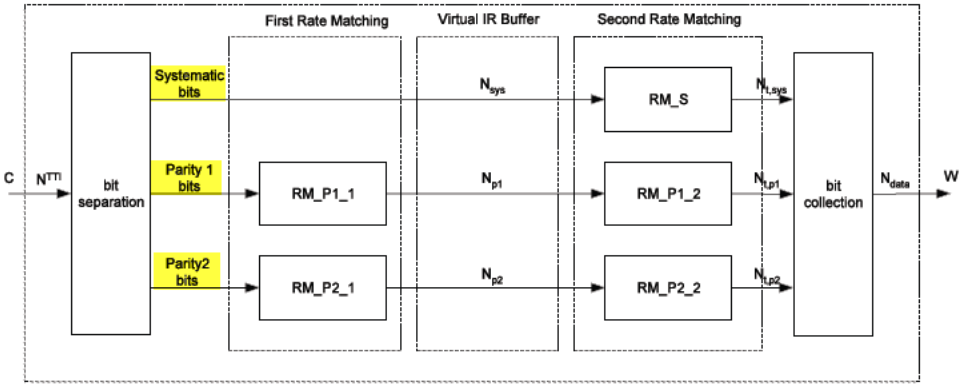


Figure 17: HS-DSCH hybrid ARQ functionality

4.5.4.1 HARQ bit separation

The HARQ bit separation function shall be performed in the same way as bit separation for turbo encoded TrCHs in 4.2.7.4 above.

TS 25.212 v6.0.0 § 4.2.3:

4.2.3 Channel coding

Code blocks are delivered to the channel coding block. They are denoted by $o_{ir1}, o_{ir2}, o_{ir3}, \ldots, o_{irK_i}$, where i is the TrCH number, r is the code block number, and K_i is the number of bits in each code block. The number of code blocks on TrCH i is denoted by C_i. After encoding the bits are denoted by $y_{ir1}, y_{ir2}, y_{ir3}, \ldots, y_{irY_i}$, where Y_i is the number of encoded bits. The relation between o_{irk} and y_{irk} and between K_i and Y_i is dependent on the channel coding scheme.

The following channel coding schemes can be applied to TrCHs:

- convolutional coding;
- turbo coding.

Usage of coding scheme and coding rate for the different types of TrCH is shown in table 1.

The values of Y_i in connection with each coding scheme:

- convolutional coding with rate 1/2: $Y_i = 2*K_i + 16$; rate 1/3: $Y_i = 3*K_i + 24$;
- turbo coding with rate 1/3: $Y_i = 3*K_i + 12$.

Table 1: Usage of channel coding scheme and coding rate

Type of TrCH	Coding scheme	Coding rate
BCH	Convolutional coding	1/2
PCH		
RACH		
CPCH, DCH, DSCH, FACH		1/3, 1/2
	Turbo coding	1/3

TS 25.212 v6.0.0 § 4.2.3.2, Figure 4:

4.2.3.2 Turbo coding

4.2.3.2.1 Turbo coder

The scheme of Turbo coder is a Parallel Concatenated Convolutional Code (PCCC) with two 8-state constituent encoders and one Turbo code internal interleaver. The coding rate of Turbo coder is 1/3. The structure of Turbo coder is illustrated in figure 4.

The transfer function of the 8-state constituent code for PCCC is:

$$G(D) = \left[1, \frac{g_1(D)}{g_0(D)}\right],$$

where

$$g_0(D) = 1 + D^2 + D^3,$$

$$g_1(D) = 1 + D + D^3.$$

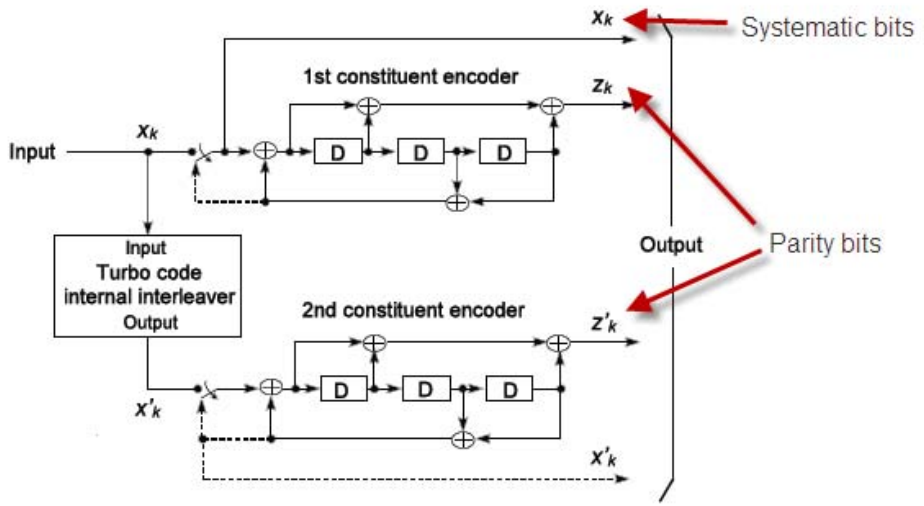
The initial value of the shift registers of the 8-state constituent encoders shall be all zeros when starting to encode the input bits.

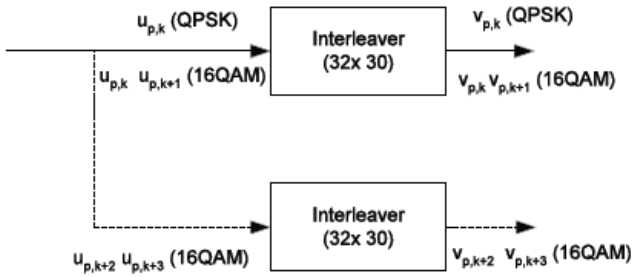
Output from the Turbo coder is

$$x_1, z_1, z'_1, x_2, z_2, z'_2, \ldots, x_K, z_K, z'_K,$$

where $x_1, x_2, \ldots, x_K$ are the bits input to the Turbo coder i.e. both first 8-state constituent encoder and Turbo code internal interleaver, and K is the number of bits, and $z_1, z_2, \ldots, z_K$ and $z'_1, z'_2, \ldots, z'_K$ are the bits output from first and second 8-state constituent encoders, respectively.

The bits output from Turbo code internal interleaver are denoted by $x'_1, x'_2, \ldots, x'_K$, and these bits are to be input to the second 8-state constituent encoder.

	 **Figure 4: Structure of rate 1/3 Turbo coder (dotted lines apply for trellis termination only)**
[f] wherein a size of the first deinterleaver is equal to a size of the second deinterleaver.	Apple's 3G Products include a first deinterleaver equal in size to the second deinterleaver. *See, e.g.,* TS 25.212 v6.0.0 §4.5.6, Figure 18: **4.5.6 Interleaving for HS-DSCH** The interleaving for FDD is done as shown in figure 18 below, separately for each physical channel. The bits input to the block interleaver are denoted by $u_{p,1}, u_{p,2}, u_{p,3}, \ldots, u_{p,U}$, where p is PhCH number and U is the number of bits in one TTI for one PhCH. For QPSK $U = 960$ and for 16QAM $U = 1920$. The basic interleaver is as the 2nd interleaver described in Section 4.2.11. The interleaver is of fixed size: R2=32 rows and C2=30 columns.

	 **Figure 18: Interleaver structure for HS-DSCH** For 16QAM, there are two identical interleavers of the same fixed size R2×C2 = 32×30. The output bits from the physical channel segmentation are divided two by two between the interleavers: bits $u_{p,k}$ and $u_{p,k+1}$ go to the first interleaver and bits $u_{p,k+2}$ and $u_{p,k+3}$ go to the second interleaver. Bits are collected two by two from the interleavers: bits $v_{p,k}$ and $v_{p,k+1}$ are obtained from the first interleaver and bits $v_{p,k+2}$ and $v_{p,k+3}$ are obtained from the second interleaver, where k mod 4=1.
12. The apparatus of claim 11,	See claim 11.
wherein if a number of the systematic bits is less than a number of the parity bits, part of the parity bits is written next to systematic bits in the first deinterleaver.	Apple's 3G Products include part of the parity bits written next to the systematic bits in the first deinterleaver if a number of the systematic bits is less than a number of the parity bits. *See, e.g.*,

	TS 25.212 v6.0.0 § 4.5.4.4: **4.5.4.4 HARQ bit collection** The HARQ bit collection is achieved using a rectangular interleaver of size $N_{row} \times N_{col}$. The number of rows and columns are determined from: $N_{row} = 4$ for 16QAM and $N_{row} = 2$ for QPSK $N_{col} = N_{data} / N_{row}$ where N_{data} is used as defined in 4.5.4.3.

Data is written into the interleaver column by column, and read out of the interleaver column by column starting from the first column.

$N_{t,sys}$ is the number of transmitted systematic bits. Intermediate values N_r and N_c are calculated using:

$$N_r = \left\lfloor \frac{N_{t,sys}}{N_{col}} \right\rfloor \quad \text{and} \quad N_c = N_{t,sys} - N_r \cdot N_{col} .$$

If N_c=0 and N_r > 0, the systematic bits are written into rows 1…N_r.

Otherwise systematic bits are written into rows 1…N_r+1 in the first N_c columns and, if N_r > 0, also into rows 1…N_r in the remaining N_{col}-N_c columns.

The remaining space is filled with parity bits. The parity bits are written column wise into the remaining rows of the respective columns. Parity 1 and 2 bits are written in alternating order, starting with a parity 2 bit in the first available column with the lowest index number.

In the case of 16QAM for each column the bits are read out of the interleaver in the order row 1, row 2, row 3, row 4. In the case of QPSK for each column the bits are read out of the interleaver in the order row1, row2.

TS 25.212 v6.0.0 § 4.5.5:

4.5.5 Physical channel segmentation for HS-DSCH

When more than one HS-PDSCH is used, physical channel segmentation divides the bits among the different physical channels. The bits input to the physical channel segmentation are denoted by $w_1, w_2, w_3, \ldots w_R$, where R is the number of bits input to the physical channel segmentation block. The number of PhCHs is denoted by P.

The bits after physical channel segmentation are denoted $u_{p1}, u_{p2}, u_{p3}, \ldots, u_{pU}$, where p is PhCH number and U is the number of bits in one radio sub-frame for each HS-PDSCH, i.e. $U = \frac{R}{P}$. The relation between w_k and $u_{p,k}$ is given below.

For all modes, some bits of the input flow are mapped to each code until the number of bits on the code is U.

Bits on first PhCH after physical channel segmentation:

$u_{1,k} = w_k \quad k = 1, 2, \ldots, U$

Bits on second PhCH after physical channel segmentation:

$u_{2,k} = w_{k+U} \quad k = 1, 2, \ldots, U$

...

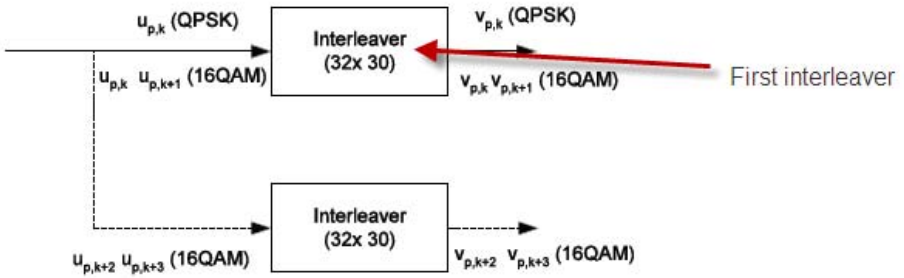
Bits on the P^{th} PhCH after physical channel segmentation:

$u_{P,k} = w_{k+(P-1)\cdot U} \quad k = 1, 2, \ldots, U$

TS 25.212 v6.0.0 § 4.5.6, Figure 18:

4.5.6 Interleaving for HS-DSCH

The interleaving for FDD is done as shown in figure 18 below, separately for each physical channel. The bits input to the block interleaver are denoted by $u_{p,1}, u_{p,2}, u_{p,3}, \ldots, u_{p,U}$, where p is PhCH number and U is the number of bits in one TTI for one PhCH. For QPSK $U = 960$ and for 16QAM $U = 1920$. The basic interleaver is as the 2nd interleaver described in Section 4.2.11. The interleaver is of fixed size: R2=32 rows and C2=30 columns.

	 **Figure 18: Interleaver structure for HS-DSCH** For 16QAM, there are two identical interleavers of the same fixed size R2×C2 = 32×30. The output bits from the physical channel segmentation are divided two by two between the interleavers: bits $u_{p,k}$ and $u_{p,k+1}$ go to the first interleaver and bits $u_{p,k+2}$ and $u_{p,k+3}$ go to the second interleaver. Bits are collected two by two from the interleavers: bits $v_{p,k}$ and $v_{p,k+1}$are obtained from the first interleaver and bits $v_{p,k+2}$ and $v_{p,k+3}$ are obtained from the second interleaver, where k mod 4=1.
13. The apparatus of claim 11,	See claim 11.
wherein if a number of the systematic bits is greater than a number of the parity bits, part of the systematic bits is written prior to the parity bits in the second deinterleaver.	Apple's 3G Products include part of the systematic bits written prior to the parity bits in the second deinterleaver if a number of the systematic bits is greater than a number of the parity bits. *See, e.g.*, TS 25.212 v6.0.0 § 4.5.4.4:

4.5.4.4 HARQ bit collection

The HARQ bit collection is achieved using a rectangular interleaver of size $N_{row} \times N_{col}$.

The number of rows and columns are determined from:

$$N_{row} = 4 \quad \text{for 16QAM and} \quad N_{row} = 2 \quad \text{for QPSK}$$

$$N_{col} = N_{data} / N_{row}$$

where N_{data} is used as defined in 4.5.4.3.

Data is written into the interleaver column by column, and read out of the interleaver column by column starting from the first column.

$N_{t,sys}$ is the number of transmitted systematic bits. Intermediate values N_r and N_c are calculated using:

$$N_r = \left\lfloor \frac{N_{t,sys}}{N_{col}} \right\rfloor \quad \text{and} \quad N_c = N_{t,sys} - N_r \cdot N_{col}.$$

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TS 25.212 v6.0.0 § 4.5.5:

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...

Bits on the P^{th} PhCH after physical channel segmentation:

$u_{P,k} = w_{k+(P-1)\cdot U} \quad k = 1, 2, \ldots, U$

TS 25.212 v6.0.0 § 4.5.6, Figure 18:

4.5.6 Interleaving for HS-DSCH

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	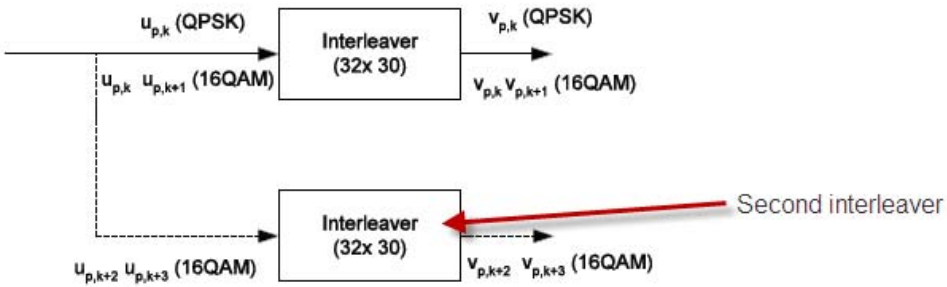 **Figure 18: Interleaver structure for HS-DSCH** For 16QAM, there are two identical interleavers of the same fixed size R2×C2 = 32×30. The output bits from the physical channel segmentation are divided two by two between the interleavers: bits $u_{p,k}$ and $u_{p,k+1}$ go to the first interleaver and bits $u_{p,k+2}$ and $u_{p,k+3}$ go to the second interleaver. Bits are collected two by two from the interleavers: bits $v_{p,k}$ and $v_{p,k+1}$are obtained from the first interleaver and bits $v_{p,k+2}$ and $v_{p,k+3}$ are obtained from the second interleaver, where k mod 4=1.
14. A method for receiving data in a communication system, comprising:	*See* claim 11. Apple infringes this claim because it has performed each and every step of this claim, including but not limited to through testing and use by its employees. Apple also infringes this claim by selling Apple's 3G Products to customers and encouraging those customers to use the products in a manner that meets each and every step of this claim.
demodulating a received symbol into a plurality of systematic bits and parity bits;	*See* claim 11[a].
writing the plurality of systematic bits on a column by column basis in a first deinterleaver and performing inter-column permutation, and writing the plurality of parity bits on a column by column basis in a second deinterleaver and performing	*See* claim 11[b] and 11[c].

inter-column permutation;	
rate marching the de-interleaved systematic bits and parity bits; and	*See* claim 11[d].
decoding the rate matched systematic bits and parity bits,	*See* claim 11[e].
wherein a size of the first deinterleaver is equal to a size of the second deinterleaver.	*See* claim 11[f].
15. The method of claim 14,	*See* claim 14.
wherein if a number of the systematic bits is less than a number of the parity bits, part of the parity bits is written next to the systematic bits in the first deinterleaver.	*See* claim 12.
16. The method of claim 14,	*See* claim 14.
wherein if a number of the systematic bits is greater than a number of the parity bits, part of the systematic bits is written prior to the parity bits in the second deinterleaver.	*See* claim 13.