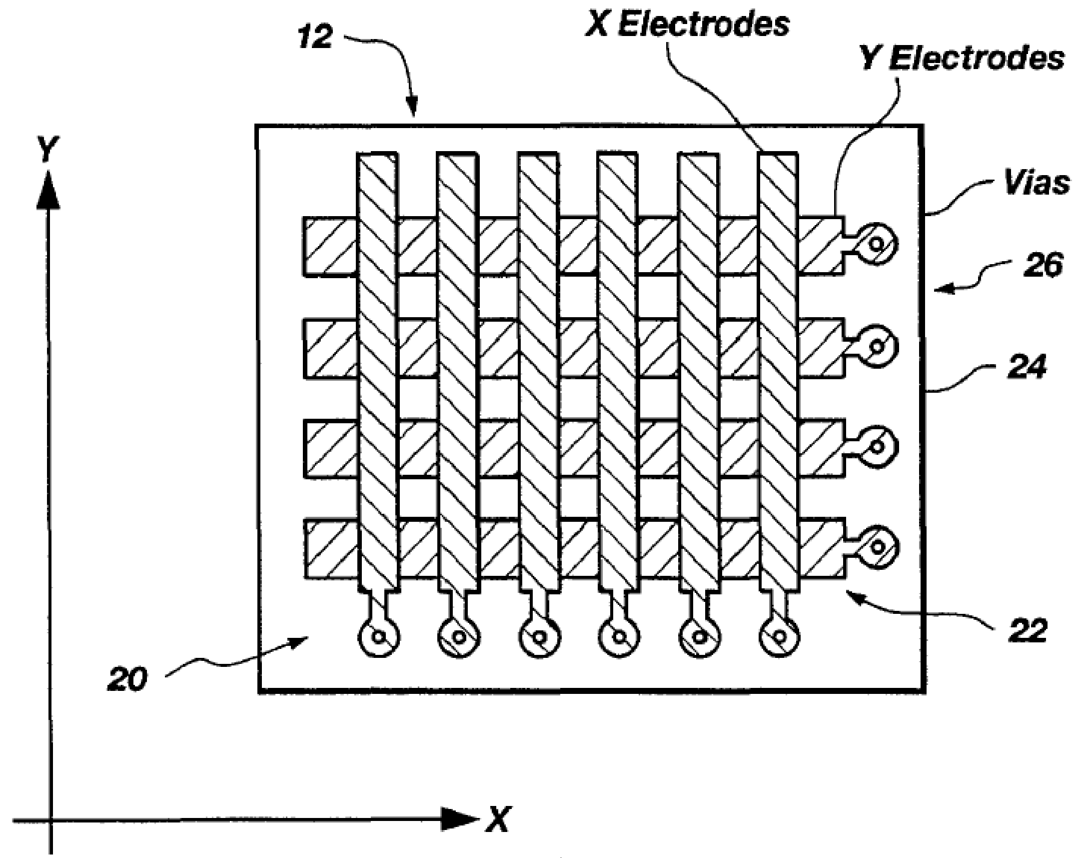
EXHIBIT 1

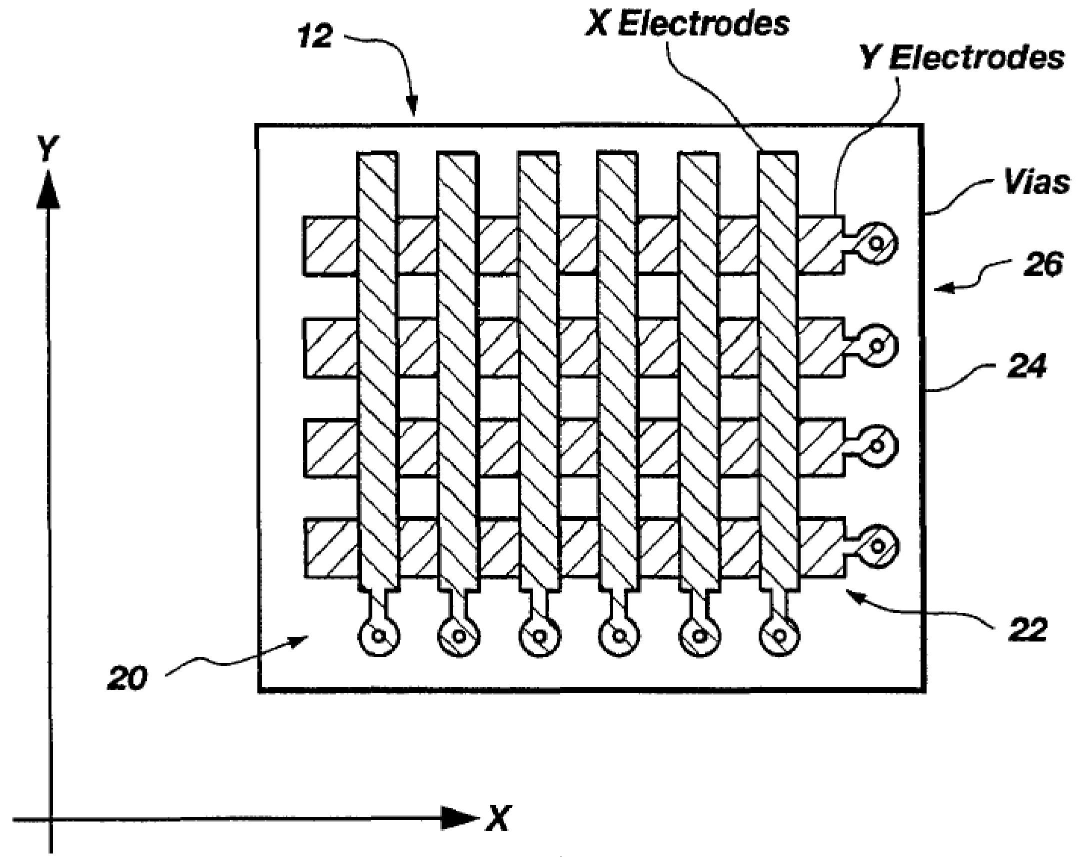
EXHIBIT V-4
SAMSUNG'S INVALIDITY CLAIM CHARTS FOR U.S. PATENT NO. 5,565,658 (GERPHEIDE '658)

U.S. Patent No. 7,920,129	Gerpheide '658
[1A] A capacitive touch sensor panel, comprising:	Gerpheide '658 discloses a capacitive touch sensor panel. See, e.g., id. at 1:10-14. For example, Gerpheide '658 states: "Apparatus and method for a capacitance-based proximity sensor with interference rejection. A pair of electrode arrays establish a capacitance on a touch detection pad, the capacitance varying with movement of a conductive object near the pad. The capacitance variations are measured synchronously with a reference frequency signal to thus provide a measure of the position of the object. Electrical interference is rejected by producing a reference frequency signal which is not coherent with the interference." See id. at Abstract.
[1B] a first set of traces of conductive material arranged along a first dimension of a two-dimensional coordinate system, the first set of traces having one or more widths including a maximum width;	Gerpheide '658 discloses a first set of traces of conductive material (e.g., X Electrodes in Fig. 2a) arranged along a first dimension of a two-dimensional coordinate system, the first set of traces having one or more widths including a maximum width. See id. at Fig. 2a, 4:41-54. For example, Gerpheide '658 states: "FIG. 2A illustrates the electrodes in a preferred electrode array 12, together with a coordinate axes defining X and Y directions. One embodiment includes sixteen X electrodes and twelve Y electrodes, but for clarity of illustration, only six X electrodes 20 and four Y electrodes 22 are shown. It is apparent to one skilled in the art how to extend the number of electrodes. The array is preferably fabricated as a multilayer printed circuit board 24. The electrodes are etched electrically conductive strips, connected to vias 26 which in turn connect them to other layers in the array. Illustratively, the array 12 is approximately 65 millimeters in the X direction and 49 millimeters in the Y direction. The X electrodes are approximately 0.7 millimeters wide on 3.3 millimeter centers. The Y electrodes are approximately three millimeters wide on 3.3 millimeter centers." Id. at 4:41-54. As shown below, Fig. 2a of Gerpheide '658 illustrates a first set of traces of conductive material (e.g., X Electrodes) arranged along a first dimension of a two-dimensional coordinate system. Fig. 2a of Gerpheide '658 also discloses the first set of traces (e.g., X

U.S. Patent No. 7,920,129	Gerpheide ’658
	Electrodes) having one or more widths including a maximum width. See, e.g., Fig. 2a, 4:41-54.  Fig. 2a

U.S. Patent No. 7,920,129	Gerpheide ’658
	To the extent Apple argues this limitation requires the first set of traces be “substantially the same width – a maximum width along their lengths,”[1] Gerpheide ’658 discloses the first set of traces that are substantially the same width – a maximum width along their lengths (e.g., X Electrodes in Fig. 2a). Id.
[1C] and a second set of traces of the conductive material spatially separated from the first set of traces by a dielectric and arranged along a second dimension of the two-dimensional coordinate system, the second set of traces having one or more widths including a minimum width;	Gerpheide ’658 discloses a second set of traces of the conductive material (e.g., Y Electrodes Fig. 2a) spatially separated from the first set of traces by a dielectric (e.g., Insulator 31 Fig. 2b) and arranged along a second dimension of the two-dimensional coordinate system, the second set of traces having one or more widths including a minimum width. See, e.g., id. at Fig. 2a-2b, 4:64-5:10. For example, Gerpheide ’658 states: “The X electrodes 20, Y electrodes 22, ground plane 25 and component traces 27 are etched copper traces within a multilayer printed circuit board. The ground plane 25 covers the entire array area and shields the electrodes from electrical interference which may be generated by the parts of the circuitry. The component traces 27 connect the vias 26 and hence the electrodes 20, 22, to other circuit components of FIG. 1. Insulator 31, insulator 32 and insulator 33 are fiberglass-epoxy layers within the printed circuit board 24. They have respective thicknesses of approximately 1.0 millimeter, 0.2 millimeters and 0.1 millimeters. Dimensions may be varied considerably as long as consistency is maintained. However, all X electrodes 20 must be the same size, as must all Y electrodes 22..” Id. at 4:64-5:10. As shown below, Fig. 2a of Gerpheide ’658 illustrates a second set of traces of conductive material (e.g., Y Electrodes) arranged along a second dimension of a two-dimensional coordinate system. Fig. 2a of Gerpheide ’658 further discloses the second set of traces (e.g., Y Electrodes) having one or more widths including a minimum width. See, e.g., id. at Fig. 2a, 4:41-54.

[1] *See* Apple’s Infringement Contentions at Exhibit 19, p. 1 (contending the Samsung Galaxy Tab 10.1 meets this limitation because “each of the first set of traces has substantially the same width – a maximum width along their entire lengths”).

U.S. Patent No. 7,920,129	Gerpheide '658
	 Fig. 2a As shown below, Fig. 2b of Gerpheide '658 illustrates the identified second set of traces spatially separated from the first set of traces by a dielectric insulator. See Fig. 2b, 5:4-9.

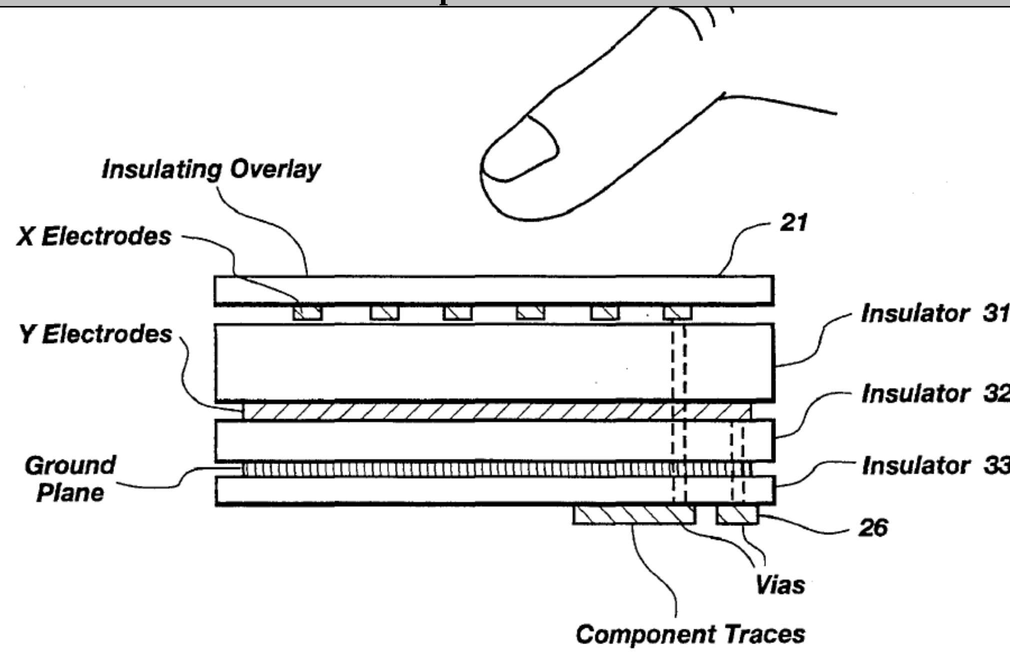
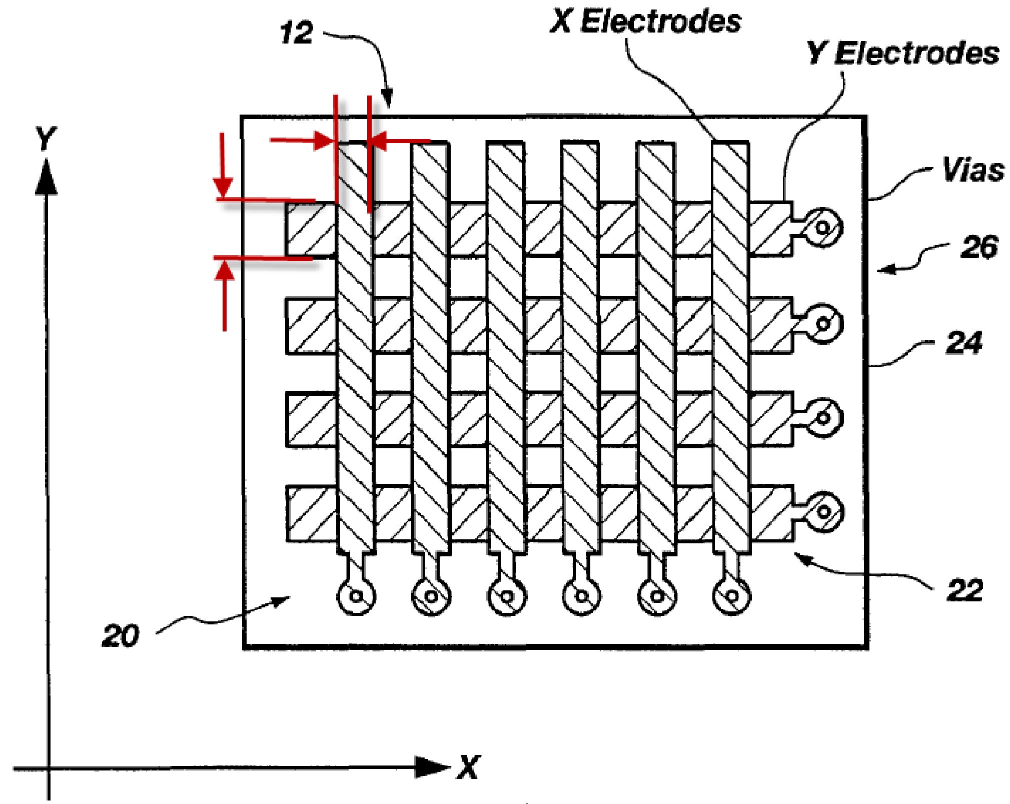
<table>
<tr><th>U.S. Patent No. 7,920,129</th><th>Gerpheide ’658</th></tr>
<tr><td></td><td>


Fig. 2b

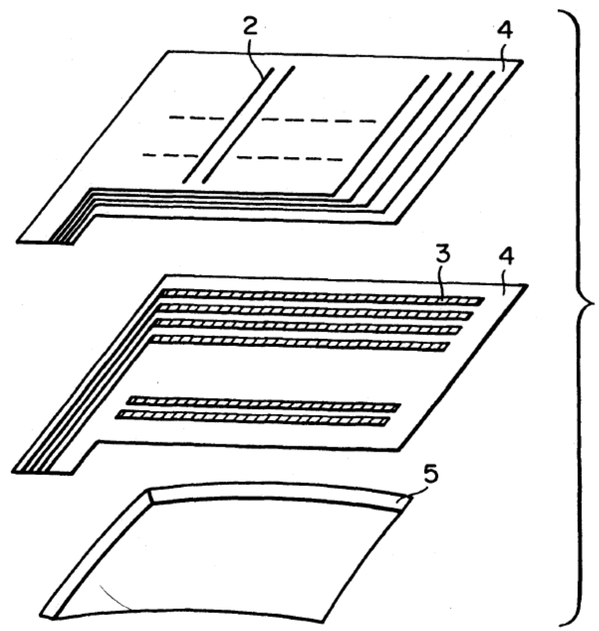
To the extent Apple argues this limitation requires the second set of traces be “substantially the same width – a maximum width along their lengths,”[2] Gerpheide ’658 discloses the second set of traces that are substantially the same width – a minimum width along their lengths (e.g., Y Electrodes in Fig. 2a). See, e.g., id. at Fig. 2a.</td></tr>
<tr><td>[1D] wherein the minimum width of the second set of traces is substantially greater than the maximum width of the first set of traces at least at an</td><td>Gerpheide ’658 discloses the minimum width of the second set of traces (e.g., Y Electrodes in Fig. 2a) is substantially greater than the maximum width of the first set of traces (e.g., X Electrodes in Fig. 2a) at least at an intersection of the first and second sets of traces to provide shielding for the first set of traces. See, e.g., id. at Fig. 2a, 4:41-54.</td></tr>
</table>

[2] *See* Apple’s Infringement Contentions at Exhibit 19, p. 2 (contending the Samsung Galaxy Tab 10.1 meets this limitation because “each of the second set of traces has substantially the same width – a minimum width along their entire lengths”).

U.S. Patent No. 7,920,129	Gerpheide ’658
intersection of the first and second sets of traces to provide shielding for the first set of traces;	For example, Gerpheide ’658 states: “FIG. 2A illustrates the electrodes in a preferred electrode array 12, together with a coordinate axes defining X and Y directions. One embodiment includes sixteen X electrodes and twelve Y electrodes, but for clarity of illustration, only six X electrodes 20 and four Y electrodes 22 are shown. It is apparent to one skilled in the art how to extend the number of electrodes. The array is preferably fabricated as a multilayer printed circuit board 24. The electrodes are etched electrically conductive strips, connected to vias 26 which in turn connect them to other layers in the array. Illustratively, the array 12 is approximately 65 millimeters in the X direction and 49 millimeters in the Y direction. The X electrodes are approximately 0.7 millimeters wide on 3.3 millimeter centers. The Y electrodes are approximately three millimeters wide on 3.3 millimeter centers.” Id. at 4:41-51. As shown below, Fig. 2a of Gerpheide ’658 further illustrates the width of the Y Electrodes is substantially greater than the width of the X Electrodes at least at an intersection of the first and second sets of electrodes.

U.S. Patent No. 7,920,129	Gerpheide ’658
	 Fig. 2a In addition to Fig. 2a, Gerpheide ’658 teaches that the minimum width of the Y Electrodes is greater than four times the maximum width of the X Electrodes. See, e.g., id. at 4:41-54 (teaching that the width of the Y Electrodes is 3 mm, while the width of the X Electrodes is only 0.7 mm). To the extent Gerpheide ’658 does not explicity disclose shielding for the first set of traces, one of ordinary skill in the art would understand that it is inherent in the electrode

U.S. Patent No. 7,920,129	Gerpheide ’658
	arrangement disclosed in Gerpheide ’658 that the wider second set of traces would provide shielding for the first set of traces. Moreover, to the extent not inherent or otherwise disclosed in Gerpheide ’658, making the minimum width of the second set of traces substantially greater than the maximum width of the first set of traces at an intersection of the first and second set of traces to provide shielding for the first set of traces would have been obvious to one of ordinary skill in the art. One of ordinary skill in the art would recognize that increasing the width of a conductor placed above a source of electromagnetic interference, in order to shield the interference from other system components, would be an obvious design choice that would yield predictable results obtained. Furthermore, using the wider second traces disclosed in Gerpheide ’658 to provide shielding was well-known in the art and would also have been obvious to one of ordinary skill in the art in light of U.S. Patent No. 5,083,118 to Kazama (“Kazama ’118”). Gerpheide ’658 recognized the benefit of protecting a capacitive touchscreen against electromagnetic interference arising from underlying circuitry. Gerpheide 658’s solution to this problem was to dispose a ground shield 25 between the circuitry and the second traces. See id. at 4:64-5:2 . For example, Gerpheide ’658 states: “The ground plane 25 covers the entire array area and shields the electrodes from electrical interference which may be generated by the parts of the circuitry.” Id. It was well-known in the art that by widening the second set of traces one could eliminate the need to “provide a further shield layer, which layer is grounded to relieve an influence from the noise of the tube surface.” See, e.g., Kazama ’118 at 1:42-46. Kazama ’118 discloses a capacitive touch sensor panel designed to be mounted on a CRT tube or LCD screen. See, e.g., id. at Abstract. The touch sensor panel comprises a first set of traces of conductive material arranged along a first dimension of a two-dimensional coordinate system, and a second set of traces of the conductive material spatially separated from the first set of traces by a dielectric, wherein the second set of traces has a minimum width that is substantially greater than the maximum width of the first set of traces at least at

U.S. Patent No. 7,920,129	Gerpheide ’658
	an intersection of the first and second sets of traces to provide shielding for the first set of traces. Kazama ’118 provides as follows: “Electrode wires 2 and 3 shown in exploded form in FIG. 2 are arranged perpendicularly on the tablet 1. The electrode wires Z [sic] and 3 are formed of ITO, which are subjected to vapor deposition etching as transparent electrodes on films 4, 4. With respect to the spacing arrangement of the electrode wires 2 and 3, the electrode wire 3 closer to CRT 5 is wider, as shown in FIG. 2, a gap therebetween being narrow.” Id. at 2:36-43. Fig. 2 of Kazama ’118 below illustrates the arrangement of traces disclosed by Kazama.  FIG. 2 Kazama ’118 recognized problems associated with electromagnetic interference arising from the underlying CRT tube or LCD screen and coupling onto the traces of the touch panel. See

U.S. Patent No. 7,920,129	Gerpheide ’658
	id. at Abstract. Kazama ’118, however, also recognized the problems associated with providing a separate shield layer to reduce electromagnetic interference. For example, Kazama ’118 states: “In use, it has been necessary to provide a further shield layer, which layer is grounded to relieve an influence from the noise of the tube surface. This results in problems of higher cost, and in deteriorating the transparency.” Id. at 1:42-46. Instead of a separate ground layer, Kazama teaches increasing the width of the second set of traces so that it is substantially greater than the width of the first set of traces at least at an intersection of the first and second sets of traces to provide shielding for the first set of traces For example, Kazama ’118 states: “one end of the electrode wire of the tablet was grounded with a low resistance, and a pattern of a layer close to the CRT tube surface was increased in width to narrow the gap of the pattern, whereby this layer functioned as a shield layer, enabling reduction of the noise of the tube surface.” Id. at 2:5-10. Kazama ’118 further states: “an increased with of the electrode wire on the side of the display surface of the input device such as a CRT, LCD, etc. to narrow a gap between the electrode wires, whereby the electrode wire not applied with a pulse functions as a shield layer.” Id. at 1:67-2:3; see also id. at Abstract (disclosing “a noise preventive means for relieving a noise from the display surface of the input device such as CRT, LCD, etc., said noise prevention means having . . . a pattern of each of the electrode wires of a layer close to the tube surface of CRT being increased and the gap between the electrode wires being narrowed”); see also id. 1:64-2:11, 1:49-56, 3:25-4:31, 2:27-44. Kazama ’118 further discloses that the “wider parallel electrode wires … act as a shield to reduce the effects of noise emanating from the display surface on the coordinate indications means,” where the coordinate indication means includes the first set of traces. See id. at 4:2-5. It would have been obvious to a person of ordinary skill in the art to combine the teachings of Gerpheide ’658 and Kazama ’118, resulting in a capacitive touch panel comprising a

U.S. Patent No. 7,920,129	Gerpheide ’658
	second set of traces with a minimum width that is substantially greater than the maximum width of a first set of traces at least at an intersection of the first and second sets of traces to provide shielding for the first set of traces. More specifically, it would have been obvious to a person of ordinary skill to remove the shield layer of Gerpheide ’658 and instead widen the second set of traces so that they function as a shield layer, as taught by Kazama ’118. The motivation for doing so is found in Kazama: to “enable[] reduction of the noise” from components or circuitry underlying the touch panel, while at the same time solving “problems in terms of cost and transparency.” Id. at 2:3-11. Moreover, it was well-known in the art of capacitive touch panels that a second set of traces could be used to provide shielding for the first set of electrode traces. For example, U.S. Patent No. 7,154,481 to Cross (“Cross ’481”), U.S. Patent Application Publication No. 2006/0227114 to Geaghan et al. (“Geaghan ’114”), and WIPO Publication No. WO 2005/073834 to Parkinson et al. (“Parkinson ’834”), which are all analogous art and directed to touch sensor panels with two-dimensional arrangements of traces of conductive material, disclose using a second set of traces to provide shielding for a first set of traces. For example, Cross ’481, which is also directed to a capacitive touch panel with a two-dimensional array of conductive traces, states: “The use of the bottom layer 514 as the reference layer advantageously provides shielding for the touch sensor from electromagnetic interference (EMI) originating in a display, such as an LCD or CRT display (not shown), located below the touch screen. This may eliminate the need for an additional conductive layer, usually found in present capacitive touch screens, to act as an EMI shield between the display and the touch sensor.” Id. at 9:61-10:1. Cross ’481 further discloses a transparent capacitive touch sensor panel designed to be mounted over a CRT or LCD, wherein a large conductive mutual capacitance reference trace is used to shield the upper one or more mutual capacitance measurement traces from electro-magnetic interference caused by the display. See, e.g., id. at Figure 5, 9:49-10:6. Cross ’481 further states: “The use of the bottom layer 514 as the reference layer advantageously provides shielding for the touch sensor from electromagnetic interference

U.S. Patent No. 7,920,129	Gerpheide ’658
	(EMI) originating in a display, such as an LCD or CRT display (not shown), located below the touch screen. This may eliminate the need for an additional conductive layer, usually found in present capacitive touch screens, to act as an EMI shield between the display and the touch sensor. An optional pattern of conductive segments (not shown) disposed on the surface of the conductive layer and coupled to the contacts 515 , 516 , 517 , 518 may be used to linearize the electric field across the surface of the top conductive layer.” Id. at 9:49-10:6. Geaghan ’114, which is directed to a capacitive touch panel with a two-dimensional array of conductive traces oriented 90 degrees from each other, states: “Rear electrodes can provide limited EMI shielding in lieu of a transparent rear shield layer. Driven rear electrodes can reduce currents due to parasitic capacitance.” Id. at [0076], see also id. at [0037](stating “[i]f driven with the same AC signal as the top resistive layer 344, 444 of the touch panel 330, 450, the rear electrodes 342, 451, 452, 453, 454, reduce capacitive coupling to the conductive elements behind the touch panel 330, 450, typically including the display and/or chassis”). Geaghan ’114 further claims: “11. The device of claim 7, wherein the one or more electrodes are driven with an AC signal. 12. The device of claim 7, wherein the one or more electrodes are configured to shield portions of the electrode layer from EMI.” Id. at Claims 11-12; see also id. [0026] – [0027] Parkinson ’834, which is also directed to a capacitive touch panel with a two-dimensional array of conductive traces, states: “the rear layer 52 is used as a shield to shield the front layer 50 from interferences from the LCD 15.” Id. at [0040]. It would have been obvious to one of ordinary skill in the art to combine the disclosure of Gerpheide ’658 with any one of Cross ’481, Geaghan ’114, or Parkinson ’834 to make the width of the second set of traces substantially greater than the maximum width of the first set of traces at least at an intersection of the first and second sets of traces to provide shielding for the first set of traces. Combining Gerpheide ’658 with any of Kazama ’118, Cross ’481, Geaghan ’114, or Parkinson ’834 would have been combining prior art elements according to known methods to yield predictable results. There would also be motivation to combine Gerpheide ’658 with any one of Cross ’481, Geaghan ’114, and Parkinson ’834: to reduce costs and improve transparency by removing the additional shield layer.

U.S. Patent No. 7,920,129	Gerpheide ’658
[1E] and wherein sensors are formed at locations at which the first set of traces intersects with the second set of traces while separated by the dielectric.	Gerpheide ’658 discloses sensors formed at locations at which the first set of traces intersects with the second set of traces while separated by the dielectric. See **[1C]**. For example, Gerpheide ’658 states: “FIG. 4 shows one specific embodiment of a synchronous electrode capacitance measurement unit 14 connected to the electrode array 12, in which algebraic sums of mutual capacitances between electrodes are measured. The components are grouped into four main functional blocks. A virtual electrode synthesis block 70 connects each of the X electrodes to one of the wires CP or CN, and each of the Y electrodes to one of the wires RP or RN. The electrodes are selectively connected to the wires by switches , preferably CMOS switches under control of the position locator apparatus 18 (FIG. 1) to select appropriate electrodes for capacitance measurement. All electrodes connected to the CP wire at any one time are considered to form a single "positive virtual X electrode". Similarly, the electrodes connected to CN, RP, and RN form a "negative virtual X electrode", a "positive virtual Y electrode", and a "negative virtual Y electrode", respectively.” Id. at 6:1-18; see also id. at 5:4:64- 5:25, 5:52-67, Fig. 2a-2b, Fig. 4. Gerpheide ’658 discloses the first set of traces and the second set of traces separated by the dielectric. See, e.g., id. at Fig. 2b, 4:64-5:10. To the extent Apple argues this claim requires a “touchscreen based on mutual capacitance,”[3] Gerpheide ’658 discloses a touchscreen based on mutual capacitance. Id.
[2A] The capacitive touch sensor panel of claim 1, further comprising a liquid crystal display (LCD) adjacent to the touch sensor panel, the LCD emitting a modulated Vcom signal,	Gerpheide ’658 discloses the capacitive touch sensor panel of claim 1, further comprising a liquid crystal display (LCD) adjacent to the touch sensor panel, the LCD emitting a modulated Vcom signal. For example, Gerpheide ’658 discloses the use of capacitive touchscreens with displays in discussing the prior art. See id. at 1:10-32. To the extent Gerpheide ’658 does not explicitly disclose a LCD adjacent to the touch sensor panel, the LCD emitting a modulated Vcom signal, one of ordinary skill in the art would

[3] *See* Apple’s Infringement Contentions at Exhibit 19, p. 5 (contending the Samsung Galaxy Tab 10.1 meets this limitation because “the Samsung Galaxy Tab 10.1 uses a touchscreen based on mutual capacitance”).

U.S. Patent No. 7,920,129	Gerpheide ’658
	understand that the capacitive touchscreen disclosed in Gerpheide ’658 inherently discloses a LCD adjacent to the touch sensor panel, the LCD emitting a modulated Vcom signal. To the extent that Philipp ’898 does not explicitly disclose emitting a modulated Vcom signal, one of ordinary skill in the art would understand that an LCD emitting a modulated Vcom signal is inherent in the LCD touch panel disclosed in Philipp ’898. See, e.g., id. at Id. at 8:19-28, 7:53-56, Figs. 3A-3B, Fig. 5. Moreover, it was well-known in the art that LCD displays emitted a modulated Vcom signal. See, e.g., Sarma, "Liquid Crystal Displays," Chapter 32 of _Electrical Measurement, Signal Processing, and Displays_, Volume 18 of _Principles and Applications of Engineering_, CRC Press LLC, 2004, p. 32-19, para. 1 (“Sarma”). For example, Sarma states: “Column driver voltage can be reduced by using a Vcom modulation drive method. In this method, the Vcom node (which is connected to all pixels in the display) is driven above and below a 5 V range of the column drivers. Each and every row time, the Vcom node is alternated between a voltage above and a voltage below the 5 V output range of the column drivers. This achieves 10 V across the LC material using 5 V column drivers. This method requires additional components and consumes additional power due to the oscillation of the Vcom node. In addition, to avoid capacitive injection problems, the row drivers usually have their negative supply modulated with the same frequency as the Vcom node. Note, however, that compared to 10 V column drivers, 5 V column drivers consume less power, and are simpler to design and fabricate using small-geometry CMOS. The Vcom modulation drive method can be used with a row (polarity) inversion scheme only (for elimination of pixel • icker) which results in some horizontal cross talk. However, column inversion and pixel inversion schemes provide better image quality with much-reduced cross talk, but they cannot be used with the Vcom modulation drive.” Id. See also U.S. Patent No. 6,128,045 to Anai at Figs. 7-8 and 5:7-21 (stating: “The common voltage generating circuit CVG generates a common voltage VCOM, whose level is inverted with respect to a reference voltage, in every horizontal scanning period and every vertical scanning period under the control of a polarity inversion signal POL supplied from the timing generating circuit 14. The common voltage VCOM is supplied to the counter

U.S. Patent No. 7,920,129	Gerpheide '658
	electrode. In synchronism with the level inversion of the common voltage VCOM, the polarity inverting circuit PV level-inverts the high vision video signal, NTSC video signal or multiplexed video signal supplied from the video signal processing circuit 19 with respect to the reference voltage in an opposite phase, and outputs the level-inverted signal. As a result, the polarity of voltage applied to the liquid crystal is periodically inverted.") See also U.S. Patent No. 7,825,885, U.S. Patent No. 6,873,312, and U.S. Patent No. 6,232,937.
[2B] and the second set of traces configured for shielding the first set of traces from the modulated Vcom signal.	See **[1D]** and **[2A]**. To the extent Gerpheide '658 does not explicitly disclose the second set of traces configured for shielding the first set of traces from a modulated Vcom signal, one of ordinary skill in the art would understand that it is inherent in the capacitive touchscreen display disclosed in Gerpheide '658, which discusses the use of an LCD device, that the inventors contemplated using the disclosed arrangement of conductive traces to shield against interference emitted from LCD screens, which would include modulated Vcom signals emitted from such screens. To the extent this claim element is not inherent in the disclosure of Gerpheide '658, as discussed above (see **[1D]**), it would have been obvious to one of ordinary skill in the art in light of the teachings of Kazama '118, that wider lower electrodes could provide shielding from noise emitted from an LCD screen, including that from a modulated Vcom signal. Moreover, it would have been obvious to one of ordinary skill in the art to combine Gerpheide '658 with Kazama '118 to provide shielding from LCD noise by widening the second set of traces. Doing so would have resulted in a combination of prior art elements according to known methods to yield predictable results.
[3] The capacitive touch sensor panel of claim 1, wherein the second set of traces are widened to substantially electrically isolate the first set of traces from a liquid crystal display (LCD).	See **[1D], [2A]**, and **[2B]**.
[5] The capacitive touch sensor panel	Gerpheide '658 discloses the capacitive touch sensor panel of claim 1 that further comprises

U.S. Patent No. 7,920,129	Gerpheide ’658
of claim 1, further comprising a computing system that incorporates the sensor panel.	a computing system that incorporates the sensor panel. See, e.g., id. at Fig. 1, 4:20-36.
[7] The capacitive touch sensor panel of claim 5, further comprising a digital audio player that incorporates the computing system.	See **[5]**. To the extent Gerpheide ’658 does not explicitly or inherently disclose a digital audio player that incorporates the sensor panel, it would have been obvious to one of ordinary skill in the art to incorporate the touch sensor panel disclosed in Gerpheide ’658 into a digital audio player. A person or ordinary skill in the art would have recognized that is was well known at the time of the invention to use touch sensor panels, such as the panel disclosed by Gerpheide ’658, to provide input to various types of digital systems, including digital audio systems. Using Gerpheide ’658’s touch sensor panel in a digital audio system would have resulted in a combination of prior art elements according to known methods to yield predictable results. Furthermore, a person of ordinary skill in the art would have been motivated to incorporate the touch sensor panel and computing system of Gerpheide ’658 into a digital audio player in light of the teachings of U.S. Patent Application Publication No. 2003/0210286 to Gerpheide et al. (“Gerpheide ’286”). Gerpheide ’286 discloses a capacitive touch sensor that maybe “The present invention can be used in portable electronic appliances…. Portable electronic appliances should be considered to include PDAs, mobile telephones, notebook computers, audio playback devices such as MP3 music players, and other similar devices that can display a list of items. ” Id. at [0043]. The motivation for incorporating the capacitive touch screen and computer system of Gerpheide ’658 in the digital audio player of Gerpheide ’286 would be to provide a robust display that would enable a digital audio player user to view information and receive feedback related to his input. See also U.S. Patent No. 7,932,898 to Philipp (“Philipp ’898”) at 14:45-54.
[9A] A digital audio player having a capacitive touch sensor panel, the touch sensor panel comprising:	See **[7]**.

U.S. Patent No. 7,920,129	Gerpheide ’658
[9B] a first set of traces of conductive material arranged along a first dimension of a two-dimensional coordinate system, the first set of traces having one or more widths including a maximum width;	See **[1B]**.
[9C] and a second set of traces of the conductive material spatially separated from the first set of traces by a dielectric and arranged along a second dimension of the two-dimensional coordinate system, the second set of traces having one or more widths including a minimum width;	See **[1C]**.
[9D] wherein the minimum width of the second set of traces is substantially greater than the maximum width of the first set of traces at least at an intersection of the first and second sets of traces to provide shielding for the first set of traces;	See **[1D]**.
[9E] and wherein sensors are formed at locations at which the first set of traces intersects with the second set of traces while separated by the dielectric.	See **[1E]**.
[10A] A capacitive touch sensor panel, comprising:	See **[1A]**.
[10B] sense traces having one or more widths including a maximum width;	See **[1B]**. Gerpheide ’658 discloses sense traces (e.g., X Electrodes in Fig. 2a) having one or more widths including a maximum width. See, e.g., id. at Fig. 4 and 6:48-63

U.S. Patent No. 7,920,129	Gerpheide ’658
[10C] and drive traces spatially separated from the sense traces by a dielectric, the drive traces having one or more widths including a minimum width,	See [**1C**]. Gerpheide ’658 discloses drive traces (e.g., Y Electrodes in Fig. 2a) spatially separated from the sense traces by a dielectric, the drive traces having one or more widths including a minimum width. See, e.g., id. at Fig. 4 and 6:48-63
[10D] the minimum width of the drive traces being substantially greater than the maximum width of the sense traces at least at an intersection of the sense and drive traces to provide shielding for the sense traces;	See **[1D]**, **[10B]**, and **[10C]**.
[10E] wherein sensors are formed at locations at which the sense traces intersect with the drive traces while separated by the dielectric.	See **[1E]**, **[10B]**, and **[10C]**.
[11A] The capacitive touch sensor panel of claim 10, further comprising a liquid crystal display (LCD) adjacent to the touch sensor panel, the LCD emitting a modulated Vcom signal,	See **[2A]**.
[11B] and the drive traces configured for shielding the sense traces from the modulated Vcom signal.	See **[2B]** and **[10C]**.
[12] The capacitive touch sensor panel of claim 10, wherein the drive traces are widened to substantially electrically isolate the sense traces from a liquid crystal display (LCD).	See **[3]** and **[10C]**.
[14] The capacitive touch sensor panel of claim 10, further comprising a computing system that incorporates the sensor panel.	See **[5]**.

U.S. Patent No. 7,920,129	Gerpheide '658
[16] The capacitive touch sensor panel of claim 14, further comprising a digital audio player that incorporates the computing system.	See **[7]**.
[17A] A method for shielding a capacitive touch sensor panel from capacitive coupling of modulated signals, comprising:	See **[1A]**, **[2A]**, and **[2B]**.
[17B] forming a first set of sense traces having one or more widths including a maximum width;	See **[1B]** and **[10B]**.
[17C] orienting the sense traces along a first dimension of a two-dimensional coordinate system;	See **[1B]** and **[10B]**.
[17D] forming a second set of drive traces spatially separated from the first set of sense traces by a dielectric, the second set of drive traces having one or more widths including a minimum width,	See **[1C]**, **[10B]**, and **[10C]**.
[17E] the minimum width of the drive traces being substantially greater than the maximum width of the sense traces at least at an intersection of the first and second sets of traces to provide shielding for the sense traces;	See **[1D]** and **[10D]**.
[17F] and orienting the drive traces along a second dimension of the two-dimensional coordinate system to form sensors at locations at which the sense traces intersect with the drive traces while separated by the dielectric.	See **[1C], [1E]**, and **[10E]**.

U.S. Patent No. 7,920,129	Gerpheide ’658
[18] The method of claim 17, further comprising affixing a liquid crystal display (LCD) adjacent to a side of the touch sensor panel closest to the drive traces, the LCD capable of emitting a modulated Vcom signal.	See **[2A]** and **[10C]**.
[19] The method of claim 17, further comprising widening the drive traces to substantially electrically isolate the sense traces from a liquid crystal display (LCD).	See **[3]**, **[10B]**, and **[10C]**.
[21A] A method for shielding a capacitive touch sensor panel from a source of capacitive coupling, comprising:	See **[1A]** and **[1D]**.
[21B] forming a first set of traces further from the source of capacitive coupling than a second set of traces, the first set of traces configured for sensing changes in mutual capacitance, the first set of traces having one or more widths including a maximum width;	See **[1B]**, **[1E]**, **[2A]**, and **[2B]**. Gerpheide ’658 discloses the first set of traces further from the source of capacitive coupling than a second set of traces, the first set of traces configured for sensing changes in capacitance, the first set of traces having one or more widths including a maximum width. For example, Gerpheide ’658 teaches a source of capacitive coupling is below the ground plane shown in Fig. 2b of Gerpheide ’658. See, e.g., id. at 4:66-5:2. Gerpheide ’658 discloses a first set of traces (e.g., X Electrodes in Figs. 2a and 2b) further from the source of capacitive coupling than a second set of traces (e.g., Y Electrodes in Figs. 2a and 2b). Gerpheide ’658 further discloses the first set of traces configured for sensing changes in mutual capacitance. See also Gerpheide ’658 at Fig. 4, 6:48-63. For example, Gerpheide ’658 states: “The capacitance measurement element 78 also contains a non-inverting drive buffer 76 which drives RN and negative virtual Y electrodes to change voltage levels copying the drive enable signal transitions. The inverting buffer 74 drives RP and the positive virtual Y electrodes to change voltage levels opposite the drive enable signal transitions. Since CP and CN are maintained at virtual ground, these voltage changes are the

U.S. Patent No. 7,920,129	Gerpheide ’658
	net voltage changes across the mutual capacitances which exist between virtual Y and virtual X electrodes. Charges proportional to these voltage changes multiplied by the appropriate capacitance values are thereby coupled onto nodes CP and CN (the "coupled charges"). The charge transfer circuit therefore supplies a proportional differential charges at outputs Qol and Qo2, which are proportional to the coupled charges and thus to the capacitances.” Id.
[21C] orienting the first set of traces along a first dimension of a two-dimensional coordinate system;	See **[1B]** and **[21B]**.
[21D] forming the second set of traces closer to the source of capacitive coupling than the first set of traces and spatially separated from the first set of traces by a dielectric,	See **[1C]** and **[21B]**.
[21E] the second set of traces having one or more widths including a minimum width, the minimum width of the second set of traces being substantially greater than the maximum width of the first set of traces at least at an intersection of the first and second sets of traces to provide shielding for the first set of traces,	See **[1D]**.
[21F] the second set of traces configured for being driven by low impedance driver outputs;	See **[1C]**, **[1D]**, and **[1D].** To the extent Gerpheide ’658 does not explicitly disclose this element, one of ordinary skill in the art would understand that it is inherent in the shielding electrode arrangement disclosed in Gerpheide ’658 that the second set of traces are configured for being driven by low impedance driver outputs. To the extent Gerpheide ’658 does not inherently or otherwise disclose this element, modifying Gerpheide ’658 to drive the shielding traces by a low impedance driver output would have been a simple design choice representing a trivial and predictable variation that would yield predictable results. Moreover, to the extent

U.S. Patent No. 7,920,129	Gerpheide ’658
	Gerpheide ’658 does not disclose this element, substituting a low impedance driver output for the disclosed arrangement would have been simple substitution of one known element for another to obtain predictable results, i.e., shielding.
[21G] and orienting the second set of traces along a second dimension of the two-dimensional coordinate system to form sensors at locations at which the first set of traces intersects with the second set of traces while separated by the dielectric.	See **[1C]** and **[1E]**.
[22] The method of claim 21, further comprising widening the drive traces to substantially electrically isolate the sense traces from a liquid crystal display (LCD).	See **[3]**.
[24A] A capacitive touch sensor panel, comprising:	See **[3]**.
[24B] sense traces formed on a first layer and arranged along a first dimension of a two-dimensional coordinate system;	See **[1B], [10B]** and **[21B]**.
[24C] and drive traces formed on a second layer spatially separated from the first layer by a dielectric, the drive traces arranged along a second dimension of the two-dimensional coordinate system;	See **[1C]** and **[10C]**.
[24D] wherein the drive traces are widened as compared to the sense traces to substantially cover the second layer except for a gap between adjacent drive traces so as to	See **[1D]**, **[3]**, **[10B]**, and **[10C]**.

U.S. Patent No. 7,920,129	Gerpheide '658
substantially electrically isolate the sense traces from a liquid crystal display (LCD);	
[24E] wherein sensors are formed at locations at which the sense traces intersect with the drive traces while separated by the dielectric;	See **[1E]** and **[10E]**.
[24F] and wherein each of the drive traces is of a substantially constant width.	See **[10C]**.
[25A] A method for shielding a capacitive touch sensor panel from coupling of modulated signals, comprising:	See **[1A]**, **[1D]**, **[2A]**, and **[2B]**.
[25B] forming a first set of sense traces on a first layer;	See **[1B]** and **[10B]**.
[25C] orienting the sense traces along a first dimension of a two-dimensional coordinate system;	See **[1B]** and **[10B]**.
[25D] forming a second set of widened drive traces on a second layer spatially separated from the first layer, the drive traces widened as compared to the sense traces to substantially cover the second layer except for a gap between adjacent drive traces so as to substantially electrically isolate the first set of sense traces from a liquid crystal display (LCD);	See **[1C]**, **[3]**, **[1D]**, **[10B]**, and **[10C]**.
[25E] and orienting the drive traces along a second dimension of the two-dimensional coordinate system to form	See **[1C]**, **[1E]**, **[10B]**, and **[10C]**.

U.S. Patent No. 7,920,129	Gerpheide ’658
sensors at locations at which the sense traces intersect with the drive traces;	
[25F] wherein each of the drive traces is of a substantially constant width.	See **[1C]** and **[10C]**.
[26A] A touch sensitive computing system, comprising:	See **[5]**.
[26B] a touch processor;	Gerpheide ’658 discloses a touch processor. See, e.g., id. at Fig. 1, 4.
[26C] a display;	Gerpheide ’658 discloses a display. See **[2A]**.
[26D] a touch sensor panel adjacent to the display and coupled to the touch processor,	See **[2A]-[2B]**.
[26E] the touch sensor panel including sense traces formed on a first layer, and drive traces formed on a second layer spatially separated from the first layer,	See **[1B]**, **[1C]**, **[10B]**, and **[10C]**.
[26F] the drive traces widened as compared to the sense traces to substantially cover the second layer except for a gap between adjacent drive traces so as to substantially electrically isolate the sense traces from a liquid crystal display (LCD),	See **[1D]**, **[3]**, **[10B]**, and **[10C]**.
[26G] wherein sensors are formed at locations at which the sense traces intersect with the drive traces;	See **[1E]**, **[10E]**, and **[21E]**.
[26H] and wherein each of the drive traces is of a substantially constant width.	See **[1C]** and **[10C]**.
[28] The touch sensitive computing system of claim 26, wherein the computing system is incorporated into	See **[5]** and **[7]**. To the extent Gerpheide ’658 does not inherently disclose this limitation, incorporating the

U.S. Patent No. 7,920,129	Gerpheide '658
a media player.	computing system of claim 26 into a digital media player would have been obvious to one of ordinary skill in the art. Incorporating the computing system of claim 26 into a digital media player would have been a simple design choice representing a trivial and predictable variation that would yield predictable results.