

EXHIBIT 18

PATENT
Response under 37 C.F.R. 1.116–
Expedited Procedure – Examining Group Art Unit 2136
Attorney Docket No.: 678-509 (P9463)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S):	Jae-Yoel KIM, et al.	**GROUP ART UNIT:** 2136
APPLICATION NO.:	09/611,518	**EXAMINER:** Colin, Carl G.
FILING DATE:	July 7, 2000	**DATED:** April 28, 2006

FOR: APPARATUS AND METHOD FOR GENERATING SCRAMBLING CODE IN UMTS MOBILE COMMUNICATION SYSTEM

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Commissioner for Patents
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AMENDMENT

Sir:

In response to the Office Action of the United States Patent and Trademark Office, which was mailed on January 28, 2006, please consider the following amendments and remarks.

05/03/2006 SHASSEN1 00000057 09611518
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CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

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Dated: April 28, 2006

Michael J. Musella

AMENDMENTS IN THE CLAIMS

1. (Previously Presented) A method for generating a primary scrambling code, the method comprising the steps of:

generating a first m-sequence from a first m-sequence generator including first shift registers having first shift register values a_i, wherein i = 0 to c-1 and where c is the total number of the registers;

generating a second m-sequence from a second m-sequence generator including second shift registers having values b_j, wherein j = 0 to c-1, and where c is the total number of the registers;

masking the first shift register values a_i with a first set of mask values K_i, wherein i = 0 to c-1 to generate a third m-sequence;

adding the first m-sequence with the second m-sequence to generate a primary scrambling code; and

adding the third m-sequence and the second m-sequence to generate a secondary scrambling code;

wherein, the masking step shifts the first m-sequence cyclically by L chips to generate an L^{th} secondary scrambling code associated with the primary scrambling code.

2-20. (Cancelled)

21. (Previously Presented) A scrambling code generator, comprising:

a first m-sequence generator to generate a first m-sequence by using a plurality of first registers with first shift register values a_i, wherein i = 0 to c-1 and where c is the total number of the first registers;

a second m-sequence generator to generate a second m-sequence by using a plurality of second registers with second shift register values b_j, wherein j = 0 to c-1 and where c is the total number of second registers;

a masking section to mask the first shift register values a_i with a first set of mask values K_i to generate a third m-sequence, wherein i = 0 to c-1 to generate a third m-sequence;

a first adder to add the first m-sequence and the second m-sequence to generate a primary scrambling code; and

a second adder to add the third m-sequence and the second m-sequence to generate a secondary scrambling code,

wherein the masking section shifts the first m-sequence cyclically by L chips to generate an L^{th} secondary scrambling code associated with the primary scrambling code.

22-30. (Cancelled)

31. (Previously Presented) The method of claim 1, wherein the primary scrambling code is one of a plurality primary scrambling codes and a K^{th} primary scrambling code is a $((K-1)*M+K)^{th}$ gold code, where M is a total number of secondary scrambling codes per primary scrambling code and 1<K<512.

32. (Previously Presented) The method of claim 1, wherein the secondary scrambling codes associated with a K^{th} primary scrambling code are from $((K-1)*M+K+1)^{th}$ to $(K*M+K)^{th}$ gold codes, where M is a total number of secondary scrambling codes per primary scrambling code and 1<K<512.

33. (Previously Presented) The method of claim 1, wherein 1<L<M, where M is a total number of secondary scrambling codes per primary scrambling code.

34. (Previously Presented) The method of claim 1, wherein the masking step is expressed by $\sum(k_i \times a_i)$.

35. (Previously Presented) The method of claim 1, further comprising:

masking the first shift register values a_i with a second set of mask values K_j to generate a fourth m-sequence, wherein j = 0 to c-1; and

adding the fourth m-sequence and the second m-sequence to generate an N^{th} secondary scrambling code associated with the primary scrambling code;

wherein, the masking step shifts the first m-sequence cyclically by N chips to generate an N^{th} secondary scrambling code.

36. (Previously Presented) The method of claim 35, wherein $1<N<M$, where M is a total number of secondary scrambling codes per primary scrambling code.

37. (Previously Presented) The method of claim 1, further comprising the step of delaying at least one of the primary scrambling code and secondary scrambling code to produce a Q-channel component, wherein the primary scrambling code and secondary scrambling code are I-channel components.

38. (Previously Presented) The scrambling code generator of claim 21, wherein the primary scrambling code is one of a plurality of primary scrambling codes and a K^{th} primary scrambling code is a $((K-1)*M+K)^{th}$ gold code, where M is a total number of secondary scrambling codes per primary scrambling code and $1<K<512$.

39. (Previously Presented) The scrambling code generator of claim 38, wherein the secondary scrambling codes associated with the K^{th} primary scrambling code are $((K-1)*M+K+1)^{th}$ to $(K*M+K)^{th}$ gold codes.

40. (Previously Presented) The scrambling code generator of claim 21, further comprising:

a second masking section to mask the first shift register values a_i, with a second set of mask values K_j, wherein j = 0 to c-1, to generate a fourth m-sequence; and

a third adder to add the fourth m-sequence and the second m-sequence to generate an N-th secondary scrambling code associated with the primary scrambling code,

wherein the second masking section shifts the first m-sequence cyclically by N chips to generate the N^{th} secondary scrambling code.

41. (Previously Presented) The scrambling code generator of claim 21, wherein the masking section shifts the first m-sequence cyclically by masking the first shift register values a_i in accordance with $\sum(K_i \times a_i)$.

42. (Previously Presented) The scrambling code generator of claim 21, wherein the first m-sequence generator cyclically shifts the first shift register values and the second m-sequence generator cyclically shifts the second shift register values.

43. (Previously Presented) The scrambling code generator of claim 21, wherein the first m-sequence generator adds predetermined shift register values of the first shift registers based on a first generating polynomial of the first m-sequence, right shifts the first shift register values a_i of the first shift registers, and replaces the first register value a_{c-1} with the result of the addition of the predetermined register values.

44. (Previously Presented) The scrambling code generator of claim 21, wherein the first m-sequence generator adds a first shift register value a_0 with a first shift register a_7 to form a next first shift register a_{c-1}.

45. (Previously Presented) The scrambling code generator of claim 21, wherein the second m-sequence generator adds predetermined shift register values of the second shift registers based on a second generating polynomial of the second m-sequence, right shifts the second shift register values b_j of the second shift registers, and replaces the second register value b_{c-1} with the result of the addition of the predetermined register values.

46. (Previously Presented) The scrambling code generator of claim 21, wherein the second m-sequence generator adds a second shift register value b_0 with a second shift register value b_5, b_7, and a second shift register value b_{10} to form a next second shift register value b_{c-1}.

47. (Previously Presented) The apparatus of claim 21, further comprising a means for delaying at least one of the primary scrambling code and the secondary scrambling code to

produce Q-channel component, wherein the primary scrambling code and the secondary scrambling code are I-channel components.

48 - 53. (Cancelled)

54. (New) A method for generating scrambling codes in mobile communication system having a scrambling code generator, the method comprising steps of:

generating a $((K-1)*M+K)^{th}$ gold code as a K^{th} primary scrambling code, where K is a natural number and M is a total number of secondary scrambling codes per one primary scrambling code; and

generating $((K-1)*M+K+1)^{th}$ through $(K*M+K)^{th}$ gold codes as secondary scrambling codes associated with the K^{th} primary scrambling code,

wherein the L^{th} Gold code is generated by adding an (L-1)-times shifted first m-sequence and a second m-sequence.

55. (New) The method as claimed in claim 54, wherein K is a primary scrambling code number and $1 \leq K \leq 512$.

56. (New) The method as claimed in claim 55, wherein the first m-sequence is generated from a first shift register memory having a plurality of first shift registers with first shift register values a_i, wherein i = 0 to c-1 and where c is the total number of the first registers and the (L-1)-times shifted first m-sequence is generated by masking the first shift register values a_i with mask values K_i, where i = 0 to c-1.

57. (New) The method as claimed in claim 56, wherein the masking is performed according to: $\sum(K_i \times a_i)$.

58. (New) The method as claimed in claim 54, wherein the generated primary scrambling code and secondary scrambling code are I-channel components and the method further comprises

delaying at least one of the primary scrambling code and secondary scrambling code to produce Q-channel components.

59. (New) An apparatus for generating scrambling codes in mobile communication system having a scrambling code generator, comprising:

a first m-sequence generator to generate a first m-sequence;

a second m-sequence generator to generate a second m-sequence; and

at least one adder for generating a ((K-1)*M+K)th Gold code as a Kth primary scrambling code by adding a ((K-1)*M+K-1)-times shifted first m-sequence and the second m-sequence,

wherein K is a natural number and M is a total number of secondary scrambling codes per one primary scrambling code.

60. (New) The apparatus of claim 59, wherein the secondary scrambling codes of the Kth primary scrambling codes are the ((K-1)*M+K+1)th through (K*M+K)th Gold codes.

61. (New) The apparatus as claimed in claim 60, wherein K is a primary scrambling code number and $1 \leq K \leq 512$.

62. (New) The apparatus as claimed in claim 59, wherein the first m-sequence generator comprises a plurality of first registers with first shift register values a_i, wherein i = 0 to c-1 and where c is the total number of the first shift registers, and the scrambling code generator further comprising at least one masking section for generating the n-times shifted first m-sequence by masking the first shift register values a_i with mask values K_i, where i = 0 to c-1.

63. (New) The apparatus as claimed in claim 62, wherein the masking is performed according to: $\sum(K_i \times a_i)$.

64. (New) The apparatus as claimed in claim 59, wherein the primary scrambling code and secondary scrambling code are I-channel components and the apparatus further comprises a

means for delaying at least one of the primary scrambling codes and secondary scrambling code to produce Q-channel components.

65. (New) A method for generating scrambling codes in mobile communication system having a scrambling code generator, comprising the steps of:

generating a first m-sequence;

generating a second m-sequence; and

generating a $((K-1)*M+K)^{th}$ Gold code as a K^{th} primary scrambling code by adding a ((K-1)*M+K-1)-times shifted first m-sequence and the second m-sequence,

wherein K is a natural number and M is a total number of secondary scrambling codes per one primary scrambling code.

66. (New) The method as claimed in claim 65, further comprising generating $((K-1)*M+K+1)^{th}$ to $(K*M+K)^{th}$ Gold codes as secondary scrambling codes corresponding to the K^{th} primary scrambling code.

67. (New) The method as claimed in claim 65, wherein K is a primary scrambling code number and $1 \leq K \leq 512$.

68. (New) The method as claimed in claim 65, wherein the first m-sequence is generated from a first shift register memory having a plurality of first shift registers with first shift register values a_i, wherein i = 0 to c-1 and where c is the total number of the first registers and the n-times shifted first m-sequence is generated by masking the first shift register values a_i with mask values K_i, where i = 0 to c-1.

69. (New) The method as claimed in claim 68, wherein the masking is performed according to: $\sum(K_i \times a_i)$.

70. (New) The method as claimed in claim 65, wherein each scrambling code is used as an I-channel component and a Q-channel component, corresponding to the I-channel component, is generated by delaying the I-channel component for a predetermined time.

REMARKS

Prior to entry of this amendment, Claims 1, 21 and 31-53 are pending in the application. Claims 48 and 51 have been rejected under 35 U.S.C. §112, first paragraph. Claims 1, 21, and 31-53 have been rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Dahlman et al. (U.S. 6,339,646) in view of Burns (U.S. 6,141,374). Claims 48-53 have been rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Dahlman et al. (U.S. 6,339,646 "Dahlman '646") in view of Dahlman et al. (WO 99/12284 "Dahlman WO").

Please cancel Claims 48-53, without prejudice.

Please add new Claims 54-70 as set forth herein. No new matter has been added.

Initially, Applicants respectfully submit the following reply to the Examiner's comments contained in the Response to Arguments section of the Office Action. Regarding item 1.2, the Examiner alleges that certain features that are relied on by the Applicants, i.e., managing a scrambling code (the relationship between scrambling codes) and a method for assigning a scrambling code, are not recited in rejected Claims 1 and 21. Each of Claims 1 and 21 recites "the masking step shifts the first m-sequence cyclically by L chips to generate an Lth secondary scrambling code associated with the primary scrambling code". It is respectfully submitted that this is in fact the relation between the primary scrambling code and the secondary scrambling code. In other words, Claims 1 and 21 recite that "the L^{th} secondary scrambling code associated with the primary scrambling code" is a result of adding "the second m-sequence" and "L-times shifted first m-sequence". Therefore it is respectfully submitted that the features relied on by the Applicants, i.e., managing a scrambling code (the relationship between scrambling codes) and a method for assigning a scrambling code, is in fact fully contained in Claims 1 and 21. It is respectfully requested that the claims be examined in light thereof.

Regarding the rejection of independent Claims 1 and 21 under §103(a), the Examiner states that Dahlman '646 in view of Burns renders the claims unpatentable. Dahlman '646 discloses slotted code usage in a cellular communications system; and, Burns discloses a method and apparatus for generating multiple matched-filter PN vectors in a CDMA demodulator. Each of Claims 1 and 21 recite "wherein, the masking step shifts the first m-sequence cyclically by L chips to generate an L^{th} secondary scrambling code associated with the primary scrambling code" and then using the masked sequence to generate a third m-sequence. The Examiner states that Dahlman '646 (at col. 3, line 60 – col. 4, line 6) and Burns (at col. 4, line 40 – col. 4, line 5) both disclose this element. The cited section of Dahlman '646 speaks about scrambling codes, but makes no reference to cyclically shifting an m-sequence to generate a secondary scrambling code and using a masked sequence to generate a third m-sequence. Further, the cited section of Burns states that extra values are inserted into each sequence, and combining sequences, but again, makes no reference to cyclically shifting an m-sequence to generate a secondary scrambling code and using a masked sequence to generate a third m-sequence.

Referring to col. 3 line 60 - col. 4 line 6 of Dahlman cited by the Examiner, the Dahlman codes are expanded by using the form "a channelization code + scrambling code + another code". It is well known that in a conventional CDMA communication system, a scrambling code is usually used to identify a base station and a mobile station, and a channelization code is usually used to distinguish channels transmitted from a mobile station or a base station. During implementation, each channel data is multiplied by different channelization codes; the sum of the multiplied result is multiplied by a scrambling code, and then transmitted. One skilled in the art would understand that col. 3 line 60 - col. 4 line 6 of Dahlman illustrates increasing a channelization code, wherein channelized and scrambled data is multiplied by another code. That is, it is clear that Dahlman represents "data x (channelization code x scrambling code x another code)".

On the contrary, the adder of the present invention, which is located within a scrambling code generator for generating scrambling codes, is for adding a first m-sequence to a second m-sequence or a shifted first m-sequence, and generating the scrambling code. Dahlman fails to disclose the adder of the present invention for generating the scrambling code and merely discloses processing data using the channelization code, the scrambling code and another code, not generating a scrambling code itself.

Additionally, referring again to col. 3, line 60 - col. 4, line 6 of Dahlman, one cell can use N scrambling codes, and if two scrambling codes, i.e., C_{i1}, C_{i2}, are used, each of the scrambling codes will be related to C_j. Channelization codes are then allocated to each of the scrambling codes. In other words, Dahlman simply suggests that the scrambling codes used in one cell are related to each other. Dahlman fails to disclose any specific relationship between the scrambling codes.

Claims 1 and 21 of the present application recite that the masking step shifts the first m-sequence cyclically by L chips to generate an L^{th} secondary scrambling code associated with the primary scrambling code as the relationship between the primary scrambling code and the secondary scrambling code. That is, the L^{th} secondary scrambling code is the result of adding "the second m-sequence" and "an L times shifted first m-sequence associated with the primary scrambling code". Dahlman merely mentions the background, conventional methods or problems of the prior art, but fails to teach the solutions and technical features of the present invention. One problem of the conventional method, described on page 4, lines 30-31 of the specification of the present invention, is that in the present UMTS standard specification, there is no description for scrambling code numbering and its generation, a problem solved by the claims of the present application.

Still further, Burns only teaches the concept of a "masking process" (see col. 3, line 40-col. 4, line 5), and the scrambling code managing method of Burns is completely different from that of the claims of the present application. More specifically, Burns in col. 3 describes the IS-95 or CDMA 2000 based scrambling code structure. As shown in col. 3, lines 4-20 of Burns, although all base stations use the same PN code (or a scrambling code), a unique shift offset for each basestation is applied to each PN code. The masking of Burns is performed to apply a unique offset to a local PN code for each base station after generating the local PN code used in all of the base stations. However, the masking process of the claims of the present application is not applied to a PN code (or a scrambling code), but to a m-sequence, which is not taught or disclosed by Burns.

Finally, although the Examiner asserts that Dahlman provides motivation for the present invention, Burns merely discloses that the use of an additional scrambling code is necessary to increase a channelization code. However, such disclosure is also taught in the background of the present invention and none of the references, either alone on in combination, discloses which codes are to be assigned as primary scrambling codes from among a plurality of Gold codes and which codes are to be assigned as secondary scrambling codes corresponding to each of the primary scrambling codes, as contained in the claims of the present application.

It is well known that Gold codes have no specific order. Likewise, in order to use Gold codes having no priority as primary and secondary scrambling codes, it is required to identify the currently used primary scrambling code and the corresponding secondary scrambling codes to a base station and a mobile station. The claims of the present application drastically simplify this process, since if a primary scrambling code and the corresponding secondary scrambling codes are generated from only two predetermined m-sequences, the corresponding secondary scrambling codes as well as the primary scrambling code to be used in the base station can be simply generated by notifying the base station and the mobile station of only the primary scrambling code.

Based on at least the foregoing, withdrawal of the rejections of Claim 1 and 21 is respectfully requested.

Turning now to the new claims presented herein, the following description is provided to assist in prosecution and in identifying support for the claimed subject matter in the specification.

Regarding new Claim 54, new Claim 54 recites, "a method for generating scrambling codes in mobile communication system having a scrambling code generator". As mentioned above, the application as originally filed not only discloses a generator for concurrently generating multiple Gold sequences using the mask functions but also describes on page 8, lines 3 to 6, that it is an object of the present invention to provide a method for efficiently dividing the set of Gold sequences into a primary scrambling code set and a secondary scrambling code set to reduce the number of mask functions stored in the memory. New Claim 54 refers to the second embodiment of the present invention as described in the specification at pages 12 to 16. This embodiment refers to a structure of primary and secondary scrambling codes as shown in Figure 9. Page 12, lines 19 to 23 states that while the first embodiment masks both m-sequences m1(t) and m2(t) to generate scrambling codes, the second embodiment involves cyclic shift of the m-sequence m2(t) only other than m1(1) to generate scrambling sequences, and as expressed by Equation 1 therein.

Furthermore, new Claim 54 recites, "generating a ((K-1)*M+K)-th gold code as a K-th primary scrambling code, where K is a natural number and M is a total number of secondary scrambling codes per one primary scrambling code". The description on page 12, lines 24 to 29 discloses:

> Referring to Fig. 9, when M secondary scrambling codes correspond to one primary scrambling code, the first, (M+2)'th, (2M+3)'th, ..., ((K-1)*M+K)'th, ..., and (511M+512)'th Gold codes are used as primary scrambling codes. The secondary scrambling codes corresponding to the (((K-1)*M+K)'th Gold code used as the (K)'th primary scrambling code are composed of M Gold codes, i.e., ((K-1)*M+(K+1)), ((K-1)*M+(K+2))..., and (K*M+K)'th gold codes. (Emphasis added.)

Additionally, new Claim 54 recites, "generating from ((K-1)*M+K+1)-th to (K*M+K)-th Gold codes as secondary scrambling codes associated with the K-th primary scrambling code". The description on page 12, lines 26 to 29 discloses that the secondary scrambling codes corresponding to the (((K-1)*M+K)'th Gold code used as the (K)'th primary scrambling code are composed of M Gold codes, i.e., ((K-1)*M+(K+1)), ((K-1)*M+(K+2))..., and (K*M+K)'th Gold codes.

Moreover, new Claim 54 recites, "wherein the L-th Gold code is generated by adding the (L-1)-times shifted first m sequence and the second m-sequence". The description on page 7, lines 23 to 25, which refers to the above-mentioned Equation 1, discloses that for the purpose of the present invention, the sum of the m-sequence m1(t) cyclically shifted time and the m-sequence m2(t) will be designated as a Gold code g. That is, g (t) = m1(t +)+m2(t).

Regarding new Claim 59, new Claim 59 recites, "an apparatus for generating scrambling codes in mobile communication system having a scrambling code generator", "a first m-sequence generator to generate a first m-sequence", and "a second m-sequence generator to generate a second m-sequence". In this context, the description on page 7 discloses in lines 14 and 15 that a Gold code used herein as a scrambling code is generated through binary adding of two distinct m-sequences.

Moreover, new Claim 59 recites, "at least one adder for generating a ((K-1)*M+K)-th gold code as a K-th primary scrambling code by adding a ((K-1)*M+K-1)-times shifted first m-sequence and the second m-sequence". The description on page 12, lines 24 to 26 discloses, referring to Fig. 9, that when M secondary scrambling codes correspond to one primary scrambling code, the first, (M+2)'th, (2M+3)'th, ... , ((K-1)*M+K)'th, ..., and (511M+512)'th Gold codes are used as primary scrambling codes. The description also discloses on page 7, lines 23 to 25, that for the purpose of the present invention, the sum of the m-sequence m1(t) cyclically shifted time and the m-sequence m2(t) will be designated as a Gold code g, that is, g (t) = m1(t +)+m2(t).

Finally, new Claim 59 recites, "wherein K is a natural number and M is a total number of secondary scrambling codes per one primary scrambling code". The description on page 12, lines 26 to 29 discloses that the secondary scrambling codes corresponding to the (((K-1)*M+K)'th Gold code used as the (K)'th primary scrambling code are composed of M Gold codes, i.e., ((K-1)*M+(K+1)), ((K-1)*M+(K+2))..., and (K*M+K)'th Gold codes.

Regarding new Claim 65, new Claim 65 recites, "a method for generating scrambling codes in mobile communication system having a scrambling code generator", "generating a first m-sequence" and "generating a second m-sequence", and "generating a ((K-1)*M+K)-th Gold code as a K-th primary scrambling code by adding the ((K-1)*M+K-1)-times shifted first m-sequence and the second m-sequence". The description on page 12, lines 24 to 26 discloses, referring to Fig. 9, that when M secondary scrambling codes correspond to one primary scrambling code, the first, (M+2)'th, (2M+3)'th, ..., ((K-1)*M+K)'th, ..., and (511M+512)'th Gold codes are used as primary scrambling codes. Further, the description on page 7, lines 23 to 25 discloses that for the purpose of the present invention, the sum of the m-sequence m1(t) cyclically shifted time and the m-sequence m2(t) will be designated as a Gold code g , that is, g (t) = m1(t +)+m2(t).

Moreover, new Claim 65 recites, "wherein K is a natural number and M is a total number of secondary scrambling codes per one primary scrambling code". The description on page 12, lines 26 to 29 discloses that the secondary scrambling codes corresponding to the ((K-1)*M+K)'th Gold code used as the (K)'th primary scrambling code are composed of M Gold codes, i.e., ((K-1)*M+(K+1)), ((K-1)*M+(K+2))..., and (K*M+K)'th Gold codes.

Independent Claims 1 and 21 are believed to be in condition for allowance. Without conceding the patentability per se of dependent Claims 31-47, these are likewise believed to be allowable by virtue of their dependence on their respective amended independent claims. Accordingly, reconsideration and withdrawal of the rejections of dependent Claims 31-47 is respectfully requested.

Accordingly, all of the claims pending in the Application, namely, Claims 1, 21, 31-47 and 54-70, are believed to be in condition for allowance. Should the Examiner believe that a telephone conference or personal interview would facilitate resolution of any remaining matters, the Examiner may contact Applicants' attorney at the number given below.

Respectfully submitted,

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