EXHIBIT 19

TFW 2136

PATENT
Attorney Docket No.: 678-509 (P9463)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S):	Jae-Yoel KIM, et al.	**GROUP ART UNIT:** 2136
APPLICATION NO.:	09/611,518	**EXAMINER:** Colin, Carl G.
FILING DATE:	July 7, 2000	**DATED:** December 11, 2006

FOR: APPARATUS AND METHOD FOR GENERATING SCRAMBLING CODE IN UMTS MOBILE COMMUNICATION SYSTEM

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE

Sir:

In response to the Office Action of the United States Patent and Trademark Office, which was mailed on August 9, 2006, please consider the following amendments and remarks.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postpaid in an envelope, addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Dated: December 11, 2006

Michael J. Musella

AMENDMENTS IN THE CLAIMS

1. (Previously Presented) A method for generating a primary scrambling code, the method comprising the steps of:

generating a first m-sequence from a first m-sequence generator including first shift registers having first shift register values a_i, wherein i = 0 to c-1 and where c is the total number of the registers;

generating a second m-sequence from a second m-sequence generator including second shift registers having values b_j, wherein j = 0 to c-1, and where c is the total number of the registers;

masking the first shift register values a_i with a first set of mask values K_i, wherein i = 0 to c-1 to generate a third m-sequence;

adding the first m-sequence with the second m-sequence to generate a primary scrambling code; and

adding the third m-sequence and the second m-sequence to generate a secondary scrambling code;

wherein, the masking step shifts the first m-sequence cyclically by L chips to generate an L^{th} secondary scrambling code associated with the primary scrambling code.

2-20. (Cancelled)

21. (Previously Presented) A scrambling code generator, comprising:

a first m-sequence generator to generate a first m-sequence by using a plurality of first registers with first shift register values a_i, wherein i = 0 to c-1 and where c is the total number of the first registers;

a second m-sequence generator to generate a second m-sequence by using a plurality of second registers with second shift register values b_j, wherein j = 0 to c-1 and where c is the total number of second registers;

a masking section to mask the first shift register values a_i with a first set of mask values K_i to generate a third m-sequence, wherein i = 0 to c-1 to generate a third m-sequence;

a first adder to add the first m-sequence and the second m-sequence to generate a primary scrambling code; and

a second adder to add the third m-sequence and the second m-sequence to generate a secondary scrambling code,

wherein the masking section shifts the first m-sequence cyclically by L chips to generate an L^{th} secondary scrambling code associated with the primary scrambling code.

22-30. (Cancelled)

31. (Previously Presented) The method of claim 1, wherein the primary scrambling code is one of a plurality primary scrambling codes and a K^{th} primary scrambling code is a $((K-1)*M+K)^{th}$ gold code, where M is a total number of secondary scrambling codes per primary scrambling code and $1<K<512$.

32. (Previously Presented) The method of claim 1, wherein the secondary scrambling codes associated with a K^{th} primary scrambling code are from $((K-1)*M+K+1)^{th}$ to $(K*M+K)^{th}$ gold codes, where M is a total number of secondary scrambling codes per primary scrambling code and $1<K<512$.

33. (Previously Presented) The method of claim 1, wherein $1<L<M$, where M is a total number of secondary scrambling codes per primary scrambling code.

34. (Previously Presented) The method of claim 1, wherein the masking step is expressed by $\sum(k_i \times a_i)$.

35. (Previously Presented) The method of claim 1, further comprising:

masking the first shift register values a_i with a second set of mask values K_j to generate a fourth m-sequence, wherein $j = 0$ to c-1; and

adding the fourth m-sequence and the second m-sequence to generate an N^{th} secondary scrambling code associated with the primary scrambling code;

wherein, the masking step shifts the first m-sequence cyclically by N chips to generate an N^{th} secondary scrambling code.

36. (Previously Presented) The method of claim 35, wherein 1<N<M, where M is a total number of secondary scrambling codes per primary scrambling code.

37. (Previously Presented) The method of claim 1, further comprising the step of delaying at least one of the primary scrambling code and secondary scrambling code to produce a Q-channel component, wherein the primary scrambling code and secondary scrambling code are I-channel components.

38. (Previously Presented) The scrambling code generator of claim 21, wherein the primary scrambling code is one of a plurality of primary scrambling codes and a K^{th} primary scrambling code is a $((K-1)*M+K)^{th}$ gold code, where M is a total number of secondary scrambling codes per primary scrambling code and 1<K<512.

39. (Previously Presented) The scrambling code generator of claim 38, wherein the secondary scrambling codes associated with the K^{th} primary scrambling code are $((K-1)*M+K+1)^{th}$ to $(K*M+K)^{th}$ gold codes.

40. (Previously Presented) The scrambling code generator of claim 21, further comprising:

a second masking section to mask the first shift register values a_i, with a second set of mask values K_j, wherein j = 0 to c-1, to generate a fourth m-sequence; and

a third adder to add the fourth m-sequence and the second m-sequence to generate an N-th secondary scrambling code associated with the primary scrambling code,

wherein the second masking section shifts the first m-sequence cyclically by N chips to generate the N^{th} secondary scrambling code.

41. (Previously Presented) The scrambling code generator of claim 21, wherein the masking section shifts the first m-sequence cyclically by masking the first shift register values a_i in accordance with $\sum(K_i \times a_i)$.

42. (Previously Presented) The scrambling code generator of claim 21, wherein the first m-sequence generator cyclically shifts the first shift register values and the second m-sequence generator cyclically shifts the second shift register values.

43. (Previously Presented) The scrambling code generator of claim 21, wherein the first m-sequence generator adds predetermined shift register values of the first shift registers based on a first generating polynomial of the first m-sequence, right shifts the first shift register values a_i of the first shift registers, and replaces the first register value a_{c-1} with the result of the addition of the predetermined register values.

44. (Previously Presented) The scrambling code generator of claim 21, wherein the first m-sequence generator adds a first shift register value a_0 with a first shift register a_7 to form a next first shift register a_{c-1}.

45. (Previously Presented) The scrambling code generator of claim 21, wherein the second m-sequence generator adds predetermined shift register values of the second shift registers based on a second generating polynomial of the second m-sequence, right shifts the second shift register values b_j of the second shift registers, and replaces the second register value b_{c-1} with the result of the addition of the predetermined register values.

46. (Previously Presented) The scrambling code generator of claim 21, wherein the second m-sequence generator adds a second shift register value b_0 with a second shift register value b_5, b_7, and a second shift register value b_{10} to form a next second shift register value b_{c-1}.

47. (Previously Presented) The apparatus of claim 21, further comprising a means for delaying at least one of the primary scrambling code and the secondary scrambling code to

produce Q-channel component, wherein the primary scrambling code and the secondary scrambling code are I-channel components.

48 - 53. (Cancelled)

54. (Currently Amended) A method for generating scrambling codes in mobile communication system having a scrambling code generator, the method comprising steps of:

generating a $((K-1)*M+K)^{th}$ gold code as a K^{th} primary scrambling code, where K is a natural number and M is a total number of secondary scrambling codes per one primary scrambling code; and

generating $((K-1)*M+K+1)^{th}$ through $(K*M+K)^{th}$ gold codes as secondary scrambling codes associated with the K^{th} primary scrambling code,

wherein an ~~the~~ L^{th} Gold code is generated by adding an (L-1)-times shifted first m-sequence and a second m-sequence.

55. (Previously Presented) The method as claimed in claim 54, wherein K is a primary scrambling code number and $1 \leq K \leq 512$.

56. (Previously Presented) The method as claimed in claim 55, wherein the first m-sequence is generated from a first shift register memory having a plurality of first shift registers with first shift register values a_i, wherein i = 0 to c-1 and where c is the total number of the first registers and the (L-1)-times shifted first m-sequence is generated by masking the first shift register values a_i with mask values K_i, where i = 0 to c-1.

57. (Previously Presented) The method as claimed in claim 56, wherein the masking is performed according to: $\sum(K_i \times a_i)$.

58. (Previously Presented) The method as claimed in claim 54, wherein the generated primary scrambling code and secondary scrambling code are I-channel components and the

method further comprises delaying at least one of the primary scrambling code and secondary scrambling code to produce Q-channel components.

59. (Previously Presented) An apparatus for generating scrambling codes in mobile communication system having a scrambling code generator, comprising:

a first m-sequence generator to generate a first m-sequence;

a second m-sequence generator to generate a second m-sequence; and

at least one adder for generating a $((K-1)*M+K)^{th}$ Gold code as a K^{th} primary scrambling code by adding a $((K-1)*M+K-1)$-times shifted first m-sequence and the second m-sequence,

wherein K is a natural number and M is a total number of secondary scrambling codes per one primary scrambling code.

60. (Previously Presented) The apparatus of claim 59, wherein the secondary scrambling codes of the K^{th} primary scrambling codes are the $((K-1)*M+K+1)^{th}$ through $(K*M+K)^{th}$ Gold codes.

61. (Previously Presented) The apparatus as claimed in claim 60, wherein K is a primary scrambling code number and $1 \leq K \leq 512$.

62. (Previously Presented) The apparatus as claimed in claim 59, wherein the first m-sequence generator comprises a plurality of first registers with first shift register values a_i, wherein i = 0 to c-1 and where c is the total number of the first shift registers, and the scrambling code generator further comprising at least one masking section for generating the n-times shifted first m-sequence by masking the first shift register values a_i with mask values K_i, where i = 0 to c-1.

63. (Previously Presented) The apparatus as claimed in claim 62, wherein the masking is performed according to: $\sum(K_i \times a_i)$.

64. (Previously Presented) The apparatus as claimed in claim 59, wherein the primary scrambling code and secondary scrambling code are I-channel components and the apparatus further comprises a means for delaying at least one of the primary scrambling codes and secondary scrambling code to produce Q-channel components.

65. (Previously Presented) A method for generating scrambling codes in mobile communication system having a scrambling code generator, comprising the steps of:

generating a first m-sequence;

generating a second m-sequence; and

generating a $((K-1)*M+K)^{th}$ Gold code as a K^{th} primary scrambling code by adding a $((K-1)*M+K-1)$-times shifted first m-sequence and the second m-sequence,

wherein K is a natural number and M is a total number of secondary scrambling codes per one primary scrambling code.

66. (Previously Presented) The method as claimed in claim 65, further comprising generating $((K-1)*M+K+1)^{th}$ to $(K*M+K)^{th}$ Gold codes as secondary scrambling codes corresponding to the K^{th} primary scrambling code.

67. (Previously Presented) The method as claimed in claim 65, wherein K is a primary scrambling code number and $1 \leq K \leq 512$.

68. (Previously Presented) The method as claimed in claim 65, wherein the first m-sequence is generated from a first shift register memory having a plurality of first shift registers with first shift register values a_i, wherein i = 0 to c-1 and where c is the total number of the first registers and the n-times shifted first m-sequence is generated by masking the first shift register values a_i with mask values K_i, where i = 0 to c-1.

69. (Previously Presented) The method as claimed in claim 68, wherein the masking is performed according to: $\sum(K_i \times a_i)$.

70. (Previously Presented) The method as claimed in claim 65, wherein each scrambling code is used as an I-channel component and a Q-channel component, corresponding to the I-channel component, is generated by delaying the I-channel component for a predetermined time.

REMARKS

Claims 1, 21, 31-47 and 54-70 are pending in the application. Claim 54 has been rejected under 35 U.S.C. §112, second paragraph, as being indefinite. Claims 58, 59, 64, 65 and 70 have been rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. Claims 1, 21, 31-47 and 54-70 have been provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 1-32 of copending application 11/003,558 (a continuation application claiming the benefit of the present application). Claims 1, 21, 31-47 and 54-70 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Dahlman et al. (U.S. 6,339,646) in view of Dahlman (WO 99/12284) and Burns (U.S. 6,141,374).

Please amend Claim 54 as set forth herein. No new matter has been added.

Regarding the rejection of Claim 54 under §112, second paragraph, the Examiner states "wherein the L^{th} Gold code is generated" is unclear. Claims 54 has been amended to read "wherein an L^{th} Gold code is generated". Claim 54 does not define an order of secondary scrambling codes, but defines that a secondary scrambling code relates to a certain primary scrambling code. The last clause in Claim 54 states how a Gold code, used as a secondary or primary scrambling code, is generated.

Based on at least the foregoing, withdrawal of the rejection of Claim 54 under §112 is respectfully requested.

Regarding the rejection of Claims 58, 64 and 70 under §112, first paragraph, as failing to comply with the written description requirement, the Examiner states:

> Claims 58 and 64 as amended recite wherein the primary scrambling code and the secondary scrambling code Claims 58 and 64 as amended recite wherein the primary scrambling code and the secondary code are I-channel components. Claim 70 recites similar limitation. However, the embodiment that applicant relies

on as illustrated in FIG. 10 describe the adders 1032-1034 generating I-channel scrambling code signal not the output from the adder 1030 used as a primary scrambling code (see page 20, line 26-page 21, line 5). Therefore, the claims as amended do not comply with the written description.

Claims 58, 64 and 70 particularly define I and Q components of primary and secondary scrambling codes. FIG. 7 discloses an adder 742 outputting an I component of the scrambling code, and a delay 722 outputting a Q component of the scrambling code, wherein the operation for separating and outputting the I/Q components is applicable to all embodiments of the present invention.

Based on at least the foregoing, withdrawal of the rejection of Claims 58, 64 and 70 under §112 is respectfully requested.

Regarding the rejection of Claims 59 and 65 under §112, first paragraph, as failing to comply with the written description requirement, the Examiner states:

> Claims 59 and 65 recite generating ((K-1)*M+K)th gold code as a primary scrambling code Claims 59 and 65 recite generating ((K-1)*M+1) times shifted first m-sequence and the second m-sequence. However, the specification explicitly states, the secondary scrambling codes are generated by adding cyclically shifted first m-sequence and the second m-sequence. The specification does not describe the claimed limitation as claimed in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed had possession of the claimed invention.

Claims 59-65 relate a transmitter being able to only generate a primary scrambling code without secondary scrambling codes. The detailed description teaches the steps of generating primary and secondary scrambling codes. There is no limitation that a secondary scrambling code has to be generated with a primary scrambling code. Moreover, in the title of invention and field of the invention, recites generating scrambling code".

Based on at least the foregoing, withdrawal of the rejection of Claims 59 and 65 under §112 is respectfully requested.

Regarding the provisional rejection of Claims 1, 21, 31-47 and 54-70 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 1-32 of copending application 11/003,558 (a continuation application claiming the benefit of the present application, i.e. the later-filed application), since there remain outstanding art rejections under §103, Applicants reserve the right to address this issue if and when all of the remaining art rejections are overcome.

Regarding the rejection of independent Claims 1, 21, 54, 59 and 65 under §103(a), the Examiner states that Dahlman et al. in view of Dahlman and Burns renders the claims unpatentable.

It is initially noted that the Examiner states in the Response to Arguments section on page 2-3 of the Office Action, that the arguments contained in the prior Response contained features not recited in the claims. The Examiner is incorrect. Specifically, the Examiner states "the Lth secondary scrambling code associated with the primary scrambling code is a result of adding the second m-sequence ad L times shifted the first m-sequence" is not recited in the claims. In the prior Response it was argued, "Claims 1 and 21 recite that "the L^{th} secondary scrambling code associated with the primary scrambling code" is a result of adding "the second m-sequence" and "L-times shifted first m-sequence"." Claim 1 recites, in part, masking the first shift register with a first set of mask values to generate a third m-sequence, then adding the third m-sequence and the second m-sequence to generate a secondary scrambling code, and wherein, the masking step shifts the first m-sequence cyclically by L chips to generate an L^{th} secondary scrambling code associated with the primary scrambling code. Therefore, adding "the second m-sequence" and "L-times shifted first m-sequence" does in fact result in an L^{th} secondary scrambling code, and is recited in the claims.

Second, the Examiner states that "the masking step shifts the first m-sequence to generate

an Lth secondary scrambling code and then using the masked sequence to generate a third m-sequence" is not recited in the claims. Again the Examiner is incorrect. Again Claim 1 recites, "the masking step shifts the first m-sequence cyclically by L chips to generate an L^{th} secondary scrambling code" and "masking the first shift register with a first set of mask values to generate a third m-sequence". Therefore, the masking step shifts the first m-sequence to generate an Lth secondary scrambling code and then using the masked sequence to generate a third m-sequence is in fact recited in the claims.

Also, it is respectfully submitted that the Examiner has only addressed two arguments out of several arguments presented in the prior Response. Therefore, it is respectfully requested that the Examiner fully consider all of the arguments presented in the prior Office Action.

Turning now to the specific art rejections, Dahlman et al. discloses slotted code usage in a cellular communications system; Dahlman discloses a method for assigning spreading codes; and, Burns discloses a method and apparatus for generating multiple matched-filter PN vectors in a CDMA demodulator.

Dahlman et al. speaks about scrambling codes, but makes no reference to cyclically shifting an m-sequence to generate a secondary scrambling code and using a masked sequence to generate a third m-sequence. Further, the cited section of Burns states that extra values are inserted into each sequence, and combining sequences, but again, makes no reference to cyclically shifting an m-sequence to generate a secondary scrambling code and using a masked sequence to generate a third m-sequence. One skilled in the art would understand that col. 3 line 60 - col. 4 line 6 of Dahlman illustrates increasing a channelization code, wherein channelized and scrambled data is multiplied by another code. On the contrary, the adder of the present invention, which is located within a scrambling code generator for generating scrambling codes, is for adding a first m-sequence to a second m-sequence or a shifted first m-sequence, and generating the scrambling code. Dahlman fails to disclose the adder of the present invention for generating the scrambling code and merely discloses processing data using the channelization code, the scrambling code and another code, not generating a scrambling code itself.

Additionally, Dahlman simply suggests that the scrambling codes used in one cell are related to each other. Dahlman fails to disclose any specific relationship between the scrambling codes.

Claims 1 and 21 of the present application recite that the masking step shifts the first m-sequence cyclically by L chips to generate an L^{th} secondary scrambling code associated with the primary scrambling code as the relationship between the primary scrambling code and the secondary scrambling code. In other words, the L^{th} secondary scrambling code is the result of adding "the second m-sequence" and "an L times shifted first m-sequence associated with the primary scrambling code".

Still further, Burns only teaches the concept of a "masking process" (see col. 3, line 40-col. 4, line 5), and the scrambling code managing method of Burns is completely different from that of the claims of the present application. The masking of Burns is performed to apply a unique offset to a local PN code for each base station after generating the local PN code used in all of the base stations. However, the masking process of the claims of the present application is not applied to a PN code (or a scrambling code), but to a m-sequence, which is not taught or disclosed by Burns.

None of the references, either alone on in combination, discloses which codes are to be assigned as primary scrambling codes from among a plurality of Gold codes and which codes are to be assigned as secondary scrambling codes corresponding to each of the primary scrambling codes, as contained in the claims of the present application.

Claim 54 relates to method for efficiently dividing the set of Gold sequences into a primary scrambling code set and a secondary scrambling code set to reduce the number of mask functions stored in the memory. Claim 54 recites, "generating a ((K-1)*M+K)-th gold code as a K-th primary scrambling code, where K is a natural number and M is a total number of secondary scrambling codes per one primary scrambling code". This feature is neither taught nor disclosed by the cited references.

Additionally, Claim 54 recites, "generating from ((K-1)*M+K+1)-th to (K*M+K)-th Gold codes as secondary scrambling codes associated with the K-th primary scrambling code". This feature is neither taught nor disclosed by the cited references.

Moreover, Claim 54 recites, "wherein the L-th Gold code is generated by adding the (L-1)-times shifted first m sequence and the second m-sequence". This feature is neither taught nor disclosed by the cited references.

Claim 59 recites, "an apparatus for generating scrambling codes in mobile communication system having a scrambling code generator", "a first m-sequence generator to generate a first m-sequence", and "a second m-sequence generator to generate a second m-sequence". This feature is neither taught nor disclosed by the cited references.

Moreover, Claim 59 recites, "at least one adder for generating a ((K-1)*M+K)-th gold code as a K-th primary scrambling code by adding a ((K-1)*M+K-1)-times shifted first m-sequence and the second m-sequence". This feature is neither taught nor disclosed by the cited references.

Finally, Claim 59 recites, "wherein K is a natural number and M is a total number of secondary scrambling codes per one primary scrambling code". This feature is neither taught nor disclosed by the cited references.

Claim 65 recites, "a method for generating scrambling codes in mobile communication system having a scrambling code generator", "generating a first m-sequence" and "generating a second m-sequence", and "generating a ((K-1)*M+K)-th Gold code as a K-th primary scrambling code by adding the ((K-1)*M+K-1)-times shifted first m-sequence and the second m-sequence". This feature is neither taught nor disclosed by the cited references.

Moreover, Claim 65 recites, "wherein K is a natural number and M is a total number of secondary scrambling codes per one primary scrambling code". This feature is neither taught nor disclosed by the cited references.

In summary, the present invention is related to a generating primary or a secondary scrambling code by adding the first shifted m sequence to the second 2 m sequence, wherein a type and an order of the generated scrambling code are determined by the number of shifting times of the first m sequence. Conventionally, it is well-known that Gold codes do not have fixed order. To use these Gold codes as primary/secondary scrambling codes, it is necessary to clearly indicate to each base station a primary scrambling code and corresponding secondary scrambling codes.

The present invention discloses:

1) generating a primary scrambling code and secondary scrambling codes with predetermined 2 m sequences;

2) using the sum of the first m sequence shifted (L-1) times and the first m sequence as L^{th} gold code; and

3) using ((K-1)*M+K)-th gold code as a K-th primary scrambling code (See claims 54, 59, and 65), and using ((K-1)*M+K+1)~(K*M+K)-th gold codes as secondary scrambling code corresponding to the K-th primary scrambling code (e.g., claim 54).

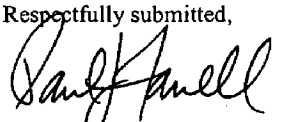
A base station and a mobile station can simply generate and indicate not only primary scrambling code to be used, but also corresponding secondary scrambling codes.

Based on at least the foregoing, withdrawal of the rejection of independent Claims 1, 21, 54, 59 and 65 under §103(a) is respectfully requested.

Independent Claims 1, 21, 54, 59 and 65 are believed to be in condition for allowance. Without conceding the patentability per se of dependent Claims 55-58, 60-64 and 66-70, these are likewise believed to be allowable by virtue of their dependence on their respective amended independent claims. Accordingly, reconsideration and withdrawal of the rejections of dependent Claims 55-58, 60-64 and 66-70 is respectfully requested.

Accordingly, all of the claims pending in the Application, namely, Claims 1, 21, 31-47 and 54-70, are believed to be in condition for allowance. Should the Examiner believe that a telephone conference or personal interview would facilitate resolution of any remaining matters, the Examiner may contact Applicants' attorney at the number given below.

Respectfully submitted,



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