EXHIBIT 11

MOS Sampled Data Recursive Filters Using Switched Capacitor Integrators

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Abstract—**A new technique to analog sampled data filtering is presented which can be fully integrated using MOS technology. Advantages of this new approach are reduced circuit complexity, low sensitivity to coefficient variations, and efficient utilization of silicon area. Performance of monolithic low Q (Q = 1) and high Q (Q = 73) filters are presented which were implemented using NMOS technology. In implementing the high Q filter a new operational amplifier design was used which had a 14-V output range, rms noise voltage of 45 μV, an open-loop gain of 6000, and a unity-gain bandwidth of 2 MHz.**

I. Introduction

ONE OF THE most common circuits in electronic systems are filters for frequency selective filtering. As large scale integration techniques are being used to integrate systems, it is becoming increasingly important to develop techniques to efficiently implement these filters. Since these applications often require a large number of filters on a single integrated circuit (IC) as well as circuitry to implement other system functions; it is desirable that the filters be fully integrated, require no trimming, and use as little silicon circuit area as possible.

Conventional active filters which use a thin film or other hybrid technology, while being a significant advance over discrete component passive filters, do not meet any of the above requirements and are therefore not appropriate for the system LSI applications.

A more promising approach is the use of charge-transfer devices (CTD) to implement analog sampled data transversal filters [1]. However, since CTD transversal filters have only zeros of transmission (no poles) in their transfer function, they are relatively inefficient in their use of silicon area in implementing simple frequency response functions: e.g., a narrow bandpass response with a Q of 90, which can be implemented with a two-pole recursive filter, requires five hundred CTD stages [2]. In addition, the large insertion loss experienced in CTD transversal filters, which is usually greater than 20 dB with nondestructive capacitive sensing, requires that a low noise output amplifier be used in order to obtain filter dynamic ranges in excess of 70 dB [3]. It is difficult to achieve the required level of noise performance with integrated MOS operational amplifiers.

Monolithic recursive filters have been implemented using analog sampled data techniques which do not have the above disadvantages. The output signal voltage in a recursive filter can be sensed directly (instead of capacitively) resulting in a larger signal and thus significantly relaxing the requirements on the noise performance of the amplifiers. Previous implementations of MOS analog sampled data recursive filters have used the conventional direct form of a second-order section and even though this organization is widely used in digital filtering, the sensitivity of the filter frequency response to the values of the filter coefficients can be very high [4]. In general this is not an important disadvantage for a digital filter since it is only necessary to increase the number of bits used in quantization of the filter coefficients until adequate performance is achieved. However, it is important in an analog implementation, because there are physical limits to the achievable coefficient accuracy.

In this paper new configurations of analog sampled data recursive filters will be presented which yield frequency responses that have a low sensitivity to the values of the filter coefficients [5], [6]. In addition these new filters will be shown to need only a small amount of silicon area and require relatively low performance amplifiers.

These filters, which are based on conventional state variable filter design techniques, make use of switches, capacitors, and operational amplifiers in a manner related to the "switched" filters that were investigated using discrete components in the late 1960's [7]. In this paper we will refer to these filters as switched capacitor filters. It will be found that the MOS technology is particularly well suited for implementing these filters for the following reasons: the high density of MOS components (e.g., MOS operational amplifiers are 3–5 times smaller than their bipolar counterparts); the high precision and stability with which filter coefficients can be derived using ratios of capacitor values; and the essentially ideal characteristics of MOSFET switches.

II. Switched Capacitor "Resistors"

A major reason that active filters have not previously been fully integrated in MOS technology is the necessity of accurately defining resistance-capacitance products, which requires that the *absolute* value of the resistors and capacitors be well controlled. In addition, integrated (diffused) resistors have poor temperature and linearity characteristics as well as requiring a large amount of silicon area.

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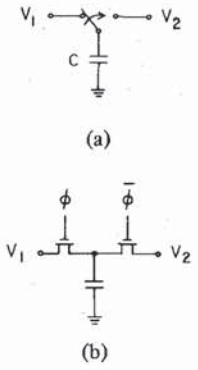


Fig. 1. (a) A "resistor" implemented using a switched capacitor. (b) MOS implementation.

A circuit that performs the function of a resistor which does not have these disadvantages has been investigated independently by several workers [5], [8], [9] and is shown in Fig. 1(a). The operation of this "resistor" is as follows: the switch is initially in the left-hand position so that the capacitor C is charged to the voltage V_1. The switch is then thrown to the right and the capacitor is discharged to the voltage V_2. The amount of charge which flows into (or from) V_2 is thus $Q = C(V_2 - V_1)$. If the switch is thrown back and forth every T_c seconds, then the current flow i into V_2 will be

$$i = \frac{C(V_2 - V_1)}{T_c}. \tag{1}$$

Thus the size of an equivalent resistor which would perform the same function as this circuit is $R = T_c/C$. If the switching rate $f_c = 1/T_c$ is much larger than the signal frequencies of interest then the time sampling of the signal which occurs in this circuit can be ignored and the switched capacitors can then be considered as a direct replacement for a conventional resistor. If, however, the switch rate and signal frequencies are of the same order then sampled data techniques are required for analysis and, as for any sampled data system, the input signal should be bandlimited below $f_c/2$ as dictated by the sampling theorem.

The MOS realization of the circuit of Fig. 1(a) is shown in Fig. 1(b). The two MOSFET's are operated as switches which are pulsed with a two phase nonoverlapping clock (ϕ and $\bar{\phi}$) at a frequency f_c. The stability and linearity of the resistance value $R = 1/f_cC$ is much better than that obtained from diffused resistors, since the insulator in a properly fabricated MOS capacitor has essentially ideal characteristics. For example, typical temperature coefficients for these capacitors are less than 10 ppm [10]. Another important advantage of the switched capacitor resistors is the high accuracy of RC time constants that can be obtained with their use. If a capacitor C_1 which is switched at a clock rate of f_c is connected to a capacitor C_2 the resultant time constant of this RC network τ_{RC} is

$$\tau_{RC} = \left(\frac{1}{f_cC_1}\right)C_2 = \frac{1}{f_c}\left(\frac{C_2}{C_1}\right). \tag{2}$$

For a given clock rate the value of τ_{RC} is therefore determined by a ratio of capacitor values which makes it insensitive to most processing variations.

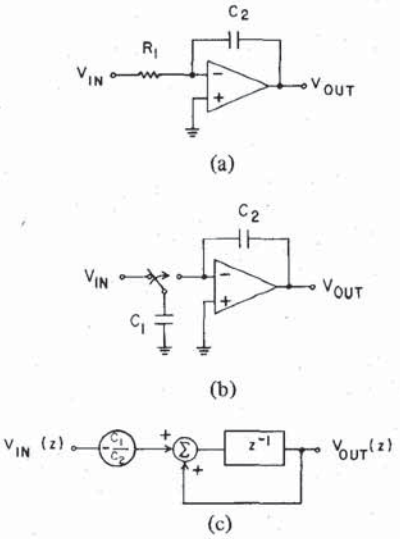


Fig. 2. (a) Conventional integrator. (b) Sampled data integrator. (c) z-transform block diagram of integrator in (b).

The relative values of the capacitors C_1 and C_2 are determined by photolithographic definition of their area. Since the capacitance per unit area is uniform across an IC it is possible to achieve high precision in the capacitor ratio. It has been shown that the error in such ratios can be less than 0.1 percent using standard MOS processing techniques [10]. In addition the stability of this ratio is extremely high since to first order there is no temperature dependence in the capacitance ratio. It is thus apparent that the switched capacitor resistor of Fig. 1 makes it possible to design precise stable RC active filters which can be fully integrated using MOS technology.

III. Analog Sampled Data State Variable Filters

The problem of implementing active filters in MOS technology has thus been reduced to a question of what kind of an active filter should be used. The state variable synthesis method [11] has the dual advantages of a very low sensitivity to coefficient values as well as only requiring relatively low performance operational amplifiers.

A. Sampled Data Integrators

State variable filters are derived from analog simulation techniques used in analog computers. The basic building block of these computers is an operational amplifier connected as an integrator, as shown in Fig. 2(a). The transfer function of this integrator is

$$H(\omega) = -\frac{1}{j\omega R_1 C_2}. \tag{3}$$

In Fig. 2(b) the resistor R_1 in the integrator has been replaced by the switched capacitor circuit of Fig. 1(a) with $C_1 = 1/f_cR_1$. In the nth clock period, the capacitor C_1 is charged to the voltage $V_{in}(nT_c)$ and then after the switch is thrown to the right, is discharged by the operational amplifier. The charge $C_1V_{in}(nT_c)$ is thus effectively transferred from C_1 to the

feedback capacitor C_2. Taking into account the delay of one clock period introduced by the switching process results in the following charge conservation equation:

$$C_2 V_{out}[nT_c] = C_2 V_{out}[(n-1)T_c] - C_1 V_{in}[(n-1)T_c]. \tag{4}$$

Since this is a sampled data system, the z-transform technique should be used, which yields the transfer function

$$H(z) = \frac{-(C_1/C_2)\, z^{-1}}{1 - z^{-1}}. \tag{5}$$

A block diagram of the z-transform interpretation of this integrator is shown in Fig. 2(c). If a high clock rate $f_c >> \frac{\omega}{2\pi}$ is assumed then z can be approximated by $1 + j\omega T_c$ which when substituted into (5) yields (3) as expected, i.e., if the capacitor C_1 is switched fast enough then it is equivalent to a resistor.

B. Second-Order Filters

There are many possible circuit organizations using state variable design techniques which can be used to implement two poles. In this section three different versions will be presented and the advantages and disadvantages of each with respect to sensitivity, the size of the capacitor ratios and circuit complexity will be discussed.

Version 1: The conventional circuit for realizing a pair of complex poles using state variable filters is shown in Fig. 3(a). A straightforward replacement of the resistors in this circuit with switched capacitors yields the circuit shown in Fig. 3(b). Since each integrator is inverting, the negative feedback around both integrators requires an additional inversion. In Fig. 3(b) this is achieved by feeding the output back into the bottom plate of the $\alpha_1 C_1$ capacitor. The charge introduced into the first integrator is thus $(V_{in} - V_{out})\, \alpha_1 C_1$ and the necessary sign inversion has been accomplished. The second integrator has a local feedback obtained through the switched capacitor $\alpha_2 C_2$. As in conventional state variable filters both bandpass (i.e., the transfer function has a zero near zero frequency) and low-pass filter characteristics are available at the outputs V_{out1} and V_{out2}, respectively. The z-transform block diagram of this filter is shown in Fig. 3(c). It is interesting to note that this block diagram is the same as a digital filter structure which was developed for low coefficient sensitivity [12]. The transfer function for the bandpass filter output at V_{out1} is

$$\frac{V_{out1}(z)}{V_{in}(z)} = \frac{\alpha_1[(1-\alpha_2) - z]}{z^2 - (2-\alpha_2)z + (1 + \alpha_1\alpha_2 - \alpha_2)} \tag{6}$$

where α_1 and α_2 are the capacitor ratios defined in Fig. 3(b). The low-pass filter output at V_{out2} has the transfer function

$$\frac{V_{out2}(z)}{V_{in}(z)} = \frac{\alpha_1\alpha_2}{z^2 - (2-\alpha_2)z + (1 + \alpha_1\alpha_2 - \alpha_2)}. \tag{7}$$

The position of the poles in the z-plane can be determined by comparing to the canonical equation for a second-order filter

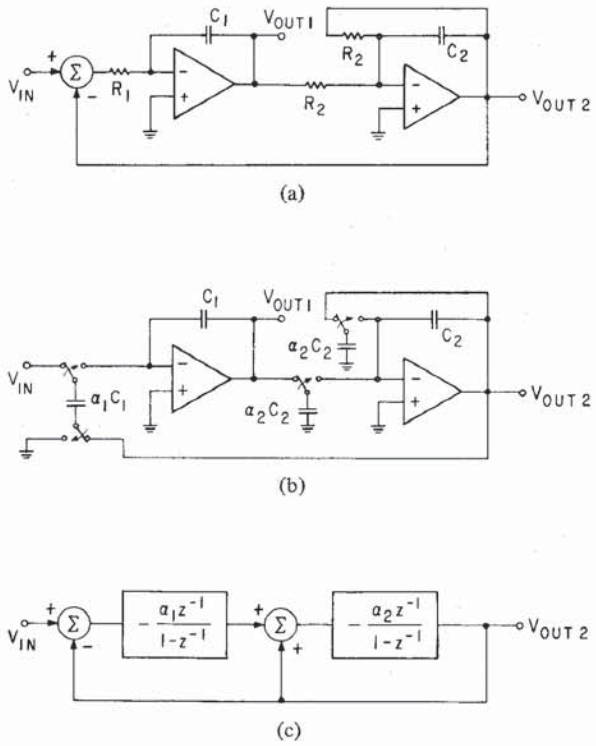


Fig. 3. (a) Conventional state variable filter. (b) Sampled data version of (a). (c) z-transform block diagram of (b).

$$H(z) = \frac{1}{z^2 - 2zR\cos\theta + R^2} \tag{8}$$

where R and θ are the polar coordinates in the z-plane of the two poles. Then the following formulas are valid

$$f_0 = \frac{f_c}{2\pi}\sqrt{\theta^2 + \ln^2(R)} \tag{9a}$$

$$Q = -\frac{\pi f_0}{f_c \ln(R)} \tag{9b}$$

where f_0 and Q are the center frequency and selectivity, respectively. From (6)-(9) the following design formulas can be derived

$$\alpha_2 = 2\left[1 - e^{-(\pi f_0/Qf_c)}\cos\left(\frac{\pi f_0}{f_c}\sqrt{4 - \frac{1}{Q^2}}\right)\right] \tag{10a}$$

$$\alpha_1 = 1 + \frac{1}{\alpha_2}(e^{-(2\pi f_0/Qf_c)} - 1). \tag{10b}$$

Since it is assumed that no trimming of component values will be performed it is necessary to investigate the sensitivity of f_0 and Q to variations in α_1 and α_2 to determine the required accuracy of these ratios. For $f_0 << f_c$ and $Q >> 1$, the sensitivity of the center frequency f_0 to α_2 is

$$S_{\alpha_2}^{f_0} = \left|\frac{\partial f_0}{\partial \alpha_2}\right| \frac{\alpha_2}{f_0} \cong \left(\frac{f_c}{2\pi f_0}\right)\sin\left(\frac{\pi f_0}{f_c}\right). \tag{11}$$

The sensitivity thus can be reduced to 0.5 (i.e., a ± 1 percent tolerance in α_2 yields a ± 0.5 percent variation in f_0) by increasing the clock rate so that $f_0 << f_c$. Similar sensitivity re-

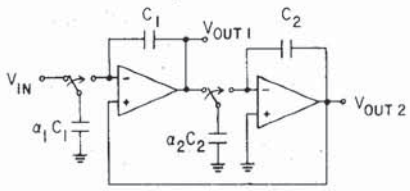


Fig. 4. Version 2 filter which has low sensitivity to the capacitor ratios α_1 and α_2.

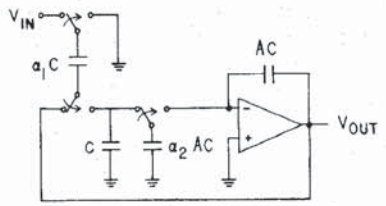


Fig. 5. Version 3 filter which only requires a single amplifier.

sults are found to hold for Q. The highest sensitivity is the Q sensitivity of α_1 which is approximately given by

$$S_{\alpha_1}^{Q} = 2\pi \frac{f_0 Q}{f_c}. \tag{12}$$

Therefore for high Q filters the clock rate required to obtain low sensitivity may be very high.

Version 2: The filter shown in Fig. 4 does not have this high sensitivity to Q. With this filter the sensitivities remain at 0.5 even for high Q filters. The single feedback line through the noninverting input of the first integrator simultaneously performs the overall negative feedback around both integrators as well as the local feedback around the second integrator. This makes possible a reduction in circuit complexity in comparison to version 1. The transfer function at the bandpass output V_{out1} of the version 2 filter is

$$\frac{V_{out1}(z)}{V_{in}(z)} = \frac{-\alpha_1 (z-1)}{z^2 - (2 - \alpha_1\alpha_2 - \alpha_2) z + (1 - \alpha_2)}. \tag{13}$$

The low-pass output V_{out2} has the transfer function,

$$\frac{V_{out2}(z)}{V_{in}(z)} = \frac{\alpha_1\alpha_2}{z^2 - (2 - \alpha_1\alpha_2 - \alpha_2) z + (1 - \alpha_2)}. \tag{14}$$

The design formulas for this filter are

$$\alpha_2 = 1 - e^{-(2\pi f_0/Qf_c)} \tag{15a}$$

$$\alpha_1 = \frac{2\left[1 - e^{-(\pi f_0/Qf_c)} \cos\left(\frac{\pi f_0}{f_c}\sqrt{4 - \frac{1}{Q^2}}\right)\right]}{1 - e^{-(2\pi f_0/Qf_c)}} - 1. \tag{15b}$$

A disadvantage of this low sensitivity filter is that in order to obtain a high value of Q (greater than 100) the capacitor ratios can become quite large (also greater than 100) which requires a large amount of silicon area. This tradeoff between the size of the capacitor ratio and sensitivity appears to be a basic property of the sampled data state variable filter approach.

Version 3: Both versions 1 and 2 use two operational amplifier integrators to realize two poles. One of the amplifiers can be replaced by a capacitor (unswitched) to yield the single amplifier low-pass filter shown in Fig. 5.

There is charge sharing between all the capacitors in this circuit so that the design of this filter is somewhat more complicated. The transfer function for this filter is

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{k\alpha_1\alpha_2}{z^2 - z(k+1) + k(1 + \alpha_1\alpha_2)} \tag{16a}$$

where

$$k = \frac{1}{(1+\alpha_1)(1 + A\alpha_2)}. \tag{16b}$$

This filter has sensitivity characteristics which are similar to version 1. The complete sensitivity expressions are quite involved and are available in [6]. Since there are three design variables α_1, α_2, and A, there is an extra degree of freedom in this second-order filter which can be removed by requiring the filter design to have the lowest possible sensitivity. It can be shown that this sensitivity optimum occurs when $\alpha_2 \approx 2$, and for $f_0 << f_c$ and $Q >> 1$ the filter sensitivities are approximately given by ($\theta = 2\pi f_0/f_c$),

$$S_{\alpha_1}^{f_0} = \frac{1}{4}\left(1 - \frac{3\theta^2}{2}\right) \tag{17a}$$

$$S_{\alpha_2}^{f_0} = S_A^{f_0} = \frac{1}{4}(1 - \theta^2) \tag{17b}$$

$$S_{\alpha_1}^{Q} = Q\theta\left(\frac{1 - \theta^2}{2 - \theta^2}\right) \tag{17c}$$

$$S_{\alpha_2}^{Q} = S_A^{Q} = \frac{Q\theta}{2}. \tag{17d}$$

A design procedure for this filter is as follows: first, choose a value of α_2; then calculate the value of k from the expression,

$$k = 2\exp\left[-\frac{\pi f_0}{Qf_c}\right]\cos\left[\frac{\pi f_0}{f_c}\sqrt{4 - \frac{1}{Q^2}}\right] - 1; \tag{18a}$$

finally, using the above values of k and α_2, calculate α_1 and A.

$$\alpha_1 = \frac{1}{\alpha_2}\left(\frac{1}{k}\exp\left[-\frac{2\pi f_0}{Qf_c}\right] - 1\right) \tag{18b}$$

$$A = \frac{1}{\alpha_2}(k^{-1}(1+\alpha_1)^{-1} - 1). \tag{18c}$$

For medium to low Q filters (i.e., $Q < 50$) the low Q sensitivity of version 2 is not required and thus the reduction in circuit complexity achieved with this design gives it a distinct advantage over the other two versions.

IV. Practical Design Considerations

A. Limitations

The only deviation from ideal operation considered so far has been the finite accuracy of the capacitance ratios. In this section the effect of the MOSFET switch and amplifier limitations will be discussed.

It is desirable to have the clock (sample) rate as high as pos-

sible relative to the filter passband frequencies in order to reduce the aliasing of the input signal (and to reduce the requirements on any antialiasing filter that may be required). The filters which have been described in the previous section are particularly amenable to high sample rate operation, because their sensitivity to parameter variations *decreases* as the clock rate is increased. However, the size of the capacitor ratios required for a given frequency response also increases with clock rate, which increases the silicon area requirements.

Since the operational amplifier is connected as an integrator, the amplifier only needs to respond to the change in signal which occurs each clock cycle. If the sample rate is high compared to the filter passband frequency then this change in voltage will be small. The slew rate requirement of the amplifier is therefore primarily dependent on the rate of change of the output signal at the passband frequencies. For related reasons, the settling time of the integrators will in general be much shorter than the large signal settling time of the amplifier connected in unity gain (which is the number usually quoted in amplifier specifications).

At very high sample rates (higher than most amplifiers would allow) the time constant of the switched capacitors will become important. This time constant is determined by the on resistance of the switches (typically several kilohms) and the value of the switched capacitances (tens of picofarads) which yields a time constant on the order of tens of nanoseconds.

Another important characteristic of the amplifier is the open-loop gain A_v. The required value for this gain is very dependent on the frequency response of the filter. As a general rule, in order for there to be a low sensitivity to A_v, A_v should be much larger than the Q of the circuit. Thus for a filter with a Q of 70 the gain should be greater than 700, while for a Q = 1 filter the gain need only be greater than 10. If these minimum values of gain are used then the capacitor ratios should be determined including the effect of the finite gain. The design equations for the version 3 filter which were given in (18a)-(18c) must therefore be modified when a finite amplifier gain is included,

$$k = \frac{2A_v \exp\left[-\frac{\pi f_0}{Qf_c}\right]\cos\left[\frac{\pi f_0}{f_c}\left(4 - \frac{1}{Q^2}\right)^{1/2}\right] - A_v\eta + \alpha_2\gamma - \exp\left[-\frac{2\pi f_0}{Qf_c}\right]}{A_v + \gamma\alpha_2 - \eta} \tag{19a}$$

$$\alpha_1 = \frac{1}{\gamma\alpha_2}\left(\frac{1}{k}\exp\left[-\frac{2\pi f_0}{Qf_c}\right] - \eta\right) \tag{19b}$$

$$A = \frac{1}{\alpha_2}\left[\frac{1}{k(1+\alpha_1)} - 1\right] \tag{19c}$$

where

$$\gamma = 1 - \frac{1+\alpha_2}{A_v} \tag{20a}$$

$$\eta = 1 - \frac{\alpha_2}{A_v}. \tag{20b}$$

The final important limitation is the thermal noise contributions of the amplifier and switches which dominate over all other noise sources. If the amplifier noise is modeled as a noise source at the positive input to the integrator amplifier it is apparent that, in addition to a direct feedthrough, the noise voltage will be sampled and stored on the integrating capacitors. If at any frequency there is gain in the filter then the sampled component of the amplifier noise will also be amplified. The other noise contribution is due to the thermal noise of the MOSFET switches which is sampled onto the switched capacitors. This results in a rms noise contribution from each switching operation of $(kT/C)^{1/2}$, where C is the switched capacitance and kT is the thermal voltage. This noise can be minimized by increasing the size of the switched capacitors.

B. MOS Amplifier Design

Since the amplifier requirements for low and high Q filters are quite different, two amplifier designs were performed. The first is a new operational amplifier design with a gain of 6000, while the second is a simple differential pair with a gain of 40. The advantage of using a simple amplifier for low Q filters is the savings achieved in circuit area (which was about a factor of 2.5).

The main problem of single-channel MOS amplifiers is the low gain per gain stage. For this reason depletion-type loads were used which inherently offer more gain than enhancement loads [13]. A single-channel NMOS operational amplifier with depletion loads is shown in Fig. 6. The input stage $M1, M2$, $M3$, and $M4$ is a single-ended differential amplifier. This is followed by the level shifter $M8$, $M9$ which drives the main gain stage. The transconductance of the driver transistor $M10$ has been increased by adding the current source $M11$, $M12$, which provides more dc bias current for $M16$ and thus increases the total gain of this stage. The transistor $M13$ (common-gate configuration) isolates the load device $M14$. The output stage $M17$, $M18$ is connected as a push-pull driver but the main gain stage has so much gain that $M18$ basically operates as a source follower with $M17$ as the load.

Frequency compensation is accomplished by an on-chip Miller capacitor C_c = 6 pF. This compensation capacitor has not been connected directly to the output of the main gain stage because this would introduce a right-half plane zero due to signal feedforward. Instead C_c has been connected to another push-pull driver ($M15$, $M16$) following the main gain stage. This configuration has the advantage that the main gain stage is essentially bypassed at high frequencies; otherwise the Miller capacitor C_c would have been applied over too many poles. The dominant pole of the amplifier is then determined by C_c multiplied by the gain of the main stage and load impedance of the input stage ($M3$).

The circuit has been designed so that its operation is largely independent of the threshold voltage variations. Configura-

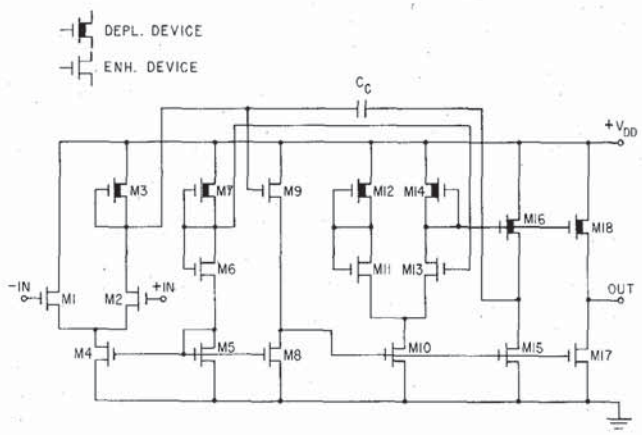


Fig. 6. Single-channel NMOS operational amplifier with depletion loads.

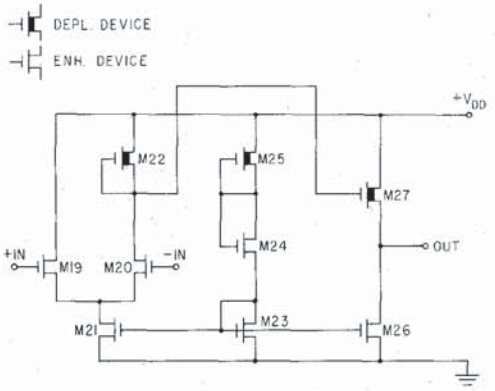


Fig. 7. Single-channel NMOS differential pair with depletion loads.

tions and geometries were selected in such a way that all quiescent voltages through the amplifier track the quiescent voltages of the bias string *M*5, *M*6, *M*7. This assures that all devices will be in saturation even for large threshold voltage variations.

As mentioned above for low Q filters an amplifier with only moderate gain is needed. For such filters a relatively simple differential amplifier which is shown in Fig. 7 has been designed. The amplifier consists of the differential input stage *M*19, *M*20, *M*21, and *M*22, the output stage *M*26, *M*27 and the bias string *M*23, *M*24, *M*25. This amplifier is the same design as the input stage to the operational amplifier of Fig. 6.

Table I contains the *w*/*l* ratios for all the MOSFET's in the two amplifiers and in Table II the measured performance of a sample of five amplifiers is given.

TABLE I
MASK DEVICE DIMENSIONS

Device	w(μm)	ℓ(μm)
M1	250	20
M2	250	20
M3	10	30
M4	35	20
M5	15	20
M6	10	25
M7	10	30
M8	15	20
M9	10	25
M10	165	20
M11	107.5	25
M12	107.5	30
M13	10	25
M14	10	30
M15	165	20
M16	122.5	30
M17	165	20
M18	122.5	30
M19	250	20
M20	250	20
M21	35	20
M22	10	30
M23	15	20
M24	10	25
M25	10	30
M26	165	20
M27	122.5	30

V. EXPERIMENTAL RESULTS

Two version 3 filters (Fig. 5) have been fabricated. One was designed to be a high Q filter with $Q = 73.1$ at a center frequency of $f_0 = 0.0366\, f_c$, while the second has the relatively low Q of 0.99 at a center frequency of $0.0165\, f_c$.

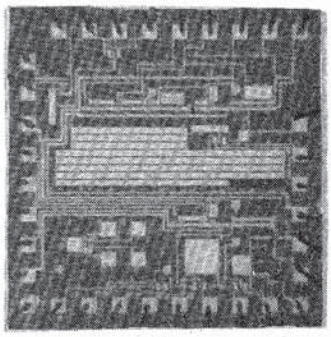
A. Description of the IC

The photograph of the completed IC is shown in Fig. 8. The overall IC size is 76 × 76 mil including contact pads. Filter I ($Q = 73$) uses the operational amplifier shown in Fig. 6. The amplifier area is 636 mil^2 and the total filter occupies an area of 2050 mil^2. Filter II ($Q = 1$) has an area of 784 mil^2 including the differential pair which occupies 320 mil^2. A 10-μm minimum feature size and 2.5-μm minimum alignment tolerance were used. The thin-oxide thickness was 1000 Å for capacitor dielectrics (grown over n^+) and 700 Å for transistor gates.

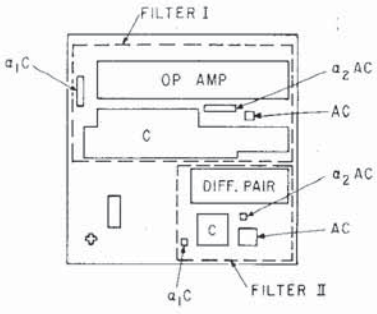
The process used an n-channel Al-gate MOS technology. The

TABLE II
PERFORMANCE PARAMETERS OF AMPLIFIERS POWER SUPPLY +15 V AND SUBSTRATE BIAS -2.5 V

	OP. AMP.	DIFF. PAIR
Input offset voltage mean	49 mV	36.5 mV
Input offset voltage standard deviation	9 mV	20 mV
Low frequency gain mean	6000	40
Low frequency gain standard deviation	290	1
Common-mode rejection ratio	60 dB	56 dB
Unity-gain frequency	2 MHz	3.4 MHz
Slew rate	2 V/μs	2 V/μs
Power supply rejection ratio	48 dB	38 dB
Input noise voltage (up to 100 kHz)	45 μV	38 μV
Output voltage swing	+0.4 V,+14.3 V	+5.4 V,+14.
Power consumption	13 mW	5 mW



(a)



(b)

Fig. 8. (a) Photograph of the integrated circuit. (b) Layout block diagram of (a).

starting material was lightly doped ($C_B = 5 \times 10^{14}\,\mathrm{cm}^{-3}$) p-type silicon with ⟨100⟩ crystal orientation. Therefore p^+ isolation diffusion was necessary in order to increase the threshold voltage of the parasitic thick oxide transistors. Further the whole wafer was implanted with boron (does $7.8 \times 10^{11}/\mathrm{cm}^2$, energy 50 keV) so that the threshold voltages of all enhancement devices would be near 0 V with zero-body bias. The depletion devices were implanted with phosphorous with a dose of $2.1 \times 10^{12}/\mathrm{cm}^2$ at an energy of 150 keV. The threshold voltage of the depletion loads is near -3 V with zero-body bias.

The capacitor areas were defined solely by the metal pattern. The area ratios of the capacitors are as follows:

TABLE III
FILTER PERFORMANCE

		Filter I	Filter II
Clock rate f_c		102.4 kHz	16 kHz
Calculated:	center frequency f_0	3.75 kHz	264 Hz
	selectivity Q	73.14	0.99
Measured:	center frequency mean	3.715 kHz	287 Hz
	center frequency standard deviation	13 Hz	1 Hz
	selectivity mean	71.2	0.97
	selectivity standard deviation	2.2	0.004
	output wideband noise (rms)	0.85 mV	160 μV

Filter I: $\alpha_1 = 0.028, \alpha_2 = 1.99, \; A = 0.015$

Filter II: $\alpha_1 = 0.06, \; \alpha_2 = 0.182, A = 0.295.$

Because of higher sensitivity of Q to coefficients for filter I (high Q) an effort has been made to make the ratio of capacitor perimeters the same as the ratio of the areas. This minimizes the dependence of the area ratio on the etching of the metal pattern. The smallest capacitor used in filter I was 2 pF and was 1 pF in filter II.

B. Performance

A summary of the calculated and measured performance parameters obtained from five filters from three different wafers appears in Table III. The agreement is excellent between theory and measurements. The high Q filter has a sensitivity of 10 for the value of Q, thus the measured 3 percent variation in Q corresponds to a 0.3 percent accuracy of the capacitance ratio. Filter II has a sensitivity of 1 to most of the ratios which results in the 0.3 percent variation of the Q and center frequency of that filter.

In filter II there was an 8 percent discrepancy between the calculated and the measured mean value of the center frequency f_0. This error was due to an error in layout in which

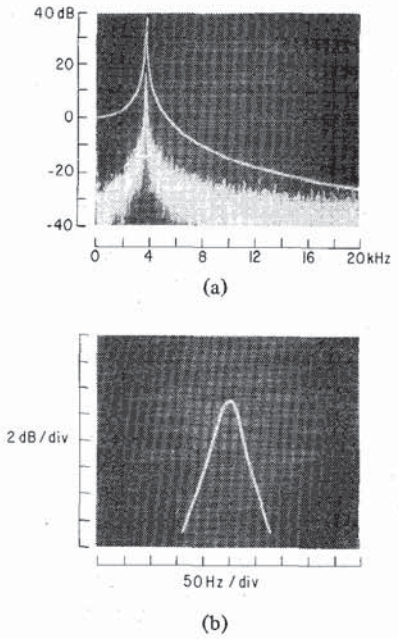


Fig. 9. (a) Frequency response and noise spectral density (amplified by 30 dB) of filter I, operated at a clock rate of 102.4 kHz. (b) Detail of the peak of the response in (a).

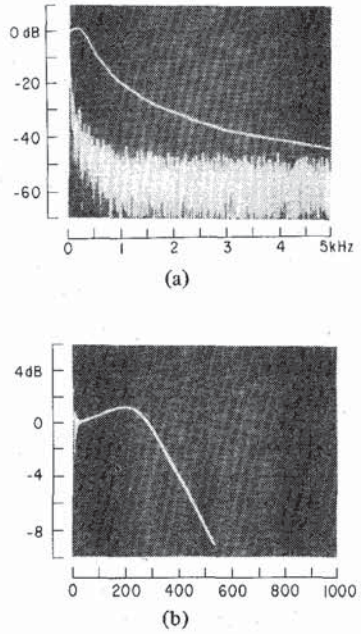


Fig. 10. (a) Frequency response and noise spectral density (amplified by 30 dB) of filter II, operated at a clock rate of 16 kHz. (b) Detail of the response in (a) at low frequencies.

long metal leads connected the switches and the top plates of the smallest capacitors (which were approximately 1 pF). This increased the value of these switched capacitors by about 8 percent. This error could have been reduced during layout in three ways: reduce the length of the metal leads; increase the size of the capacitors; and take the effect of this parasitic into account since it will be a constant for a given layout of the metal leads. More care in layout was taken in filter I with the result that even though the sensitivity was 10 times higher for this filter the response was closer to the design goals.

The clock rates which were used to take data were 102.4 kHz for filter I and 16 kHz for filter II. These rates were chosen in order to be compatible with a systems application, however insignificant variations were noticed in the performance for clock rates which ranged from 100 Hz to 500 kHz. At low frequencies leakage currents limited the operation while the high frequency end was limited by the clock drivers which were used. Also, it was found that the width of the clock pulses could be reduced to less than 0.2 μs without any degradation of performance.

In the top trace in Fig. 9(a) the frequency response of filter I is shown. The reference level of 0 dB at dc corresponds to 0 dB insertion loss through the filter. The peak of the response is a factor of Q times larger ($Q \approx 73.14$ yields 37.3 dB). Also shown in Fig. 9(a) is the noise spectral density with a 30-Hz bandwidth in which the scale has been increased by 30 dB. As expected because of the 37.3 dB gain of the filter at the center frequency the noise also shows a peak at f_0. An expanded scale of the region near the peak of the filter response is shown in Fig. 9(b). The very narrow 3-dB width of $\approx$50 Hz can be seen around the center frequency of 3715 Hz.

In the upper curve in Fig. 10(a) the response of filter II is shown and in Fig. 10(b) the response on an expanded scale at low frequencies is shown. Also shown in Fig. 10(a) is the noise of the filter after an amplification of 30 dB (bandwidth of 30 Hz). Since this filter has very little gain in the passband the noise is not amplified, however the $1/f$ noise of the input MOSFET's of the amplifier can be seen.

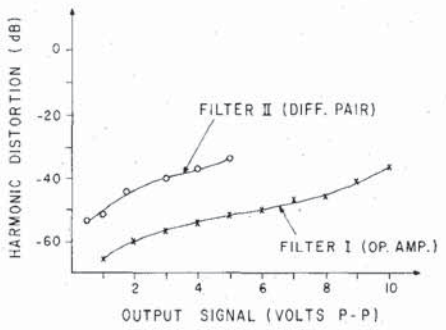


Fig. 11. Harmonic distortion of both filters as a function of the output signal (signal frequency is 3.715 kHz for filter I and 100 Hz for filter II).

In order to define the dynamic range it is necessary to determine the dependence of the total harmonic distortion on signal size. In Fig. 11 the harmonic distortion is plotted as a function of the output signal for both filters. It is clearly seen that the high gain of the operational amplifier used in filter I results in larger output swings with decreased harmonic distortion in comparison to filter II with the differential pair amplifier.

VI. Conclusions and Future Developments

Three different versions of a new analog sampled data filtering approach based on state variable design techniques have been discussed. An important advantage of this approach is

that monolithic high Q filters can be implemented using single-channel MOS technology. Two low-pass second-order filters have been designed and fabricated and the experimental results confirm the theoretical considerations presented.

The switched integrators which were used to implement these filters have application in many other organizations. A particularly interesting one for implementing more complex frequency response functions is the use of leapfrog or active-ladder synthesis techniques [14]. The two pole filters described in this paper are actually a limiting form of the leapfrog method which can be used to synthesize any number of poles and zeros with very low sensitivity.

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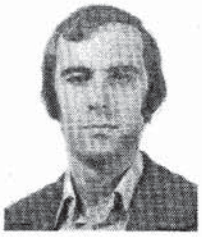

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Paul R. Gray (S'65–M'69–SM'76), for a photograph and biography, see p. 90 of the April 1977 issue of this JOURNAL.