1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

DYNETIX DESIGN SOLUTIONS INC., a California corporation, Plaintiff, v. SYNOPSYS INC., a Delaware corporation, and DOES 1-50, Defendants.	Case No.: CV 11-05973 PSG **ORDER GRANTING-IN-PART DEFENDANT'S MOTION FOR SUMMARY JUDGMENT OF NON-INFRINGEMENT OF VCS MULTICORE AND GRANTING MOTION FOR SUMMARY JUDGMENT OF NON-INFRINGEMENT OF VCS CLOUD** **(Re: Docket Nos. 136, 141)**

In this patent infringement case, Defendant Synopsys Inc. ("Synopsys") moves for

summary judgment of non-infringement on both the allegedly infringing features of its VCS tool

("VCS Multicore") and VCS Cloud.[1] Plaintiff Dynetix Design Solutions Inc. ("Dynetix") opposes.

The parties appeared for a hearing on the matter. Having reviewed the papers and considered the

arguments of counsel, the court GRANTS-IN-PART Synopsys' motion on VCS Multicore and

GRANTS Synopsys' motion on VCS Cloud.

---

[1] See Docket Nos. 136, 141.

1

Case No.: C 11-05973 PSG
ORDER RE DEFENDANT'S MOTIONS FOR SUMMARY JUDGMENT

I. BACKGROUND

On December 5, 2011, Dynetix filed this suit, alleging that Synopsys infringes Dynetix's patent, United States Patent 6,466,898 ("the '898 patent").[2] Dynetix and Synopsys are both electronic design automation ("EDA") companies, involved in creating software tools to design and test integrated circuits.[3] The '898 patent discloses a multithread HDL logic simulator that can process both VHDL and Verilog languages in a single program and use special algorithms to accelerate performance on multiprocessor systems.[4]

VCS is an EDA tool and a logic simulator.[5] As previously mentioned, Dynetix accuses both the multicore features of VCS and VCS Cloud. VCS Multicore features two levels of parallelism: Design Level Parallelism ("DLP") and Application Level Parallelism ("ALP").[6] DLP allows the user to run a parallel simulation by dividing the circuit design under testing ("DUT") into multiple partitions, then simulating those partitions on different threads.[7] A partition is comprised of a group of components within the circuit design. ALP allows the user to run simulations in parallel with other applications.[8] VCS Cloud is a prototype software program intended to allow customers to access and execute Synopsys tools on third party cloud-computing resources, but was terminated and never commercialized.[9]

---

[2] See Docket No. 1. Synopsys filed an answer and cross-complaint denying infringement of Dynetix's patent and claiming that Dynetix's products infringe two of Synopsys's patents. See Docket No. 58.

[3] See Docket No. 1 ¶ 8; Docket No. 64 ¶ 3.

[4] '898 Patent at 1. Dynetix has asserted 18 claims of the '898 patent: claims 1-3, 5-7, 19-23, 36, 37, 39, 44, 45, 48, and 53. See Docket No. 143, Ex. B.

[5] See Docket No. 142 ¶ 8.

[6] See id. ¶ 9-10.

[7] See Docket No. 64 ¶ 2.

[8] See id. ¶ 17.

[9] See Docket No. 137 ¶¶ 2-4.

2

Case No.: C 11-05973 PSG
ORDER RE DEFENDANT'S MOTIONS FOR SUMMARY JUDGMENT

On September 3, 2012, Synopsys moved for partial summary judgment of non-infringement ("first motion for summary judgment"), challenging that Dynetix cannot prove VCS Multicore infringes claims 1-3, 5-7, 36, 37, 39, 44, 45, 48, and 53 ("the parallel simulation claims") by automatically detecting the number of available processors to create threads.[10] The court granted Synopsys' motion for summary judgment as to ALP, but found triable issues of fact as to DLP.[11]

Synopsys later brought two additional motions for summary judgment, alleging that VCS Multicore does not infringe the parallel simulation claims ("second motion for summary judgment") by achieving either linear to super-linear scalable performance speedup or superlinear scalable simulation, and that VCS Cloud does not infringe claims 19-23 ("the remote access claims") ("third motion for summary judgment").[12] The court addresses Synopsys' second and third motions for summary judgment here.

II.   LEGAL STANDARDS

Summary judgment is appropriate only if there is "no genuine dispute as to any material fact and the movant is entitled to judgment as a matter of law."[13] The moving party bears the initial burden of production by identifying those portions of the pleadings, discovery and affidavits which demonstrate the absence of a triable issue of material fact.[14] If, as here, the moving party is the defendant, he may do so in two ways: by proffering "affirmative evidence negating an element of the non-moving party's claim," or by showing the non-moving party has insufficient evidence to

---

[10] See Docket No. 62.

[11] See Docket No. 297.

[12] See Docket No. 136, 141.

[13] See Fed. R. Civ. P. 56(a).

[14] See Fed. R. Civ. P. 56(c)(1); Celotex Corp. v. Catrett, 477 U.S. 317, 323 (1986).

3

Case No.: C 11-05973 PSG
ORDER RE DEFENDANT'S MOTIONS FOR SUMMARY JUDGMENT

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28

establish an "essential element of the non-moving party's claim."[15] If met by the moving party, the

burden of production then shifts to the non-moving party, who must then provide specific facts

showing a genuine issue of material fact for trial.[16] The ultimate burden of persuasion, however,

remains on the moving party.[17] In reviewing the record, the court must construe the evidence and

the inferences to be drawn from the underlying evidence in the light most favorable to the non-

moving party.[18]

　　　　Under Rule 56(d), if the nonmovant cannot, for specified reasons, present facts essential to

justify its opposition to the motion, "the court may (1) defer considering the motion or deny it; (2)

allow time to obtain affidavits or declarations or to take discovery; or (3) issue any other

appropriate order."[19] This requires the nonmovant to show "(1) the specific facts that they hope to

elicit from further discovery, (2) that the facts sought exist, and (3) that these sought-after facts are

"essential" to resist the summary judgment motion."[20] The nonmovant must also demonstrate that

he diligently pursued previous discovery opportunities.[21]

　　　　To infringe a claim, each claim limitation must be present in the accused product, literally

or equivalently.[22] Patent infringement is a two-step process: first, the court must construe the

asserted claims; then, the court must compare the accused products with the construed claims and

---

[15] Celotex Corp., 477 U.S. at 331.

[16] See id. at 330; *T.W. Elec. Service, Inc. v. Pac. Elec. Contractors Ass'n*, 809 F.2d 630, 630 (9th Cir. 1987).

[17] Id.

[18] See Anderson, 477 U.S. at 248; Matsushita Elec. Indus. Co., Ltd. v. Zenith Radio Corp., 475 U.S. 574, 587 (1986).

[19] See Fed. R. Civ. P. 56(d).

[20] See Family Home and Fin. Ctr., Inc. v. Fed. Home Loand Mortg. Corp., 525 F.3d 822, 827 (9th Cir. 2008).

[21] See Bank of Am., NT & SA v. PENGWIN, 175 F.3d 1109, 1118 (9th Cir. 1999).

[22] See Dawn Equip. Co. v. Kentucky Farms, Inc., 140 F.3d 1009, 1014 (Fed. Cir. 1998).

4

determine whether the products contain each limitation of the claims, either literally or equivalently.[23] A product literally infringes if it contains each element and limitation of the patent claim as construed.[24] A product may also infringe under the doctrine of equivalents, which applies if the element in the accused device performs substantially the same function, in substantially the same way, to obtain substantially the same result as the element claimed in the patent.[25]

III.   DISCUSSION

A.   Whether VCS Multicore Infringes the Parallel Simulation Claims

As noted above, the focus of Synopsys' second motion for summary judgment of non-infringement is that VCS Multicore does not achieve "linear to super-linear scalable performance speedup" or "super-linear scalable simulation," as required by the claim language.[26]

Of the thirteen parallel simulation claims Dynetix asserts are infringed by VCS Multicore, only claims 1, 36, and 45 are independent. Claim 1 recites:[27]

> 1. A method of performing multithreaded event-driven logic simulation of an integrated circuit design, coded in one or a plurality of Hardware Description Language ("HDL") languages including VHDL, Verilog languages and a mixed thereof on a multiprocessor platform, comprising the steps of:
> […]
> (c) automatically detecting the number of microprocessors (CPUs) available on the multiprocessor platform to create a master thread and a plurality of slave threads for concurrent execution of the multithreaded event-driven simulation of the design **to achieve linear to super-linear scalable performance speedup as according to the number of CPUs on the multiprocessor platform.**

Claim 36 and 45 contain similar claim language:[28]

---

[23] See Freedman Seating Co. v. American Seating Co., 420 F.3d 1350, 1356-57 (Fed. Cir. 2005).

[24] See id. at 1357.

[25] See Abbott Laboratories v. Sandoz, Inc., 566 F.3d 1282, 1296-97 (Fed. Cir. 2009).

[26] See Docket No. 141 at 4.

[27] '898 Patent, col. 23, ll. 8-28.

[28] Id., col. 28, ll. 28-48 and col. 29, ll. 35-56.

5

Case No.: C 11-05973 PSG
ORDER RE DEFENDANT'S MOTIONS FOR SUMMARY JUDGMENT

36. A method of **achieving super-linear scalable** Hardware Description Language simulation for a multithreaded event-driven simulation of a circuit design on a multiprocessor platform, comprising the steps of:

45. A program product of **achieving super-linear scalable** Hardware Description Language simulation for a multithreaded event-driven simulation of a circuit design on a multiprocessor platform, comprising the steps of:

There are two issues raised by Synopsys' present challenge: (1) whether VCS Multicore achieves "linear to super-linear" performance speedup, and (2) whether the performance speedup is "scalable."

1. "Linear to Super-Linear" Performance Speedup

Synopsys first argues that DLP does not achieve "linear to super-linear" speedup. The court construed the terms as follows:

The terms linear and super-linear describe the speedup that a parallel simulation will achieve when performing on hardware containing one or more processing units.

A simulation is linear if the speedup that is achieved is equal to the number of available processing units. For example, a simulation that runs two times as fast on hardware containing two processing units is linear. Similarly, if the simulation runs four times as fast on four processing units, it is again linear.

A simulation that has a speedup greater than the number of processing units is super-linear. For example, in a process executed on two processing units runs three times as fast as the same simulation on one processing unit, it is super-linear.[29]

Synopsys submits pre-release DLP test results as well as a declaration from its engineer Pallab Dasgupta showing the speedup is never linear to super-linear.[30] Synopsys attributes this limitation to the challenge of coordinating communication and synchronization across multiple partitions.[31] Dynetix, however, points to other test data presented at a VCS summit meeting in March 2008[32] that its expert Dr. Minesh Amin ("Amin") interprets as showing the required speedup for most test

---

[29] Docket No. 121 at 174, ll. 8-23.

[30] See Docket No. 142 ¶ 19, Ex. A.

[31] See id. ¶ 15.

[32] See Docket No. 168 ¶ 63, Ex. 10 at 27243-44.

6

Case No.: C 11-05973 PSG
ORDER RE DEFENDANT'S MOTIONS FOR SUMMARY JUDGMENT

cases up to about 8 processors.[33] On this evidence alone, this appears to be a factual dispute among experts – one best left to the trier of fact.

Even if this were not enough, the court must also note and consider Dynetix's Rule 56(d) request asserting that at the time this motion was filed, Synopsys had not yet provided Dynetix with the code of VCS Multicore Dynetix needed to conduct its own performance tests.[34] In a case involving a method patent for computerized weather forecasting, the Federal Circuit recently reversed the district court's grant of summary judgment despite plaintiff's Rule 56(d) request, which asserted the plaintiff needed defendant's source code to adequately oppose the motion for summary judgment.[35] The Federal Circuit held that although the defendant maintained that the source code was irrelevant, "[e]xamining the source code would have enabled [the plaintiff] to determine if [the defendant]'s noninfringement position was correct—which [the plaintiff] believed to not be the case."[36] The plaintiff was entitled to a "reasonable chance to disprove [the defendant's] position on noninfringement," and thus summary judgment was inappropriate.[37] Similarly, here, Dynetix did not have access to Synopsys' code to aid its efforts to oppose Synopsys' summary judgment. Although Dynetix requested the code from Synopsys in February

---

[33] See id. Amin also prepared a table from performance test data in an August 2007 Synopsys presentation. See Docket No. 168-1 ¶ 57, Ex. 7 at 27598. While Synopsys raises serious doubts as to the legitimacy of Amin's table reflecting the August 2007 presentation because it is unsupported by the underlying evidence – the underlying data does not mention the number of available rather than participating processors, see Docket No. 205 at 5-6 and Docket No. 183 at 2-3 – Synopsys never specifically challenges the March 2008 summit test data. Construed in the light most favorable to the non-moving party, as it must be under Rule 56, the underlying March 2008 summit data and Amin's opinion creates a triable issue of infringement of the parallel simulation claims.

[34] See Docket No. 168-1 ¶ 14.

[35] See Baron Servs., Inc. v. Media Weather Innovations LLC, Case No. 2012-1285, 2013 WL 1876511 (Fed. Cir. May 7, 2013), at *5-6.

[36] Id. at *5.

[37] Id.

7

Case No.: C 11-05973 PSG
ORDER RE DEFENDANT'S MOTIONS FOR SUMMARY JUDGMENT

2012,[38] it was only provided on November 16, 2012,[39] and even then Dynetix was not able to run it because it did not have the necessary license keys and enabling devices.[40] Dynetix later was forced to file a motion to compel production of full access to the executable code, which the court granted.[41] Without the opportunity to conduct its own tests at the time the opposition was due, Dynetix was unfairly disadvantaged in refuting Synopsys' assertions regarding the code.[42]

2. "Scalable"

Synopsys next argues that DLP does not achieve "scalable" performance. The court interpreted "scalable performance" to mean that "there is a consistent increase in performance for each added processing unit."[43] Synopsys contends that VCS Multicore does not exhibit any such consistent increase as processing units are added. Synopsys' expert explains that as DLP creates one thread for each partition and one additional thread for the remainder of the circuit,[44] in a scenario where the DUT is already partitioned and contains only four partitions, DLP will not create more than five threads.[45] Synopsys acknowledges that as the number of processors increases from one to five, DLP would experience consistent speedup.[46] However, due to the limitations of the particular design identified by Synopsys, DLP would not continue to experience that speedup

---

[38] See Docket No. 168-1 ¶ 2. See also Docket No. 38 at 2.

[39] See Docket No. 168-1 ¶ 9.

[40] See id. ¶ 10-13.

[41] See Docket No. 256.

[42] Cf. Baron Services, Inc., 2013 WL 1876511, at *5-6.

[43] Docket No. 121 at 174, ll. 23-25.

[44] See Docket No. 142 ¶ 13.

[45] See id. ¶ 15.

[46] See id.; See also Docket No. 141 ("DLP may achieve some increase in performance for each microprocessor on which a thread is executed, but it will not achieve a consistent increase in performance for additional microprocessors beyond the number of threads.").

8

1

2

past five microprocessors. In other words, even if the number of microprocessors were increased to eight, DLP would not utilize more than five separate microprocessors.

3

4

5

6

7

8

9

10

11

12

13

Synopsys urges the court to hold as a matter of law that DLP cannot infringe if it practices "scalable," or "consistent" performance speedup only up to a number of microprocessors rather than across the entire range of zero to infinity. But nothing in the claim language or the court's claim construction of "scalable" defines the range, but merely requires that within the applicable range, the performance speedup be "consistent." The question of whether the scalable performance speedup must occur over at least five, ten, or twenty additional processors is for the jury, and not the court, to determine. Moreover, Synopsys misses the point. It is irrelevant to point out scenarios in which the accused product might not infringe; "an accused product that sometimes, but not always, embodies a claimed method nonetheless infringes."[47] As long as the accused product sometimes practices every step of the claim, it will infringe.[48]

14

15

16

17

18

19

20

21

22

Although ALP is now no longer at issue in this case, Synopsys brought its motion for summary judgment against ALP as well and so in the interest of completeness, and in light of the pending motion for reconsideration, the court addresses ALP briefly here. ALP does not partition a simulation but runs the entire DUT on a single thread.[49] The parallelism of ALP is in running the simulation in parallel with other applications, not running different parts of the simulation in parallel on different microprocessors.[50] Accordingly, it appears undisputed that ALP does not increase the speed of the simulation itself.[51] Dynetix presents no evidence to the contrary because

23

24

[47] Bell Communication Research, Inc. v. Vitalink Communications Corp., 55 F.3d 615, 622 (Fed. Cir. 1995).

25

[48] See id.

26

[49] See Docket No. 142 ¶ 17.

27

[50] See id.

28

[51] See id. ¶ 18.

9

its consolidated opposition contains no argument as to ALP.[52] As a result, even if ALP were still at issue, no reasonable jury could find that it infringes, rendering Synopsys' second summary judgment motion of non-infringement on VCS Multicore warranted at least as to ALP.

B.   Whether VCS Cloud Infringes the Remote Access Claims

Synopsys' third motion for summary judgment of non-infringement asserts that VCS Cloud does not infringe the remote access claims because it does not use a graphical user interface ("GUI") but rather uses a command line interface.   The court construed a GUI as "a computer user interface that allows interaction using graphical objects such as icons, images, and windows as opposed to merely a command line interface."[53]

Of the remote access claims, claims 19 and 23 are independent, while claims 20-22 are dependent on claims 19. Claim 19 provides:[54]

> 19. A method of executing remote Hardware Description Language ("HDL") compilation and multithreaded simulation (event-driven, cycle-based, and a combination of both) of a circuit design employing a user's local and remote single-processor or multiprocessor hosts, comprising the steps of:
> […]
> **installing and executing a graphical user interface program ("GUI") on the user's local host to specify remote hosts** on which the HDL design compilation and simulation is to be performed;
> **automatically activating network connection by the GUI** to the server program to send the user's commands from the user's local host to the remote hosts to be executed thereof;

Claim 23 also requires use of a GUI:[55]

> 23. A program product of executing remote Hardware Description Language ("HDL") compilation and multithreaded simulation of a circuit design employing a user's local and remote single-processor or multiprocessor hosts, comprising:
> […]

---

[52] See Docket No. 168 at 33-38.

[53] Docket No. 121 at 176, ll. 13-17.

[54] '898 Patent, col. 25, ll. 65-67, col. 26, 1-17.

[55] Id., col. 26, ll. 35-53.

10

Case No.: C 11-05973 PSG
ORDER RE DEFENDANT'S MOTIONS FOR SUMMARY JUDGMENT

1
2
3

means to provide a graphical user interface program ("GUI") on the user's local host to specify remote hosts on which the HDL design compilation and simulation is to be performed;
means to automatically activate network connection by the GUI to the server program to send the user's commands from the local host to the remote hosts to be executed thereof;

4

Synopsys presents undisputed evidence showing VCS Cloud does not meet these claim limitations.

5

6

The local host of VCS Cloud, Cloud Connections, offers a command line interface only.[56] The

7

program provides a command prompt and users may enter text commands.[57] This does not contain

8

"icons, images, or windows" and is specifically disclaimed in the court's interpretation as the

9

opposite of a GUI.[58]

10

Dynetix argues creatively that VCS Cloud at some point uses a Firefox web browser, which

11

is "unquestionably a GUI."[59] For example, Dynetix also points out a file in the source code which

12

appears to use an "automated mechanism" to "execute VCS in parallel." But even if that is true,

13

the plain language claims 19 and 23 require "means to automatically activate network connection

14

by the GUI to the server program." Activation of the network connection clearly refers to the

15

initialization of the connection between the local host and the remote host, not just any automatic

16

transmission used at some point in the process. Even Dynetix and Amin appear to admit that the

17

command line interface is used to access VCS Cloud.[60] As Dynetix has not provided any evidence

18

to contradict Synopsys' assertion, and in fact seems to admit it, Dynetix fails to carry the burden of

19

20

21

22

23

---

[56] See Docket No. 137 ¶ 4.

24

[57] See id.; See also Ex. A.

25

[58] Docket No. 121 at 176, ll. 13-17.

26

[59] Docket No. 168 at 39.

27

[60] See id.; Docket No. 168-1 ¶ 67 ("The command line interface referenced by Newell's declaration is just one interface, likely required at the beginning, to access VCS Cloud.").

28

11

Case No.: C 11-05973 PSG
ORDER RE DEFENDANT'S MOTIONS FOR SUMMARY JUDGMENT

opposing summary judgment with specific evidence showing a genuine issue of material fact for trial.[61]

Dynetix also fails to present evidence that VCS Cloud uses a GUI installed on a local host to specify remote hosts. This limitation, required by the plain language of claims 19 and 23, cannot be met by Dynetix's bare assertion that "[i]t is also impossible that VCS Cloud does not use GUI… VCS Cloud is simply VCS, which is based heavily on GUI and cannot be handled alone by a command line interface."[62] "Broad conclusory statements offered by [] experts are not evidence and are not sufficient to establish a genuine issue of material fact."[63]

Dynetix again points to its discovery woes and requests relief under Rule 56(d), but here the court is less sympathetic to Dynetix's plight. Dynetix concedes that the source code for VCS Cloud had been produced in October 2012, well before Synopsys' third motion for summary judgment was filed.[64] Its lament that "Dynetix has been busy with various urgent tasks in this case"[65] is not sufficient to deny this motion on Rule 56(d) grounds. Dynetix has not identified facts were justifiably "unavailable," and its actions demonstrate a lack of diligence.[66]

IV. CONCLUSION

Synopsys' motion for summary judgment of non-infringement of VCS Multicore is GRANTED-IN-PART and Synopsys' motion for summary judgment of non-infringement of VCS Cloud is GRANTED.

---

[61] See Celotex Corp., 477 U.S. at 330; T.W. Elec. Service, Inc., 809 F.2d at 630.

[62] Docket No. 168-1 ¶ 67.

[63] Telemac Cellular Corp., 247 F.3d at 1329.

[64] See Docket No. 168 at 40-41.

[65] Id. at 41.

[66] Fed. R. Civ. P. 56(d); See also Bank of Am., 175 F.3d at 1118.

12

IT IS SO ORDERED.

Dated: May 14, 2013

_____
PAUL S. GREWAL
United States Magistrate Judge

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28

Case No.: C 11-05973 PSG
ORDER RE DEFENDANT'S MOTIONS FOR SUMMARY JUDGMENT