UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

DYNETIX DESIGN SOLUTIONS INC., a California corporation, Plaintiff/Counter-defendant, v. SYNOPSYS INC., a Delaware corporation, and DOES 1-50, Defendants/Counter-claimant.	Case No.: CV 11-05973 PSG **ORDER DENYING COUNTER-DEFENDANT'S MOTION TO DISMISS AND MOTION FOR SUMMARY JUDGMENT OF NON-INFRINGEMENT** **(Re: Docket No. 87)**

In this patent infringement suit, Plaintiff Dynetix Design Solutions Inc. ("Dynetix") sued Defendant Synopsys Inc. ("Synopsys"), and Synopsys countersued, asserting its own set of patents (the "counterclaim"). Presently before the court is the Dynetix's motion to dismiss and alternatively, motion for summary judgment regarding Synopsys' counterclaim. Synopsys opposes. The parties appeared for hearing. Having reviewed the papers and considered the arguments of counsel, the court DENIES Dynetix's motion to dismiss and motion for summary judgment.

I. BACKGROUND

Dynetix and Synopsys are both electronic design automation ("EDA") companies, involved in creating software tools to design and test integrated circuits.[1] On December 5, 2011, Dynetix filed suit against Synopsys.[2] Synopsys filed a response and counterclaim, denying infringement of Dynetix's patent and claiming that Dynetix's various products infringed on two of Synopsys's patents.[3] In particular, Synopsys counterclaims that Dynetix's V2Sim and RaceCheck products infringe two of Synopsys's patents, U.S. Patent No. 5,706,473 ("the '473 Patent") and U.S. Patent No. 5,784,593 ("the '593 Patent").[4]

A. Synopsys' Patents in Suit

The '473 Patent, entitled "Computer Model of a Finite State Machine Having Inputs, Outputs, Delayed Inputs, and Delayed Outputs," describes a computer system having a computer model that can be manipulated "for the purposes of simulation, synthesis, and optimization."[5] On January 9, 2013, the court held a claim construction hearing and defined the disputed term "finite state machine" ("FSM") as "a sequential circuit whose finite number of output values at a given instant depends on either the sequence of previous inputs, current inputs, or both."[6]

The '593 Patent, entitled "Simulator Including Process Levelization," describes a method of using a circuit design simulator that takes a circuit specification written in Hardware Description

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[1] See Docket No. 1 ¶ 8; Docket No. 64 ¶ 3.

[2] See Docket No. 1.

[3] See Docket No. 9.

[4] See Docket No. 58 ¶¶ 17, 23.

[5] '473 Patent.

[6] See Docket No. 254 at 129.

Language ("HDL") and simulates how that circuit would behave with a given set of inputs.[7] HDL is a textual language used to specify the layout of circuit design.[8] Process levelization "attempts to find the ordering of the evaluations of the statements in the processes," or in other words, an appropriate order of process execution.[9]

B. The Accused Products

The V2Sim product is an HDL logic simulator. The simulator takes a circuit design encoded in HDL and simulates its logic and behavior with a given a set of inputs.[10]

The RaceCheck product is a verification tool that checks for "hard-to-detect race logic."[11] Race logic is "any logic construct that behaves differently when executed in [a] different order[]"[12] which if left uncorrected in a circuit could result in unpredictable results in field operations.[13] The RaceCheck product consists of a static race logic checker and a dynamic race logic checker, which can be used separately or simultaneously.[14] RaceCheck can be used in conjunction with V2Sim as a comprehensive verification solution that detects race logic conditions in a circuit, corrects those conditions, and then tests the circuit.[15]

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[7] '593 Patent.

[8] See Docket No. 114, Ex. H.

[9] See id. at 21.

[10] Docket No. 173 ¶ 7.

[11] See Docket No. 171 at 1.

[12] Id.

[13] See Dynetix's U.S. Patent No. 7,334,203 ("the '203 Patent"), entitled "RaceCheck: a race logic analyzer program for digital integrated circuits," which according to Dynetix's website claims the RaceCheck product. See Docket No. 114, Ex. G.

[14] See id.

[15] Id.

II. LEGAL STANDARD

Summary judgment is appropriate only if there is "no genuine dispute as to any material fact and the movant is entitled to judgment as a matter of law."[16] "Since the ultimate burden of proving infringement rests with the patentee, an accused infringer seeking summary judgment of noninfringement may meet its initial responsibility either by providing evidence that would preclude a finding of infringement, or by showing that the evidence on file fails to establish a material issue of fact essential to the patentee's case."[17] If met by the movant, the burden of production then shifts to the non-moving party, who must then provide specific facts showing a genuine issue of material fact.[18] The ultimate burden of persuasion, however, remains on the moving party.[19] In reviewing the record, the court must construe the evidence and the inferences to be drawn from the underlying evidence in the light most favorable to the non-moving party.[20]

Under Rule 56(d), if the nonmovant cannot, for specified reasons, present facts essential to justify its opposition to the motion, "the court may (1) defer considering the motion or deny it; (2) allow time to obtain affidavits or declarations or to take discovery; or (3) issue any other appropriate order."[21] This requires the nonmovant to show "(1) the specific facts that they hope to elicit from further discovery, (2) that the facts sought exist, and (3) that these sought-after facts are

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[16] Fed. R. Civ. P. 56(a).

[17] Novartis Corp. v. Ben Venue Laboratories, Inc., 271 F.3d 1043, 1046 (Fed. Cir. 2001).

[18] See Celotex Corp. v. Catrett, 477 U.S. 317, 330 (1986).

[19] Id.

[20] See Anderson, 477 U.S. at 248; Matsushita Elec. Indus. Co., Ltd. v. Zenith Radio Corp., 475 U.S. 574, 587 (1986).

[21] See Fed. R. Civ. P. 56(d).

"essential" to resist the summary judgment motion."[22] The nonmovant must also demonstrate that he diligently pursued previous discovery opportunities.[23]

To infringe a claim, each claim limitation must be present in the accused product, literally or equivalently.[24] Patent infringement is a two-step process: first, the court must construe the asserted claims; then, the court must compare the accused products with the construed claims and determine whether the products contain each limitation of the claims, either literally or equivalently.[25] A product literally infringes if it contains each element and limitation of the patent claim as construed.[26] A product may also infringe under the doctrine of equivalents, which applies if the element in the accused device performs substantially the same function, in substantially the same way, to obtain substantially the same result as the element claimed in the patent.[27]

III. DISCUSSION

A. Dynetix's 12(b)(6) Motion to Dismiss

The court first addresses the timeliness and the validity of Dynetix filing its motion to dismiss after it filed an answer to Synopsys' counterclaim. A motion to dismiss must be made before pleading if a responsive pleading is allowed. As such, "[p]ost-answer motions to dismiss are technically prohibited pursuant to Ninth Circuit authority."[28]

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[22] Family Home and Fin. Ctr., Inc. v. Fed. Home Loand Mortg. Corp., 525 F.3d 822, 827 (9th Cir. 2008).

[23] See Bank of Am., NT & SA v. PENGWIN, 175 F.3d 1109, 1118 (9th Cir. 1999).

[24] See Dawn Equip. Co. v. Kentucky Farms, Inc., 140 F.3d 1009, 1014 (Fed. Cir. 1998).

[25] See Freedman Seating Co. v. American Seating Co., 420 F.3d 1350, 1356-57 (Fed. Cir. 2005).

[26] See id. at 1357.

[27] See Abbott Laboratories v. Sandoz, Inc., 566 F.3d 1282, 1296-97 (Fed. Cir. 2009).

[28] Augustine v. U.S., 704 F.2d 1074, 1075 n. 3 (9th Cir.1983).

Nevertheless, "despite this seemingly unambiguous mandatory language, courts are split on allowing post-answer motions to dismiss, and no bright-line rule against allowing such a motion exists in the Ninth Circuit."[29] Indeed, district courts in the Ninth Circuit have entertained "post-answer motions to dismiss despite the mandatory language in Rule 12(b)."[30] "With respect to post-answer Rule 12(b) motions that raise nonwaivable defenses, [however,] the solution is not necessarily to deny the motion, but rather, to treat it as a different motion that would be permissible."[31] This appears to be the case here.

"Accordingly, and under Ninth Circuit precedent, the court will construe defendant's 12(b)(6) motion as a 12(c) motion for judgment on the pleadings to the extent the motion deals with plaintiffs' ability to state a [patent infringement] claim."[32] Under a Rule 12(c) motion, "judgment on the pleadings is properly granted when, accepting all factual allegations in the complaint as true, there is no issue of material fact in dispute, and the moving party is entitled to judgment as a matter of law."[33] The court's assessment of a Rule 12(c) challenge is substantially similar to that of a Rule 12(b)(6) challenge because, under both rules, a court must determine whether the complaint "contains sufficient factual matter, accepted as true, to state a claim to relief that is plausible on its face."[34]

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[29] Yocum v. Rockwell Med. Technologies, Inc., Case No. 12-CV-568-MMA(MDD), 2012 WL 2502701, at *2 (S.D. Cal. 2012) (citing Moreno–Garcia v. Yakima Police Dep't, 2010 U.S. Dist. LEXIS 114656, *3-4 (E.D. Wash. Oct. 27, 2010) (citing cases)).

[30] Vineyard v. Soto, 2011 U.S. Dist. LEXIS 129274, *9–*10 (D. Or. Nov. 7, 2011).

[31] Schlachte v. U.S., Case No. 07-6446 PJH, 2008 WL 3977901, at *4 (N.D. Cal. 2008).

[32] Id.

[33] Chavez v. U.S., 683 F.3d 1102, 1108 (9th Cir. 2012).

[34] Id (citing Ashcroft v. Iqbal, 556 U.S. 662, 678 (2009)).

Turning to the merits of Dynetix's motion, Dynetix argues that Synopsys' counterclaim improperly assumes that Dynetix's products embody its '898 Patent,[35] even though the complaint never actually mentions this assumption, and improperly relies on the technical description of the patent to describe the allegedly infringing features of Dynetix's products.[36]

Dynetix misunderstands the standard for assessing the sufficiency of a complaint like Synopsys'. The Supreme Court has explained that the trial court is limited to determining whether the complaint "contains sufficient factual matter, accepted as true, to state a claim to relief that is plausible on its face."[37] Thus, the court is not permitted to assess whether supporting evidence is "speculative." Moreover, Synopsys' claim that Dynetix's products practice the '898 Patent is plausible on its face because Dynetix's original complaint made such an admission.[38] Accepting these assertions as true, there is no reason why Synopsys could not rely on this patent for purposes of pleading, before Synopsys had a chance to conduct discovery, for information on the features of the accused products.[39] Tellingly, Dynetix never actually denies its products practice the '898 Patent, but merely asserts that the products practice the claims of the '898 Patent, not the patent

[35] Dynetix asserts the '898 Patent against Synopsys in the original action filed on December 5, 2011.

[36] See Docket No. 58.

[37] Iqbal, 556 U.S. at 678.

[38] See, e.g., Docket No. 1 ¶ 12 ("Dynetix practices the inventions claimed in the '898 Patent by making and selling V2Sim and RaceCheck").

[39] Invitrogen Corp. v. Clontech Laboratories, Inc., 429 F.3d 1052, 1070 (Fed. Cir. 2005) ("Section 112 requires that the patent specification enable those skilled in the art to make and use the full scope of the claimed invention without undue experimentation in order to extract meaningful disclosure of the invention and, by this disclosure, advance the technical arts.").

itself. As the claims define the invention covered by the patent, this is a distinction without a difference.[40]

B. Dynetix's Motion for Summary Judgment on Non-Infringement

The court now addresses Dynetix's alternative motion for summary judgment of non-infringement.

1. The '473 Patent

Dynetix argues that it does not infringe Synopsys' asserted claims 7-12 from the '473 Patent, because Dynetix does not practice each of the limitations of claim 7, the only independent claim.[41] Claim 7 reads:

> A method of simulating a circuit on a computer system, said circuit including a computer model of a Finite State Machine (FSM), said computer system including a processor and a memory, said processor being coupled to said memory, said method comprising:
> […]
> accessing a first input value;
> accessing a first delayed input value;
> accessing a first delayed output value; and
> executing a simulation program on said processor causing said processor to access a first output value from said computer model using said first input value, said first delayed input value and said first delayed output value, said first output value corresponding to an output value of said circuit.[42]

Dynetix first argues that Synopsys cannot prove that the accused products simulate any circuits including FSMs. As noted above, at the time the motion was filed the court had not construed "FSM," but has since interpreted the term to mean "a sequential circuit whose finite number of output values at a given instant depend on either the sequence of previous inputs,

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[40] See Phillips v. AWH Corp., 415 F.3d 1303, 1312 (Fed. Cir. 2005) ("It is a bedrock principle of patent law that the claims of a patent define the invention").

[41] See Docket No. 87.

[42] '593 Patent, col. 15-16, ll. 60-67, 1-12.

current inputs, or both."[43] Synopsys responds by submitting the expert declaration of Dr. Martin G. Walker ("Walker"), who, after inspecting the source code and user manuals of the accused products, opines that the RaceCheck and V2Sim products often simulate several circuits containing FSMs.[44] Walker specifically notes portions of a design simulated by Dynetix, named "uart.vhd," which contains a transmitter circuit, "txmt.vhd," and a receiver circuit containing the RXCVER.V file.[45] According to Walker, both the transmitter and receiver circuits model FSMs, comprised of multiple flip-flops and registers.[46]

This evidence shows both that Dynetix itself may have infringed, and that it intentionally induced its customers to engage in infringing activities.[47] While Dynetix disputes that FSMs can include flip-flops,[48] nothing in the court's claim construction excludes the use of flip-flops in a FSM. Treating all inferences in favor of the non-moving party, a reasonable jury could find that FSMs may consist of flip-flops.

Dynetix next argues conclusorily that Dynetix's products do not access any input, delayed input, or delayed output value as required by claim 7. Synopsys in turn points to Walker's analysis

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[43] See Docket No. 254 at 129.

[44] See Docket No. 173 ¶ 17-19. It is unclear whether Synopsys' theory of infringement is whether the FSM may be comprised of a single flip-flop, or the configuration of a number of flip-flops. See, e.g., Docket No. 113 ("for example, one type of finite state machine is a "flip-flop"). As Synopsys appears to argue the latter in its supplemental reply, the court primarily evaluates this version of Synopsys' theory.

[45] Docket No. 192, Ex. B ¶¶ 5-9.

[46] See id.

[47] See Docket No. 232 (citing *Alloc, Inc. v. U.S. Int'l Trade Comm'n*, 342 F.3d 1361, 1374 (Fed. Cir. 2003)).

[48] Dynetix's reply states that "Dynetix's simulation tool does not contain any flip-flops." See Docket No. 120 at 6. But the supporting declaration does not say anything about the use of flip-flops. In fact, the declaration states elsewhere that Dynetix products do simulate flip-flops. See, e.g., Docket No. 232-1 ¶ 5, 10 ("just because Dynetix products can simulate finite state machines containing flip-flops…"). See also Docket No. 192, Ex. C at 129-130.

of V2Sim's source code, which identified specific portions where the V2Sim product accesses inputs, delayed inputs, outputs, and delayed outputs of various circuit design components.[49] Further, Walker also found parts of the RXCVER.v file to be simulated with inputs, elayed inputs, and delayed outputs as required by claim 8.[50] Synopsys also argues that the V2Sim and RaceCheck user's manual shows that the products access inputs, outputs, delayed inputs, and delayed outputs.[51] This creates a triable issue of fact that Dynetix's products satisfy the limitations of claim 7.

2. The '593 Patent

For the '593 Patent, Synopsys asserts claims 8-13. Dynetix claims that it does not infringe because Synopsys cannot establish infringement of claims 8 and 12, the two independent claims.

a. Claim 8

Claim 8 requires the following:

> A method of simulating a system on a computer, said method comprising the steps of:
> determining an end time of a first cycle;
> evaluating a stimulus process using said end time;
> evaluating a set of processes that include a combinational feedback loop, said set of processes that include a combinational feedback loop including a state change signal and a process in said combinational feedback loop;
> if said state change signal is activated, then evaluating a subset of processes of said set of processes including the process in said combinational feedback loop effected by said state change signal; and
> else if said state change signal is not activated, then determining a next end time of a second cycle.[52]

[49] See Docket No. 173 ¶ 20. See also id., Ex. A (expert's claim-by-claim analysis of how V2Sim while simulating RXCVER.V practices the steps of accessing a first input value, a first delayed input value, and a first delayed output value).

[50] See Docket No. 192, Ex. B ¶ 7, Ex. C.

[51] See Docket No. 172 at 22.

[52] '593 Patent, col. 19, ll. 35-50.

Dynetix interprets the limitations "determining an end time of a first cycle," "evaluating a stimulus process using said end time," and "determining a next end time of a second cycle" to limit claim 8 to embodiments that use cycle-based simulation. Dynetix claims that its products use event-driven simulation, not cycle-based, and so its products do not infringe claim 8. As Synopsys points out, however, the court is not required to accept Dynetix's conclusory allegation that only cycle-based simulation can satisfy claim 8, and instead focuses on the actual language of claim 8. Synopsys also contends that even the event-driven features of the accused products practice all three steps challenged by Dynetix. Walker identifies points in the products' User's Manual showing that the products identify the end time of the simulation, in addition to at other points of the simulation.[53] This creates a triable issue of fact that Dynetix's products exhibit the limitations challenged above.

Moreover, Synopsys also identifies code implementing cycle-based simulation features in the RaceCheck product. Walker notes that sections of code exhibiting cycle-based features appear to have been commented out, but it is unclear when these features were taken out.[54] Dynetix does not contest that the code was once a part of its product, but states that the feature "has been abandoned in all Dynetix's products."[55] Under Dynetix's own assertions, the implication is that Dynetix's product once contained cycle-based simulation features, which at a minimum creates a disputed issue of fact regarding infringement.

Dynetix also argues that its products do not evaluate "combinational feedback loops," which occurs "where an output signal is fed back into a combinational component of a system" and may cause problems when the design is simulated.[56] But as Synopsys points out, the RaceCheck

[53] See Docket No. 173 ¶ 25. See also Docket No. 172 at 21, 25.

[54] See Docket No. 173 ¶ 27.

[55] Docket No. 90 ¶ 13.

[56] '593 Patent, col. 2, ll. 42-44.

brochure touts RaceCheck's ability to "Detect[] a comprehensive set of… Combinational feedback loops."[57] Walker has also located code in RaceCheck demonstrating that the product evaluates a set of processes to determine if the set includes a combinational feedback loop.[58] Synopsys therefore has pointed to specific evidence establishing a genuine issue of material fact on whether the products exhibit this limitation.

b. Claim 12

Next, Dynetix contends that Synopsys is unable to prove the accused products practice the limitations of claim 12, which reads:

> A computer implemented method of generating an ordered sequences of processes from a plurality of processes, said plurality of processes including a first process and a second process, said plurality of processes representing a hardware description language specification of a system, said method comprising:
> […]
> ordering said plurality of processes so that processes that drive said nets are evaluated prior to processes that use said nets; and
> […]
> wherein if a process is part of a combinational feedback loop, then attempting to split said process so as to break said combinational feedback loop.[59]

While claim 12, like claim 8, also involves detecting combinational feedback loops within the set of evaluated processes, claim 12 further requires that upon finding the combinational feedback loop, the invention also "attempt[] to split said process so as to break said combinational feedback loop." Dynetix argues that Synopsys cannot prove that Dynetix's customers practice this element of splitting and breaking the combinational feedback loop. As Dynetix points out, Synopsys must show that customers actually practiced this element.[60] Synopsys' theory of

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[57] Docket No. 171 at 2.

[58] See Docket No. 173 ¶ 28.

[59] '593 Patent, col. 20, ll. 1-23.

[60] See ACCO Brands, Inc. v. ABA Locks Mfr. Co., 501 F.3d 1307, 1313 (Fed. Cir. 2007) ("In order to prove direct infringement, a patentee must either point to specific instances of direct infringement or show that the accused device necessarily infringes the patent in suit.").

infringement of this limitation is that RaceCheck allows customers to identify race logic conditions, which Synopsys states includes combinational feedback loops, and fix those conditions, which constitutes "breaking" the combinational feedback loop. As evidence that RaceCheck aids customers in doing so, Synopsys submits Terence Chan's ("Chan") deposition stating that RaceCheck identifies race logic problems to enable the user to fix them.[61] A reasonable trier could take Chan's testimony to indicate further that users proceed to do just that. The identify-and-fix function of the RaceCheck product is further demonstrated by the '203 Patent, which according to Dynetix's website claims the RaceCheck product.[62] In describing the technology, the '203 Patent notes that "the combinational feedback loops, if present, will cause the event-driven simulation to run forever, thus they can only be detected by the static race logic checker program. Those combinational feedback loops must be corrected before the dynamic race logic checker program can analyze the CUT [circuit-under-test]."[63] This creates a triable issue of fact that Dynetix and its customers infringe because Dynetix enables its customers to use RaceCheck to detect and correct combinational feedback loops.

Dynetix also argues that its products do not "order said plurality of processes" in the way described by claim 12. In response, Synopsys points to Chan's testimony that V2Sim and RaceCheck "evaluate[] processes according to range order only in the circuit initialization phase," or "rank the process blo[ck]s in the circuit," "but only for the purpose of the circuit presimulation

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[61] Docket No. 192, Ex. C at 62.

[62] See Docket No. 114, Ex. G. ("Dynamic race logic checker uses advanced multithreaded… HDL simulation technologies to detect 'real-life' race events").

[63] '203 Patent, col. 15, ll. 10-16.

in the initialization of the circuit."[64] A reasonable jury could equate Dynetix's admission that the products rank the processes according to range order as satisfying the "ordering" limitation.

Because the court finds triable issues of fact regarding Dynetix's infringement of both patents, the court need not reach Synopsys' Rule 56(d) request.

IV. CONCLUSION

Dynetix's motion to dismiss and, in the alternative, for summary judgment of non-infringement is DENIED.

IT IS SO ORDERED.

Dated: May 21, 2013

PAUL S. GREWAL
United States Magistrate Judge

[64] Docket No. 192, Ex. C at 201-02.