1

2

3

4

5

6

7

8

UNITED STATES DISTRICT COURT

9

NORTHERN DISTRICT OF CALIFORNIA

10

SAN JOSE DIVISION

	) Case No.: C 11-5973 PSG
11 DYNETIX DESIGN SOLUTIONS INC., a	)
California corporation,	) **ORDER RE: FINAL CLAIM**
12	) **CONSTRUCTION RULINGS**
	)
13 Plaintiff/Counter-defendant,	)
	)
14 v.	)
	)
15 SYNOPSYS INC., a Delaware corporation,	)
	)
16 Defendants/Counter-claimant.	)
	)
17	)

18

19   In this patent infringement suit, Plaintiff and counter-defendant Dynetix Design Solutions,

20 Inc. ("Dynetix") alleges that Defendant and counter-claimant Synopsys, Inc. ("Synopsys")

21 infringes U.S. Patent No. 6,466,898 ("the '898 patent"). Synopsys counterclaims that Dynetix

22 infringes U.S. Patent No. 5,706,473 ("the '473 patent") and U.S. Patent No. 5,784,593 ("the '593

23 patent"). On October 10, 2012 and January 9, 2013, the court construed terms in the '898 patent

24 and the '473 patent, respectively. The court's final constructions are as follows:

25

CLAIM TERM	**CONSTRUCTION**
"Multithreaded simulation" '898 patent	A "thread" is a process flow in a program that runs on a central processing unit ("CPU"). "Multithreaded simulation" means

26

27

28

1

Case No.: 11-5973 PSG
ORDER

	a simulation of circuit functionalities by executing multiple process flows concurrently on multiple CPUs.
"To achieve linear to super-linear scalable performance speedup/simulation" '898 patent	The terms "linear" and "super-linear" describe the speedup that a parallel simulation will achieve when performing hardware containing one or more processing units. A simulation is "linear" if the speedup that is achieved is equal to the number of available processing units. For example, a simulation that runs two times as fast on hardware containing two processing units is "linear." Similarly, if the simulation runs four times as fast on four processing units, it is again "linear." A simulation that has a speedup greater than the number of processing units is "super-linear." For example, if a process executed on two processing units runes three times as fast as the same simulation on one processing unit, it is "super-linear." "Scalable performance" means there is a consistent increase in performance for each added processing unit.
"Achieving super-linear scalable" '898 patent	This term in the preamble limits claims 36 and 45.
"Event queue" '898 patent	An "event" in simulation is a task to be processed at a specified time resulting in a change of state. "Event queue" is a sequence of events held in temporary storage waiting to be processed.
"Common design database" '898 patent	A "design database" is a database in which the simulation later compiles design files and stimulus files supplied by the user.

United States District Court

For the Northern District of California

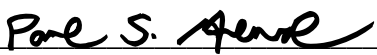|	The phrase "common design database" means a design database which contains various compiled design modules that may be coded in different design languages that are processed by the same multithreaded simulation engine.
"To create a master thread and a plurality of slave threads" '898 patent	Creating one thread for each processor where the master thread is executed on one processor and each of the slave threads is executed on a separate remaining processor.
"Pre-examining each user-specified HDL source file" '898 patent	The simulator examining the content of each source file to automatically detect its coded file language before compiling the source file.
"Specify remote hosts" '898 patent	The user identifying remote computers by name.
"Graphical user interface" or "GUI" '898 patent	A computer user interface that allows interaction using graphical objects such as icons, images, and windows as opposed to merely a command line interface.
"By at the beginning" '898 patent	The court finds this term may be construed by correcting the typographical error. The phrase shall be corrected to "at the beginning."
"Means to provide a graphical user interface program ('GUI') on the user's local hosts" '898 patent	No ruling or construction in light of the court's concern that this claim may be indefinite.
"Finite state machine" '473 patent	A sequential circuit whose finite number of output values at a given instant depends on either the sequence of previous inputs, the current input, or both.

The parties should rest assured that the court arrived at these constructions with a full

appreciation of not only the relevant intrinsic and extrinsic evidence, but also the Federal Circuit's

3

Case No.: 11-5973 PSG
ORDER

teachings in Phillips v. AWH Corp.[1] and its progeny. As the parties undoubtedly appreciate,

certain of these terms relate to claims no longer at issue in light of the court's various summary

judgment rulings. So that the parties may pursue whatever recourse they believe is necessary, a

complete opinion will issue before entry of any judgment.

IT IS SO ORDERED.

Dated: August 21, 2013

_____

PAUL S. GREWAL
United States Magistrate Judge

---

[1] 415 F.3d 1303, 1312-15 (Fed. Cir. 2005).

4

Case No.: 11-5973 PSG
ORDER