UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

SYNTEST TECHNOLOGIES, INC., Plaintiff, v. CISCO SYSTEMS, INC., Defendant.	Case No.: 5:12-cv-05965-PSG **CLAIMS CONSTRUCTION ORDER** **(Re: Docket No. 35)**

In this patent infringement suit, Plaintiff Syntest Technologies, Inc. asserts that Defendant Cisco Systems, Inc. infringed one or more claims within three of its patents.[1] Consistent with Pat. L.R. 4-3(c), the parties seek construction of terms and phrases of the patents-in-suit. A lengthy – and helpful – tutorial and claims construction hearing was held last Friday, October 18, 2013. As the court previewed at the conclusion of the hearing, the court will proceed to issue its constructions now without setting forth its reasoning and analysis.

[1] See Docket No. 64 (First Amended Complaint) (asserting infringement of U.S. Patent Nos. 7,007,213 ("the '213 patent"), 7,434,126 ("the '126 patent"), and 7,779,323 ("the '323 patent")).

CLAIM TERM/DISPUTE	CONSTRUCTION
Whether the claim preambles are limiting with respect to the ’213 patent (claims 1 and 29), the ’126 patent (claim 1), and the ’323 patent (claim 1).	Only the preamble to claim 1 of the ’126 patent is limiting.
“providing ordered capture clocks” The ’213 patent (claims 1, 29), the ’126 patent (claim 1), and the ’323 patent (claim 1)	triggering a capture clock pulse in at least one clock domain in response to a capture clock pulse in another clock domain
“applying an ordered sequence of capture clock pulses to all said scan cells within said N clock domains in said normal mode during a capture operation, the ordered sequence of capture clock pulses comprising at least two capture clock pulses from two or more selected capture clocks, for controlling two or more clock domains, in a sequential order” The ’213 patent (claims 1, 29)	applying one or more capture clock pulses (without including shift clock pulses in the capture window) to the scan cells within a clock domain in normal mode, followed by applying one or more capture clock pulses (without including shift clock pulses in the capture window) to the scan cells in the next sequentially ordered clock domain in normal mode by triggering a capture clock pulse in the latter clock domain in response to a capture clock pulse in the former clock domain
“applying an ordered sequence of capture clocks to all said scan cells within said N clock domains, the ordered sequence of capture clocks comprising at least a plurality of capture clock pulses from two or more selected capture clocks placed in a sequential order such that all clock domains are never triggered simultaneously during a capture operation” The ’126 patent (claim 5) and the ’323 patent (claim 1)	applying one or more capture clock pulses (without including shift clock pulses in the capture window) to the scan cells within a clock domain in normal mode, followed by applying one or more capture clock pulses (without including shift clock pulses in the capture window) to the scan cells in the next sequentially ordered clock domain in normal mode by triggering a capture clock pulse in the latter clock domain in response to a capture clock pulse in the former clock domain such that all clock domains are never triggered simultaneously during a capture operation
“when detecting or locating selected delay faults within a clock domain said selected capture clock controlling the clock domain contains at least two consecutive said capture clock pulses to launch the transition and capture the output response” The ’213 patent (claims 1, 29)	testing of delay faults is performed by applying two or more consecutive capture clock pulses to the clock domain with the first pulse initiating (launching) the transition at a targeted terminal and each subsequent pulse capturing the response at a scan cell
The ordering of the claim steps 1(a)-1(e). The ’126 patent (claim 1) The meaning of checking whether said design database contains any multiple capture violations The ’126 patent (claim 1)	The claimed steps 1(a), 1(b), and 1(c) must precede 1(d) and 1(e). verifying whether the design complies with scan and BIST-specific design rules

"each shift clock pulse comprising a clock pulse applied in scan mode" The '213 patent (claims 1, 29) and the '126 patent (claim 1)	each shift clock pulse comprising a pulse of the capture clock at a frequency that need not be the same as the normal operating frequency of the domain's system clock
"each capture clock pulse comprising a clock pulse applied in normal mode" The '213 patent (claims 1, 29) and the '126 patent (claim 1)	each capture clock pulse comprising a pulse of the capture clock at a frequency that need not be the same as the clock when generating shift clock pulses
What structures are disclosed by the specification with respect to "means for generating and shifting-in N test stimuli to all said scan cells within said N clock domains in said integrated circuit or circuit assembly during a shift-in operation" The '323 patent (claim 1)	**Function:** Generating N test stimuli. **Structure:** If self-test – the PRPG with or without a phase shifter. If scan-test – the ATPG. **Function:** Shifting-in N test stimuli. **Structure:** If self-test – the DFT system. If scan-test – the ATE.

The parties should rest assured that the court arrived at these constructions with a full appreciation of not only the relevant intrinsic and extrinsic evidence, but also the Federal Circuit's teaching in *Phillips v. AWH Corp.*,[2] and its progeny. So that the parties may pursue whatever recourse they believe is necessary, a complete opinion that sets forth the court's reasoning and analysis will issue before entry of any judgment.

IT IS SO ORDERED.

Dated: October 22, 2013

PAUL S. GREWAL
United States Magistrate Judge

[2] 415 F.3d 1303, 1312-15 (Fed. Cir. 2005).