UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

SYNTEST TECHNOLOGIES, INC., Plaintiff, v. CISCO SYSTEMS, INC., Defendant.	Case No. 5:12-cv-05965-PSG **CLAIMS CONSTRUCTION ORDER** **(Re: Docket No. 74)**

In this patent infringement suit, Plaintiff SynTest Technologies, Inc. alleges that Defendant Cisco Systems, Inc. infringes U.S. Patent Nos. 7,007,213, 7,434,126 and 7,779,323. The parties submitted ten claim construction disputes from those asserted patents for resolution by the court. The court issued a summary construction order a few days after the hearing and explained that a more complete order would follow providing the court's reasoning.[1] The court now provides that reasoning.

[1] *See* Docket No. 74.

I. BACKGROUND

A. The Parties

SynTest and Cisco are California corporations with principal places of business in this district.[2] SynTest creates and licenses tools for the design of application specific integrated circuits ("ASICs"). SynTest is the assignee of each of the asserted patents. Cisco is a former SynTest customer. SynTest alleges Cisco developed and uses ASICs practicing the patents-in-suit without a valid license.[3]

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[2] *See* Docket No. 64 at ¶¶ 4-5. The background material describing the technology at issue in this section is drawn from the parties' opening claim construction briefs. *See* Docket No. 44 at 1-6 and Docket No. 46 at 1-9.

[3] After the court issued its constructions, the parties stipulated that under those constructions Cisco's accused instrumentalities do not practice certain limitations and thus does not infringe the asserted patents. *See* Docket No. 78 at ¶¶ 7-14.

NONINFRINGEMENT BASIS NO. 1:

7. The Court construed the claim limitation "providing ordered capture clocks" in Claim 1 of the '126 Patent as "triggering a capture clock pulse in at least one clock domain in response to a capture clock pulse in another clock domain";

8. The Court construed the claim limitation "applying an ordered sequence of capture clock pulses to all said scan cells within said N clock domains in said normal mode during a capture operation, the ordered sequence of capture clock pulses comprising at least two capture clock pulses from two or more selected capture clocks, for controlling two or more clock domains, in a sequential order" in Claims 1 and 29 of the '213 Patent as "applying one or more capture clock pulses (without including shift clock pulses in the capture window) to the scan cells within a clock domain in normal mode, followed by applying one or more capture clock pulses (without including shift clock pulses in the capture window) to the scan cells in the next sequentially ordered clock domain in normal mode by triggering a capture clock pulse in the latter clock domain in response to a capture clock pulse in the former clock domain";

9. The Court construed the claim limitation "applying an ordered sequence of capture clocks to all said scan cells within said N clock domains, the ordered sequence of capture clocks comprising at least a plurality of capture clock pulses from two or more selected capture clocks placed in a sequential order such that all clock domains are never triggered simultaneously during a capture operation" in Claim 1 of the '323 Patent as "applying one or more capture clock pulses (without including shift clock pulses in the capture window) to the scan cells within a clock domain in normal mode, followed by applying one or more capture clock pulses (without including shift clock pulses in the capture window) to the scan cells in the next sequentially ordered clock domain in normal mode by triggering a capture clock pulse in the latter clock domain in response to a capture clock pulse in the former clock domain such that all clock domains are never triggered simultaneously during a capture operation";

10. Cisco asserts that the Cisco Accused Instrumentalities1 do not practice the limitations recited above in Paragraphs 7-9 as construed by the Court at least because they trigger a domain's capture clock pulses based on the number of cycles that have occurred in a

B. The Technology

1. Fault Testing the Logic of an Integrated Circuit

Before an ASIC can be manufactured, its logic must first be tested to see if it works as intended. Testing tools can be built into an AISC that work either with external automatic test equipment or alone. Testing tools built into the circuit itself are collectively known as a Built-In Self-Test.

ASICs commonly contain millions of "flip-flops" that act as memory cells. A flip-flop stores states of logic as a one or zero. The state of a flip-flop is controlled by electronic pulses that run through the ASIC. The frequency of these pulses is in turn controlled by a clock. The area of an ASIC controlled by a clock is called a clock domain. A single ASIC can have dozens of such domains – each controlled by separate clocks operating at different frequencies.

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common reference clock, rather than triggering a capture clock pulse in at least one clock domain in response to a capture clock pulse in another clock domain, and, therefore, a final judgment of noninfringement should be entered in Cisco's favor.

11. Cisco has indicated that it intends to seek summary judgment in this action on at least the grounds described in the preceding paragraph, and the parties agree that the Court's Claim Construction Order would warrant summary judgment of noninfringement at this time on that basis and, therefore, a final judgment of noninfringement should be entered in Cisco's favor;

NONINFRINGEMENT BASIS NO. 2:

12. The Court construed each of the phrases "each shift clock pulse comprising a clock pulse applied in scan mode" and "each capture clock pulse comprising a clock pulse in normal mode," in Claim 1 of the '126 Patent and Claims 1 and 29 of the '213 Patent as referring to "a pulse of the capture clock";

13. Cisco asserts that the clock that comprises capture clock pulses in the Cisco Accused Instrumentalities does not also comprise shift clock pulses and, therefore the Cisco Accused Instrumentalities lack a shift clock pulse that comprises a pulse of the capture clock and do not practice this limitation as construed by the Court;

14. Cisco has indicated that it intends to seek summary judgment in this action on at least the grounds described in the preceding paragraph, and the parties agree that the Court's Claim Construction Order would warrant summary judgment of noninfringement at this time on that basis and, therefore, a judgment of noninfringement should be entered in Cisco's favor on all claims of infringement of the '213 and the '126 Patent . . .

See also Docket No. 74.

2. Design For Test Techniques

Logic faults include "stuck-at" faults and "delay" faults. With a stuck-at fault, the state of the flip-flop is stuck at one or zero. A delay fault is one that causes the ASIC to operate slower than expected. The three patents in this case share a common specification and are directed to a specific design for test ("DFT") technique for detecting whether the logic in an ASIC suffers from any other type of fault. The asserted patents describe DFT techniques "that can facilitate detection or location of physical defects that can manifest themselves as logic faults within an integrated circuit or circuit assembly."[4]

The particular scan design at issue in the asserted patents involves loading (or "shifting") test patterns into storage elements of an ASIC using clock pulses known as "shift clock pulses."[5] When an ASIC receives the shift clock pulses and is operating in what is called "scan mode," the ASIC reacts by shifting the test stimuli into the ASIC's storage elements. Next, when the ASIC is operating in what is called "normal mode" and receives "capture clock pulses,"[6] those pulses cause the ASIC to operate on the loaded test stimuli as it would when operating in its normal functional mode.[7] Finally, when the ASIC is returned to scan mode and it receives additional shift clock

[4] Docket No. 45-4, Ex. D at 5.

[5] Docket No. 45-1, Ex. A at Fig. 10.

[6] ASICs with multiple system clocks can experience "clock skew" among the system clocks, which can create difficulties in detecting faults. Docket No. 45-1, Ex. A at 1:39-47. One prior art approach to solving that problem involved taking "over control of all system clocks" and reconfiguring "them as capture clocks." *Id.* at 1:49-50. The parties agree that a "capture clock" is a "reconfigured system clock." *See* Docket No. 35, Ex. A, at 1; *see also* Docket No. 45-1, Ex. A at 9:20 ("The reconfigured system clocks are called capture clocks."). The particular type of "capture clock" claimed in the patents-in-suit is a single reconfigured system clock that provides both shift clock pulses and capture clock pulses – depending on the "mode" in which the circuit operates.

[7] In the "daisy-chain" technique, one variant of this general technique, the capture clock pulse of one domain is triggered by the occurrence of a capture clock pulse of a preceding domain. *See id.* at 4:66-5:10. The "token ring" technique, another variant, is similar, except that the second domain's capture clock pulse is triggered based by occurrence of a particular signal level in the preceding domain's capture clock pulses. *See id.* at 5:11-16. For both variants, the first capture clock pulse of one of the clock domains is triggered by activity of the capture clock pulse of the preceding clock domain.

pulses, the shift clock pulses are applied to collect or "shift out" of the storage elements the results of the circuit's operation, so that they can be analyzed.

3. Detecting Faults Within and Crossing Clock Domains

An "integrated circuit or circuit assembly, in general, contains two or more system clocks, each controlling one module, or logic block, called [a] clock domain."[8] In other words, a "clock domain" is a module or logic block of an ASIC that is controlled by a single system clock. The system clock is the clock that drives the normal functional operation of the clock domain. ASICs can experience logic faults that occur completely "within" a given clock domain, as well as faults that "cross" multiple clock domains.[9] One aspect of the invention claimed in the asserted patents is the ability to detect both faults within and faults crossing any two clock domains.[10]

C. The Independent Asserted Claims

1. Claim 1 of the '213 Patent

Independent claim 1 of the '213 patent provides:

> 1. A method for providing ordered capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains in an integrated circuit or circuit assembly during self-test, where N>I, each clock domain having one or more capture clocks and one or more scan cells, each capture clock comprising a selected number of shift clock pulses and a selected number of capture clock pulses, each shift clock pulse comprising a clock pulse applied in scan mode, each capture clock pulse comprising a clock pulse applied in normal mode; said method comprising the steps of:
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> (a) generating and loading N pseudorandum stimuli to all said scan cells within said N clock domains in said integrated circuit or circuit assembly, by applying said shift clock pulses to all said scan cells in said scan mode for loading or shifting-in said N pseudorandom stimuli to all said scan cells, during a shift operation;
>
> (b) applying an ordered sequence of capture clock pulses to all said scan cells within said N clock domains in said normal mode during a capture operation, the ordered sequence of capture clock pulses comprising at least two capture clock pulses from two or more selected capture clocks, for controlling two or more clock domains, in a sequential order, wherein each said selected capture clock must contain at least one said capture clock pulse, and when detecting or locating selected delay faults within a clock domain, said selected

[8] *Id.* at 1:31-33.

[9] *Id.* at 1:39-46.

[10] *See, e.g., id.* at 1:16-18 ("[T]he present invention relates to the detection or location of logic faults within each clock domain and logic faults crossing any two clock domains, during self-test or scan-test, in an integrated circuit or circuit assembly.").

capture clock controlling the clock domain contains at least two consecutive said capture clock pulses to launch the transition and capture the output response; and

(c) compacting N output responses of all said scan cells to signatures, by applying said shift clock pulses to all said scan cells in said scan mode for compacting or shifting-out said N output responses to form said signatures, during a compact operation.[11]

2. Claim 1 of the '126 Patent

Independent claim 1 of the '126 patent provides:

1. A computer-aided design (CAD) method for providing ordered capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains in an integrated circuit or circuit assembly in scan-test and selftest mode, where N>1, each clock domain having one capture clock and a plurality of scan cells, each capture clock comprising a selected number of shift clock pulses and a selected number of capture clock pulses, each shift clock pulse comprising a clock pulse applied in scan mode, each capture clock pulse comprising a clock pulse applied in normal mode, said CAD method comprising the computer-implemented steps of:

(a) compiling the HDL code or netlist that represents said integrated circuit or circuit assembly in physical form into a design database;

(b) performing test rule check for checking whether said design database contains any multiple-capture rule violations in said scan-test or said self-test mode;

(c) performing test rule repair until all said multiple-capture rule violations have been fixed;

(d) performing multiple-capture test synthesis for generating a testable HDL code or netlist; and

(e) generating HDL test benches and automatic test equipment (ATE) test programs for verifying the correctness of said testable HDL netlist in said scan-test or said self-test mode.[12]

3. Claim 1 of the '323 Patent

Independent claim 1 of the '323 patent provides:

1. An apparatus for providing ordered capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains in an integrated circuit or circuit assembly in scan-test or self-test mode, where N>1, each clock domain having one capture clock and a plurality of scan cells, each capture clock comprising a plurality of capture clock pulses; said apparatus comprising:

(a) means for generating and shifting-in N test stimuli to all said scan cells within said N clock domains in said integrated circuit or circuit assembly during a shift-in operation;

(b) means for applying an ordered sequence of capture clocks to all said scan cells within said N clock domains, the ordered sequence of capture clocks comprising at least a plurality of capture clock pulses from two or more selected capture clocks placed in a sequential order such that all clock domains are never triggered simultaneously during a capture operation; and

(c) means for analyzing output responses of all said scan cells to locate any faults therein.[13]

[11] *See* Docket No. 45-1 at 23:10-46.

[12] *See* Docket No. 45-2 at 22:39-64.

II. LEGAL STANDARDS

Almost nine years after the Federal Circuit's seminal *Phillips* decision,[14] the canons of claim construction are now well-known – if not perfectly understood – by parties and courts alike. "To construe a claim term, the trial court must determine the meaning of any disputed words from the perspective of one of ordinary skill in the pertinent art at the time of filing."[15] This requires a careful review of the intrinsic record, comprised of the claim terms, written description, and prosecution history of the patent.[16] While claim terms "are generally given their ordinary and customary meaning," the claims themselves and the context in which the terms appear "provide substantial guidance as to the meaning of particular claim terms." Indeed, a patent's specification "is always highly relevant to the claim construction analysis."[17] Claims "must be read in view of the specification, of which they are part."[18] Although the patent's prosecution history "lacks the clarity of the specification and thus is less useful for claim construction purposes," it "can often inform the meaning of the claim language by demonstrating how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be."[19] The court also has the discretion to consider extrinsic evidence, including dictionaries, learned treatises, and testimony from experts and

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[13] *See* Docket No. 45-3 at 22:39-58.

[14] *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005).

[15] *Chamberlain Group, Inc. v. Lear Corp.*, 516 F.3d 1331, 1335 (Fed. Cir. 2008).

[16] *See id.* ("To construe a claim term, the trial court must determine the meaning of any disputed words from the perspective of one of ordinary skill in the pertinent art at the time of filing. Intrinsic evidence, that is the claims, written description, and the prosecution history of the patent, is a more reliable guide to the meaning of a claim term than are extrinsic sources like technical dictionaries, treatises, and expert testimony.") (citing *Phillips*, 415 F.3d at 1312).

[17] *Phillips*, 415 F.3d at 1312-15.

[18] *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995); *see also Ultimax Cement Mfg. Corp v. CTS Cement Mfg. Corp.*, 587 F. 3d 1339, 1347 (Fed. Cir. 2009).

[19] *Phillips*, 415 F.3d at 1317 (internal quotations omitted).

inventors.[20] Such evidence, however, is "less significant than the intrinsic record in determining the legally operative meaning of claim language."[21]

III. DISCUSSION

A. Dispute #1: Whether the Preamble to Claim 1 of the '126 Patent is Limiting

CLAIM TERM/DISPUTE #1	
Whether the claim preambles of independent claims 1 and 29 of the '213 patent, claim 1 of the '126 patent and claim 1 of the '323 patent are limiting.	
SynTest's Preferred Construction	**Cisco's Preferred Construction**
Not a claim construction issue	The preambles are limiting
CONSTRUCTION/RESOLUTION	
Only the preamble to claim 1 of the '126 patent is limiting.	

The parties dispute whether the claim preambles are limiting with respect to the '213 patent (claims 1 and 29), the '126 patent (claim 1) and the '323 patent (claim 1).

Although SynTest believes the question does not constitute a claim construction issue, it argues in the alternative that not all of the preambles are limiting. Because language in the preambles is repeated in the claim terms or referenced elsewhere in the patent, many of the ideas in the preambles necessarily will be addressed in other portions of the construction and there is no reason for the court to construe them within the preamble. SynTest does recognize one exception: the preamble to claim 1 of the '126 patent. The reason is that limitations A through E of that claim merely describe performing tasks on a circuit and limitations from the preamble are necessary for these later limitations to have meaning.[22] In contrast, claims 1 and 29 of the '213 patent fully

[20] *See id.* ("Although we have emphasized the importance of intrinsic evidence in claim construction, we have also authorized district courts to rely on extrinsic evidence, which 'consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises.'") (quoting *Markman*, 52 F.3d at 980).

[21] *Id.* (citing *C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 862 (Fed. Cir. 2004)) (internal quotations and additional citations omitted).

[22] *See* Docket No. 45-2, Ex. B at 22:39-64.

describe the concept of testing within step B: the claim preamble is merely extolling the virtues of the patent and, according to SynTest, is not necessary to provide structure to the claim.[23] Similarly, the preamble from claim 1 of the '323 patent is not limiting, according to SynTest, because the purported limitation that N be greater than one is fully described in step B of claim 1.

Cisco disagrees, relying upon the Federal Circuit teaching that when "limitations in the body of the claim rely upon and derive antecedent basis from the preamble, then the preamble may act as a necessary component of the claimed invention."[24] According to Cisco, because all three preambles here supply antecedent bases for limitations that follow, all three claim preambles are limiting.

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[23] *See Deere & Co. v. Bush Hog, LLC*, 703 F.3d 1349, 1358 (Fed. Cir. 2012) (If "the body of the claim describes a structurally complete invention, a preamble is not limiting where it 'merely gives a name' to the invention, extols its features or benefits, or describes a use for the invention." (quoting *Catalina Marketing, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801, 809 (Fed. Cir. 2002))).

[24] *Eaton Corp. v. Rockwell Int'l Corp.*, 323 F.3d 1332, 1339 (Fed. Cir. 2003) ("The method steps of claim 14 thus require the manipulation of particular structures that are identified and described only by the preamble, during a particular sequence of events defined only" and therefore "the preamble of claim 14 limits the claimed invention."); *see also Electro Sci. Indus. v. Dynamic Details, Inc.*, 307 F.3d 1343, 1348 (Fed. Cir. 2002)

> To determine the meaning of "circuit boards," this court begins with the claim language. The preamble defines "circuit boards" as "at least first and second substantially identical circuit boards each having at least a first conductor layer, a dielectric layer, and a second conductor layer." References throughout the rest of the claim to "circuit boards" rely upon and derive antecedent basis from this preamble language. Therefore, this preamble definition limits the term "circuit boards" throughout the claim.

see also Rapoport v. Dement, 254 F.3d 1053, 1059 (Fed. Cir. 2001)

> First, we note that the disputed phrase "treatment of sleep apneas" is technically part of the preamble of the interference count, because it appears before the transition word "comprising." However, there is no dispute in this case that the phrase should be treated as a claim limitation. Moreover, without treating the phrase "treatment of sleep apneas" as a claim limitation, the phrase "to a patient in need of such treatment" would not have a proper antecedent basis.

see also Pitney Bowes, Inc. v. Hewlett-Packard Co., 182 F.3d 1298, 1306 (Fed. Cir. 1999);

> The preamble statement that the patent claims a method of or apparatus for "producing on a photoreceptor an image of generated shapes made up of spots" is not merely a statement describing the invention's intended field of use. Instead, that statement is intimately meshed with the ensuing language in the claim. For example, both independent claims conclude with the clause "whereby the appearance of smoothed edges are given to the generated shapes". Because this is the first appearance in the claim body of the term "generated shapes", the term can only be understood in the context of the preamble statement "producing on a photoreceptor an image of generated shapes made up of spots."

SynTest has the better of the argument, at least on the merits. The determination of whether preambles are limiting necessarily affects the meaning – and therefore the size and scope – of the asserted claims.[25] Absent guidance on whether the preambles limit the scope of asserted claims, the jury would be invited "to choose between alternative meanings" of the disputed claims generating *O2 Micro* error. This court thus must resolve this "actual dispute regarding the proper scope" of the claims.[26] Because the body of claims 1 and 29 of the '123 patent as well as claim 1 of the '323 patent "describe a structurally complete invention,"[27] the preambles to those claims do not limit the meaning of the claims. A careful review shows the disputed language in the preambles as to those claims is repeated in the body of the claim and Cisco identifies no instance in which these preambles provide a unique description of structure referenced later in the claims. In short, there are no necessary antecedent bases in these preambles. In contrast, because the preamble to claim 1 of the '126 patent is necessary for limitations A through E to have meaning, that preamble is limiting.

[25] *See Laboratoires Perouse, S.A.S. v. W.L. Gore & Associates, Inc.*, 528 F. Supp. 2d 362, 372 (S.D.N.Y. 2007) ("The preamble is an introductory phrase that may summarize the invention, its relation to the prior art, or its intended use or properties," but may in some cases constitute a limitation.") (quoting 3-8 Chisum on Patents § 8.06 (2007)).

[26] *O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co., Ltd.*, 521 F.3d 1351, 1360 (Fed. Cir. 2008) ("When the parties raise an actual dispute regarding the proper scope of these claims, the court, not the jury, must resolve that dispute.").

[27] *See supra* note 23.

B. Dispute #2: " Providing Ordered Capture Clocks"

CLAIM TERM/DISPUTE #2	
"providing ordered capture clocks" The '213 patent (claims 1 and 29), the '126 patent (claim 1) and the '323 patent (claim 1)	
SynTest's Preferred Construction	**Cisco's Preferred Construction**
"providing two or more test clocks in a given order"	"triggering at least one clock domain's capture clock pulse in response to activity of another clock domain's capture clock pulse"
CONSTRUCTION/RESOLUTION	
"triggering a capture clock pulse in at least one clock domain in response to a capture clock pulse in another clock domain"	

Two disputes lie between the parties over the construction of "providing ordered capture clocks": (1) whether triggering should be incorporated into the construction and (2) whether a capture clock should be defined as a test clock.

1. Triggering Should Be Incorporated Into the Construction

The asserted patents specifically describe the "invention"[28] as using either "daisy-chain clock triggering" or "token-ring clock enabling" techniques for providing or applying ordered capture clocks:

> In the present invention, the multiple-capture DFT system uses a daisy-chain clock-triggering or token-ring clock-enabling technique to generate and order capture clocks one after the other.[29]
>
> * * *
>
> The multiple-capture DFT system in the present invention further comprises applying an ordered sequence of capture clocks and operating each capture clock at its selected clock speed in the capture operation (cycle). The ordered sequence of capture clocks is applied to

[28] *See Trading Techs. Int'l, Inc. v. eSpeed, Inc.*, 595 F.3d 1340, 1353-54 (Fed. Cir. 2010) (limiting claim by characteristic identified as the "present invention" in the specification, but cautioning against the risk of improperly reading a "preferred embodiment into" the claim) (citing *Saunders Group, Inc. v. Comfortrac, Inc.*, 492 F.3d 1326, 1332 (Fed. Cir. 2007) ("A patent that describes only a single embodiment is not necessarily limited to that embodiment.")); *Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc.*, 381 F.3d 1111, 1117 (Fed. Cir. 2004) ("And, even where a patent describes only a single embodiment, claims will not be read restrictively unless the patentee has demonstrated a clear intention to limit the claim scope using words or expressions of manifest exclusion or restriction." (internal quotations and citations omitted)).

[29] Docket No. 45-1, Ex. A at 4:57-60.

> the circuit under test one-by-one using the daisy-chain clock-triggering or token ring clock-enabling technique.[30]

Both techniques require generation of capture clock pulses for one clock domain in direct response to a capture clock pulse in another clock domain. For example, in the daisy-chain technique, the occurrence of a transition (e.g., from low-to-high or high-to-low) of a preceding clock domain's capture clock pulse triggers generation of capture clock pulses in the next clock domain.[31] The token-ring technique is similar, except that the next domain's capture clock pulses are activated based on the occurrence of a particular signal level (e.g. low or high) in the preceding domain's capture clock pulses.[32] In other words, daisy-chain clock-triggering "uses clock edges to trigger the next operation" and token-ring clock-enabling "uses signal levels to enable the next operation."[33] For both options, the occurrence of the first capture clock pulse of one of the clock domains depends directly on the activity of a capture clock pulse of a previous clock domain.

The term "triggering" encompasses the response requirement because the applicants specifically used the term "triggered" to describe how the claimed invention provided ordered

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[30] *Id.* at 5:34-40.

[31] *See* Docket No. 45-1, Ex. A at 4:66-5:10.

> As an example, assume that the capture cycle contains 4 capture clocks, CK1, CK2, CK3, and CK4. (Please refer to FIGS. 3 and 10 in the DETAILED DESCRIPTION OF THE DRAWINGS section for further descriptions). The daisy-chain clock-triggering technique implies that completion of the shift cycle triggers the GSE signal to switch from shift to capture cycle which in turn triggers CK1, the rising edge of the last CKI pulse triggers CK2, the rising edge of the last CK2 pulse triggers CK3, and the rising edge of the last CK3 pulse triggers CK4. Finally, the rising edge of the last CK4 pulse triggers the GSE signal to switch from capture to shift cycle.

Id. at 5:18-20.

> The only difference between these two techniques is that the former uses clock edges to trigger the next operation, the latter uses signal levels to enable the next operation.

[32] *See id.* at 5:11-16

> The token-ring clock-enabling technique implies that completion of the shift cycle enables the GSE signal to switch from shift to capture cycle which in turn enables CK1, completion of CKI pulses enables CK2, completion of CK2 pulses enables CK3, and completion of CK3 pulses enables CK4.

Id. at 5:18-20.

[33] *Id.* at 5:18-20.

capture clocks in both the '126 and '323 patents.[34] The term also is consistent with the applicants' generic use of the term "trigger" during prosecution of the '213 patent when discussing how the Nadeau-Dostie2 reference "triggered" its domains.[35]

Because the patentee relied on the claim requirement of "applying an ordered sequence of capture clock pulses" in "a sequential order" during prosecution to distinguish the prior art,[36] use of the trigger term is appropriate in the court's construction. At bottom, the foundation of the asserted patents is that the test in the second domain is triggered based on the completion of the test in the first domain – once the first domain is done, the second domain then is activated.[37]

2. A "Capture Clock" Should Not Be Limited to a "Test Clock"

The term "capture clock" appears multiple times in each asserted claim of each asserted

[34] *See* Docket No. 45-2, Ex. B at 23:20-24:2 ("capture clock pulses from two or more selected capture clocks placed in a sequential order such that all clock domains are never triggered simultaneously during a capture operation"); Docket No. 45-3, Ex. C at 22:53-56 (providing "capture clock pulses" in "a sequential order such that all clock domains are never triggered simultaneously during a capture operation").

[35] Ex. G to Cisco Opening Br. at ST000047

> '[A]ll' second domain clock pulses (see B1, B2, and B3 in FIG. 4) in Nadeau-Dostie2 must be aligned at the same positive edge so that they can be 'all' captured simultaneously, which leads to power consumption problems since all scan cells would be triggered simultaneously, every few cycles. In contrast, the present application, however, 'all' second domain clock pulses can be placed in a staggered order or in a sequential order.

See also id. at ST000050 (figure showing Nadeau-Dostie triggering all domain capture pulses simultaneously).

[36] Docket No. 45-7, Ex. G at ST000048. Although the prior art provided an alternative to triggering "clock suppression," Docket No. 47-5, Ex. E (Hetherington and Rajski Paper), that technique was identified during prosecution as problematic because the "shift clock pulses may also need precise timing alignment" and as "a result, it becomes quite difficult to perform at-speed self-test for designs containing clock domains operated at totally unrelated frequencies, e.g., 133 MHz and 60 Mhz." Docket No. 45-1, Ex. A at 3:15-18. To avoid this problem, the asserted patents explain that the invention "uses a daisy-chain clock triggering or token-ring clock enabling technique to generate and order capture clocks." Docket No. 45-1, Ex. A at 4:57-62, 5:34-40. This technique provides a "major benefit" enabling the use of asynchronous clock domains. *Id.* at 5:47-62. When daisy-chain or token-ring clocking is used, there is no need to align any capture clock or shift clock pulses, because each subsequent domain's capture clock pulse necessarily will be triggered after the occurrence of the previous domain's capture clock pulses.

[37] The language in the specification referring to programming does not constitute a third independent technique, but additional refinement to the daisy-chain or token-ring techniques described above – for example by altering the relative order in which the domains are applied.

patent. The parties generally agree that the term "capture clock" in the asserted patents means a "reconfigured system clock."[38] This construction is consistent with language from the asserted patents that the "reconfigured system clocks are called capture clocks."[39] The parties also agree that a single construction ought to control the same term's meaning across the family of patents.[40]

Despite this agreement, SynTest urges that the court substitute the term "capture clock" with the generic term "test clock." SynTest points to the patentees' use of "test clock" once during the prosecution history when referring to the capture clock. But this does not justify SynTest's proposed substitution.[41] When the patentees used the "test clock" term they were merely pointing out that the capture clock in these claims was being used to perform testing and that this particular capture clock was a special type of clock: a clock that provided both capture clock pulses and shift clock pulses, depending on the mode of operation:

> In many designs, a clock domain may be only controlled by one test clock. Thus, this test clock will contain clock pulses applied in scan mode (hence shift clock pulses) and clock pulses in normal mode (hence capture clock pulses).

While it is therefore true that the capture clock claimed in the asserted patents can be used during testing, it does not follow that every "test clock" is a capture clock as claimed in the asserted patents. Indeed, not every test clock is a "reconfigured system clock," which the parties have agreed and the patents confirm is the claimed "capture clock." And not every test clock is the special type that contains both capture clock pulses and shift clock pulses depending on the operational mode – as the patentees stressed the claimed "capture clock" was in this case.

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[38] *See* Docket No. 35, Ex. A at 1 ("capture clock(s)" in all asserted claims means "a reconfigured system clock").

[39] Docket No. 45-1, Ex. A at 9:20; *see also id.* at 1:47-50 (explaining that the patent's concept was to "take over control of all system clocks and reconfigure them as capture clocks").

[40] *See* Docket No. 46 at 10.

[41] *See id.* at 12.

The other justification for using the term "test clock" in this construction is the unremarkable observation that "external tests, like ATEs, are applicable to the present" invention[42] combined with a statement from the specification that, when "scan test is employed, the multiple-capture DFT system is usually resided in [sic] an ATE and, thus, all capture clocks are controlled externally."[43] There is no dispute, however, the reconfigured system clocks that are the "capture clocks" in the asserted patents can be generated internally or controlled externally. The patents explain that the system clocks can be generated inside of the circuit being tested or can be received from an external source at one of their input pins.[44] Whether generated internally or controlled externally, the capture clocks are reconfigured system clocks, and they are clocks that contain both shift clock pulses and capture clock pulses, depending on the operational mode.

In sum, construing the term capture clock to be a test clock is not warranted.

[42] Docket No. 46 at 12.

[43] Docket No. 45-1, Ex. A at 5:52-54.

[44] *Id*. at 1:34-35 ("Each system clock is either directly coming from a primary input (edge pin/connector) or generated internally.").

C. Dispute #3: "Applying an Ordered Sequence of Capture Clock Pulses to All Said Scan Cells Within Said N Clock Domains in Said Normal Mode During a Capture Operation, the Ordered Sequence of Capture Clock Pulses Comprising at Least Two Capture Clock Pulses From Two or More Selected Capture Clocks, for Controlling Two or More Clock Domains, in a Sequential Order"

CLAIM TERM/DISPUTE #3	
"applying an ordered sequence of capture clock pulses to all said scan cells within said N clock domains in said normal mode during a capture operation, the ordered sequence of capture clock pulses comprising at least two capture clock pulses from two or more selected capture clocks, for controlling two or more clock domains, in a sequential order" The '213 patent (claims 1 and 29)	
SynTest's Preferred Construction	**Cisco's Preferred Construction**
"applying in a sequential order one or more capture clock pulses (without including shift clock pulses in the capture window) to the scan cells within a clock domain in normal mode, followed by applying another one or more capture clock pulses (without including shift clock pulses in the capture window) to the scan cells in the next sequentially ordered clock domain in normal mode for that next clock domain and continuing with this sequential order until the test is complete"	"triggering at least one clock domain's capture clock pulse in response to activity of another clock domain's capture clock pulse such that pulses from the capture clocks are received in a sequential order by all said scan cells within said N clock domains in said normal mode during a capture operation, the ordered sequence of capture clock pulses comprising at least two capture clock pulses from two or more selected capture clocks, for controlling two or more clock domains"
CONSTRUCTION/RESOLUTION	
"applying one or more capture clock pulses (without including shift clock pulses in the capture window) to the scan cells within a clock domain in normal mode, followed by applying one or more capture clock pulses (without including shift clock pulses in the capture window) to the scan cells in the next sequentially ordered clock domain in normal mode by triggering a capture clock pulse in the latter clock domain in response to a capture clock pulse in the former clock domain"	

Here, the parties dispute (1) whether "applying an ordered sequence" should be limited to "triggering" (2) whether the capture clock pulses must come from the capture clocks and (3) whether the pulses must be applied to each of N clock domains and (4) whether the phrase "without including shift clock pulses in the capture window" should be included.

In light of the central nature of the triggering concept to the asserted patents discussed above, triggering is included in the court's construction.

SynTest's proposed construction removes the requirement that "capture clock pulses" come "from two or more selected capture" clocks[45] and instead permits the capture clock pulses to come from anywhere. Its proposed construction also eliminates the requirement that the "ordered sequence of capture clock pulses" must be applied to "all scan cells within each of N clock domains of the integrated circuit or circuit assembly during a capture" operation[46] and refers to "continuing with this sequential order until the test is complete," an indefinite concept. Such a construction would provide an argument that a test is "complete," even where (1) capture clock pulses have not been applied to all scan cells within each of N clock domains (2) during a capture operation – features explicitly recited in the claim. These modifications are not warranted.

Cisco also urges the construction also inappropriately reintroduces claim limitations that the applicants deleted from the claims during prosecution in response to a claim rejection.[47] During prosecution of the '213 patent, the PTO specifically objected to the claim phase: "and does not contain any said shift clock pulse during a capture operation" as being not enabled. Patentees responded by deleting that phrase from the claims.[48] A construction that reads that limitation back into the claims is not warranted.[49]

But inspection of the prosecution history reveals such a narrow view of the claim language is not warranted. It is correct that, in response to the Examiner's Section 112 objection, the applicants deleted language from the claim and agreed with the Examiner's statement that only

[45] Docket No. 45-1, Ex. A at 23:32-33; 26:37-38 (requiring "at least two [said] capture clock pulses from two or more selected capture clocks").

[46] *See id.* at 23:28-29; 26:33-35.

[47] Twice the phrase "without including shift clock pulses in the capture window" – referring to pulses provided by a first and second selected capture clock – was deleted following a rejection.

[48] *See* Docket No. 45-7, Ex. G at ST000035, 44-45 (noting that Applicants deleted this language from the claims to obviate the Examiner's enablement rejections under § 112, first and second paragraph).

[49] *See, e.g., 3M Innovative Properties Co. v. Avery Dennison Corp.*, 350 F.3d 1365, 1372 (Fed. Cir. 2004) (refusing to import "sequential" claim limitation in the claim where patentee deleted the limitation in response to a rejection under 35 U.S.C. 112, second paragraph).

capture clock pulses can occur during the capture cycle, when the scan enable signal is inactive.[50] As pointed out to the Examiner during an interview with Dr. Wang and as demonstrated in the diagram Dr. Wang provided, however, the prior art recognizes a distinction between the capture cycle and the capture window or capture operation for purposes of fault testing.[51] Specifically, the prior art LOS methods for delay fault testing require that a last shift clock pulse launch the capture operation.[52] This distinction with the prior art is reflected in the specification.[53] Cisco failed to satisfy its burden of proof that SynTest "unequivocally disavowed a certain meaning to obtain his patent."[54]

[50] *See* Docket No. 45-7, Ex. G at ST000044-45.

[51] *See id.* at ST000050.

[52] *See id.* at ST000045-46.

[53] *See* Docket No. 45-1 at 3:8-11 (the approach discussed by Hetherington "rests on using multiple shift-followed-by-capture clocks each operating at its operating frequency, in a programmable capture window, to detect faults at-speed").

[54] *Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1324 (Fed. Cir. 2003); *Am. Innotek, Inc. v. United States*, 113 Fed. Cl. 668, 677-79 (Fed. Cl. 2013) (review of statements to examiner and figures precluded a finding of disclaimer).

D. Dispute #4: "Applying an Ordered Sequence of Capture Clocks to All Said Scan Cells Within Said N Clock Domains, the Ordered Sequence of Capture Clocks Comprising at Least a Plurality of Capture Clock Pulses From Two or More Selected Capture Clocks Placed in a Sequential Order Such that All Clock Domains Are Never Triggered Simultaneously During a Capture Operation"

CLAIM TERM/DISPUTE #4	
"applying an ordered sequence of capture clocks to all said scan cells within said N clock domains, the ordered sequence of capture clocks comprising at least a plurality of capture clock pulses from two or more selected capture clocks placed in a sequential order such that all clock domains are never triggered simultaneously during a capture operation" The '126 patent (claim 5) and the '323 patent (claim 1)	
SynTest's Preferred Construction	**Cisco's Preferred Construction**
"applying in a sequential order one or more capture clock pulses (without including shift clock pulses in the capture window) from a first selected test clock, which is derived from a first system clock, to the scan cells within a first one or more clock domains the first selected test clock controls, followed by applying another one or more capture clock pulses (without including shift clock pulses in the capture window) from a second selected test clock, which is derived from a second system clock, to the scan cells within a second one or more clock domains the second selected test clock controls, and continuing with this sequential order until the test is complete such that not all clock domains are ever activated simultaneously"	"triggering at least one clock domain's capture clock pulse in response to activity of another clock domain's capture clock pulse such that pulses from the capture clocks are received in a sequential order by all said scan cells within said N clock domains, the ordered sequence of capture clocks comprising at least a plurality of capture clock pulses from two or more selected capture clocks and such that all clock domains are never triggered simultaneously during a capture operation"
CONSTRUCTION/RESOLUTION	
"applying one or more capture clock pulses (without including shift clock pulses in the capture window) to the scan cells within a clock domain in normal mode, followed by applying one or more capture clock pulses (without including shift clock pulses in the capture window) to the scan cells in the next sequentially ordered clock domain in normal mode by triggering a capture clock pulse in the latter clock domain in response to a capture clock pulse in the former clock domain such that all clock domains are never triggered simultaneously during a capture operation"	

In addition to the disputes resolved in the two preceding constructions, dispute number four raises the additional issues of whether the construction should (1) delete "during a capture operation" from the claim – to prohibit simultaneous triggering even during the shift operation, (2) whether the term "activated" can be substituted for the term "triggered," (3) whether one

capture clock may control multiple clock domains and (4) whether the agreed construction of "capture clock" can be substituted with "test clock from which is derived a system clock."

This claim term is similar to the claim phrase reviewed above, except that it contains an additional requirement that "all clock domains are never triggered simultaneously during a capture operation." The court will not rehash its analysis above.

SynTests's construction of this term also deletes "during a capture operation" from the claim phrase "such that all clock domains are never triggered simultaneously during a capture operation." Although the claim specifically states the time period when all clock domains should not be simultaneously triggered – during a capture operation – the proposed construction removes that language from the claim so that the claims also prohibit simultaneously triggering clock domains during a shift operation. This construction that is inconsistent with the relevant specifications. For example, Figure 13 of the '323 patent illustrates that the first pulses in the shift cycle for all clocks are triggered simultaneously. The proposed construction transparently and retroactively sidesteps prior art: this is improper.

Without justification SynTest's proposed construction also substitutes the term "activated" for "triggered." Elsewhere in its argument, SynTest draws a distinction between "triggering" and other types of activation (e.g., enabling), but no accounting of the difference between the two is laid out in support of such a distinction. If "triggered" only referred to the very specific "daisy-chain" technique, it would be inappropriate to substitute the specific term "triggered" with a generic term "activated." Because the claim uses the term "triggered," the same term should be used in the construction.

E. Dispute #5: Independent Claims 1 and 29 Do Not Require Delay Fault Testing to Be At Speed

CLAIM TERM/DISPUTE #5	
"when detecting or locating selected delay faults within a clock domain said selected capture clock controlling the clock domain contains at least two consecutive said capture clock pulses to launch the transition and capture the output response" The '213 patent (claims 1 and 29)	
SynTest's Preferred Construction	**Cisco's Preferred Construction**
"testing of delay faults is performed by applying two or more consecutive capture clock pulses to the clock domain with the first pulse initiating (launches) the transition, and the next one or more pulses that capture the output response at one or more scan cell(s)"	"when detecting or locating selected delay faults within a clock domain, said selected capture clock controlling the clock domain contains at least two consecutive said capture clock pulses generated at the domain's rated clock speed to launch the transition and capture the output response"
CONSTRUCTION/RESOLUTION	
"testing of delay faults is performed by applying two or more consecutive capture clock pulses to the clock domain with the first pulse initiating (launching) the transition at a targeted terminal and each subsequent pulse capturing the response at a scan cell"	

Cisco urges the delay fault testing must be done at speed, but SynTest counters this construction is inconsistent with dependent claim 15 that claims delay fault testing at speed. If at speed is read into the independent claims 1 and 29 and then dependent claim 15 is rendered a nullity under the doctrine of claim differentiation.[55]

The court agrees with SynTest. "The doctrine of claim differentiation is 'based on the common sense notion that different words or phrases used in separate claims are presumed to indicate that the claims have different meanings and scope.'"[56] "The doctrine is not a hard and fast

[55] *See* Docket No. 45-1, Ex. A

> 15. The method of claim 1, wherein said applying an ordered sequence of capture clock pulses further comprises selectively operating all said capture clock pulses controlling a selected clock domain at their rated clock speed, for detecting or locating delay faults within said selected clock

[56] *Starhome GmbH v. AT&T Mobility LLC*, Case No. 2012-1694, 2014 WL 685639, at *7 (Fed. Cir. Feb. 24, 2014) (quoting *Karlin Tech. Inc. v. Surgical Dynamics, Inc.*, 177 F.3d 968, 971-72 (Fed. Cir. 1999)).

rule, but instead "a rule of thumb that does not trump the clear import of the specification.'"[57] In this case, a common sense comparison of the independent and dependent claims shows that the additional requirement of default testing at speed should not be read into the claim.

F. Dispute #6: The Ordering of Claim Steps 1(a) Through 1(e) of Claim 1 of the '126 Patent

CLAIM TERM/DISPUTE #6	
The ordering of claim steps (a) through (e) in claim 1 of the '126 patent.	
SynTest's Preferred Construction	**Cisco's Preferred Construction**
The order is not limiting and the elements can follow in any order.	The claimed steps must occur in the following order: 1(a), 1(b), 1(c), 1(d) and then 1(e).
CONSTRUCTION/RESOLUTION	
The claimed steps 1(a), 1(b) and 1(c) must precede steps 1(d) and 1(e).	

Claim 1 of the '126 patent provides for certain steps in a particular order:

> (a) compiling the HDL code or netlist that represents said integrated circuit or circuit assembly in physical form into a design database;
>
> (b) performing test rule check for checking whether said design database contains any multiple-capture rule violations in said scan-test or said self-test mode;
>
> (c) performing test rule repair until all said multiple-capture rule violations have been fixed;
>
> (d) performing multiple-capture test synthesis for generating a testable HDL code or netlist; and
>
> (e) generating HDL test benches and automatic test equipment (ATE) test programs for verifying the correctness of said testable HDL netlist in said scan-test or said self-test mode.[58]

The parties dispute whether the method claim elements listed above must be performed in order.[59] SynTest urges that for the order of a method claim to be binding it must be "unequivocally

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[57] *Id.* (quoting *Edwards Lifesciences LLC v. Cook Inc.*, 582 F.3d 1322, 1332 (Fed. Cir. 2009)); *see also Netcraft Corp. v. eBay, Inc.*, 549 F.3d 1394, 1400 n.1 (Fed. Cir. 2008) ("While claim differentiation may be helpful in some cases, it is just one of many tools used by courts in the analysis of claim terms.").

[58] *See* Docket No. 45-2, Ex. B at 22:39-64.

[59] Although "a method claim necessarily recites the steps of the method in a particular order, as a general rule the claim is not limited to performance of the steps in the order recited, unless the claim explicitly or implicitly requires a specific order." *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1345 (Fed. Cir. 2008) (citing *Interactive Gift Express, Inc. v. Compuserve Inc.*, 256

dictated;"[60] but *Baldwin Graphics* does not support such a per se requirement. The *Baldwin* court's holding was milder: the claim need only "implicitly or explicitly" require a specific order in light of the specification.[61] Here, all of the multiple-capture rule violations must be identified before steps (d) and (e) may be completed. It is insufficient for any violation to be missed, because the resulting netlist then may not detect the faults in design. The court holds – and the parties agreed at oral argument – that not all violations must be identified before each may be fixed – step B need not be completed, in its entirety, before Step C is performed.

G. Dispute #7: The Meaning of Checking Whether Said Design Database Contains Any Multiple Capture Violations

CLAIM TERM/DISPUTE #7	
The meaning of checking whether said design database contains any multiple capture violations The '126 patent (claim 1)	
SynTest's Preferred Construction	**Cisco's Preferred Construction**
"verifying whether the design complies with scan and BIST-specific design rules"	"identifying each multiple capture rule violation that exists in the design database"
CONSTRUCTION/RESOLUTION	
verifying whether the design complies with scan and BIST-specific design rules.	

In the design of an ASIC, the goal is to fix all rule violations. The parties dispute whether the claim requires all rule violations to be identified before all identified rule violations can be fixed. The dispute with respect to whether such an ordering is required turns on whether "'any' multiple-capture rule violation as used in the Claim step 1(b) refers to 'all' multiple capture

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F.3d 1323, 1342-43 (Fed. Cir. 2001). Despite that backdrop, the "specification or prosecution history" may "require a narrower, order-specific construction of a method claim in some cases." *Id.* (citing *Interactive Gift Express, Inc. v. Compuserve Inc.*, 256 F.3d 1323, 1342-43 (Fed. Cir. 2001).

[60] *See* Docket No. 50 at 22 (citing *Baldwin Graphic*, 512 F.3d at 1345).

[61] *See supra* note 59.

violations."[62] If after a review, no multiple-capture rule violations are found, the next step of fixing all rule violations is completed by doing nothing. Similarly, Cisco's reference to the use of the word "any" in the specification as it relates to clock skews is simply unavailing. The term "any" is used repeatedly in the claim language itself, without signifying all is meant. For example, the preamble states that what is claimed is an "apparatus for providing ordered capture clocks to detect or locate faults within N clock domains and faults crossing any two clock domains."[63] Any cannot mean all in this context. Similarly, one dependent claim includes the phrase "applying said capture clock pulses concurrently to two or more selected clock domains which do not interact with each other or do not have any logic block crossing."[64] Any could not mean all in this context, either.

The parties agree that multiple-capture refers to a method for delay testing.[65] Cisco does not contend that there is anything indefinite about the term "rule violations" as it relates to delay fault testing of an ASIC in design. One "of ordinary skill in the relevant art could not discern" that multiple-capture rules violations refer to delay testing violations that would apply to the multiple-capture methods of delay fault testing.[66]

[62] Docket No. 51 at 24.

[63] Docket No. 45-3 at 22:39-31.

[64] *See id.* at 23:28-30.

[65] Docket No. 51 at 25:7-10.

[66] *Haliburton Entergy Servs., Inc. v. M-I LLC*, 514 F.3d 1244, 1249-1250 (Fed. Cir. 2008).

H. Dispute #8: "Each Shift Clock Pulse Comprising a Clock Pulse Applied in Scan Mode"

CLAIM TERM/DISPUTE #8	
"each shift clock pulse comprising a clock pulse applied in scan mode" The '213 patent (claims 1, 29) and the '126 patent (claim 1)	
SynTest's Preferred Construction	**Cisco's Preferred Construction**
"each waveform from a clock which generates a shift clock pulse at a frequency that need not be at the same speed as the normal operating frequency of that domain's system clock"	"each shift clock pulse comprising a pulse of the capture clock applied while a scan enable signal for the clock domain is asserted"
CONSTRUCTION/RESOLUTION	
"each shift clock pulse comprising a pulse of the capture clock at a frequency that need not be the same as the normal operating frequency of the domain's system clock"	

The parties agree that "each shift clock pulse comprising a clock pulse applied in scan mode" can be construed as a pulse of a test clock when scan enable is active. Cisco attempts to limit the clock that can generate this pulse to a reconfigured system clock, the same clock generating the capture clock pulses with both the shift clock pulses and the capture clock pulses being generated at the same frequency. This construction ignores the specification, which identifies the reach of the invention to embrace both self-test and scan-test.[67] Additionally, the specification recognizes that separate clocks can be responsible for shift clock pulses and capture clock pulses.[68] As Cisco acknowledges, while adequate delay fault testing requires capture clock pulses be at-speed[69] "the shifting frequency is irrelevant to at-speed testing."[70] This is because "testing of delay faults at-speed [with this invention] is now performed by applying two

[67] *See* Docket No. 45-1, Ex. A at 4:39-42 ("This invention applies to any self-test or scan-test method that requires multiple capture clock pulses (without including shift clock pulses) in the capture cycle.").

[68] *See id.* at 5:28-32.

[69] *See* Docket No. 44 at 18:2-20.

[70] *See id.* at 19:6-9 (quoting Docket No. 45-1, Ex. A at 4:19-22).

consecutive capture clock pulses (double captures) rather than using the shift followed- by-capture clock pulses."[71]

I. Dispute #9: "Each Capture Clock Pulse Comprising a Clock Pulse Applied in Normal Mode"

CLAIM TERM/DISPUTE #9	
"each capture clock pulse comprising a clock pulse applied in normal mode" The '213 patent (claims 1, 29) and the '126 patent (claim 1)	
SynTest's Preferred Construction	**Cisco's Preferred Construction**
"each waveform from a clock which generates capture clock pulses that need not be at the same speed as the clock when generating shift clock pulses"	"each capture clock pulse comprising a pulse of the capture clock applied while a scan enable signal for the clock domain is not asserted"
CONSTRUCTION/RESOLUTION	
"each capture clock pulse comprising a pulse of the capture clock at a frequency that need not be the same as the clock when generating shift clock pulses"	

The discussion to dispute number eight applies with equal force to dispute number nine.

[71] *See id.* at 4:49-52.

J. What Means-Plus-Function Structures are Disclosed in the Specification of the '323 Patent

CLAIM TERM/DISPUTE #10	
What structures are disclosed by the specification with respect to "means for generating and shifting-in N test stimuli to all said scan cells within said N clock domains in said integrated circuit or circuit assembly during a shift-in operation" The '323 patent (claim 1)	
SynTest's Preferred Construction	**Cisco's Preferred Construction**
Means: Generating test stimuli **Structure:** If self-test – PRPG is responsible for generating N Test stimuli. Use of a phase shifter is optional. If scan-test – ATPG is responsible for generating N Test stimuli **Means:** for shifting-in test stimuli **Structure:** If self-test – the DFT system controls the operation and can utilize the system clock or any other clock. If scan-test – the ATE	**Means:** Generating test stimuli **Structure:** PRPG combined with a phase shifter **Means:** for shifting in test stimuli **Structure:** The reconfigured system clock
CONSTRUCTION/RESOLUTION	
Function: Generating N test stimuli. **Structure:** If self-test – the PRPG with or without a phase shifter. If scan-test – the ATPG. **Function:** Shifting-in N test stimuli. **Structure:** If self-test – the DFT system. If scan-test – the ATE.	

Because the parties agree on the function, the only issue before the court is the corresponding structure. The parties agree that there are two elements to the structure: (1) generating N test stimuli and (2) shifting in N test stimuli to all said scan cells. With respect to the first structure, Cisco contends that "the specification unambiguously explains that PRPGs combined with phase shifters are used to generate test stimuli."[72] Cisco ignores that the phase shifters are identified as "optional" by the patent.[73] Moreover, by citing only to the PRPG, Cisco again attempts to limit the invention to self-test. A PRPG is not a requirement for scan-test.

[72] Docket No. 44 at 21:15-16.

[73] Docket No. 45-3 at 22:5-7 ("Each PRPG-MISR pair is composed of a PRPG, an optional phase shifter, an optional space compactor, a MISR, and a comparator.").

Cisco identifies the "capture clock" as the structure for the second element citing that "[d]uring each shift cycle" a "series of pulses" are "applied through capture clocks" to shift stimuli to all scan cells within all clock" domains.[74] Cisco again cites to the capture clock in an effort to read out scan-test, which is inappropriate for all the reasons discussed above.

By contrast, and to address the fact that the invention covers both scan-test and self-test, SynTest identified the DFT system as the structure for both the generation of test stimuli and the shifting in of data. The specification explicitly supports this structure as performing both functions in both scan-test and self-test.[75] SynTest argues that the shifting operation is different from the capture operation and the clocks therefore need not be at the same speeds and can originate from different clocks. Cisco's construction improperly requires a scan-enabled system, but the claim language does not require this limitation.

The court agrees that scan design is not completely dependent upon the use of a scan-enabled signal. While the use of a scan-enabled signal may be the most common way to shift data in and out of a scan chain during test, the specification makes clear that the "multiple-capture DFT system of the present invention further comprises any method or apparatus for performing the shift operation at any selected clock speed within each clock" domain.[76] The specification also recognizes that separate clocks can generate shift clock pulses and capture clock pulses.[77] Cisco's additional limitations are unwarranted.

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[74] *See* Docket No. 44 at 19:16-18 (quoting Docket No. 45-1, Ex. A at 10:47-50).

[75] *See* Docket No. 45-3, Ex. C at 9:16-20 ("During the shift operation, the multiple-capture DFT system first generates and shifts pseudorandom or predetermined stimuli through all scan cells SC in all scan chains SCN . . . ."); 5:46-50 ("When self-test is employed, the multiple-capture DFT system is usually placed inside the integrated circuit . . . . When scantest is employed, the multiple-capture DFT system is usually resided in an ATE.").

[76] *See* Docket No. 45-1, Ex. A at 4:31-33.

[77] *See id.* at 5:28-32.

IT IS SO ORDERED.

Dated: June 9, 2014

PAUL S. GREWAL
United States Magistrate Judge