United States District Court
Northern District of California

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN JOSE DIVISION

VIA TECHNOLOGIES, INC. (A CALIFORNIA CORPORATION), et al.,

Plaintiffs,

v.

ASUS COMPUTER INTERNATIONAL, et al.,

Defendants.

Case No. 14-cv-03586-BLF

ORDER CONSTRUING CLAIMS IN U.S. PATENT NO. 7,313,187

[Re: ECF 116]

Plaintiffs VIA Technologies, Inc., a California corporation, VIA Technologies, Inc., a Taiwan corporation, and VIA Labs, Inc., (collectively, "Via") bring this action alleging patent infringement and trade secret misappropriation against Defendants ASUS Computer International, ASUSTeK Computer Inc., and ASMedia Technology Inc. ("ASM") (collectively, "Asus"). The patent portion of the lawsuit alleges Asus infringes Via's U.S. Patent No. 7,313,187 (the "'187 Patent"). The Court held a tutorial on June 3, 2016, and a *Markman* hearing on June 10, 2016, for the purpose of construing five disputed terms in the '187 Patent.

I. BACKGROUND ON THE '187 PATENT

The '187 Patent is titled "High Speed Serial Linking Device with De-Emphasis Function and the Method Thereof." As computers require higher and higher rates of data transmission, it becomes more difficult to transmit data while minimizing signal loss on a circuit board. '187 Patent at 1:20-24, 27-30. The '187 Patent describes and claims solutions to improve signal integrity in a high-speed circuit environment. '187 Patent at 1:60-2:35. It accomplishes this by taking a stream of data bits (a string of "0's" and "1's") and using a technique known as "de-emphasis." '187 Patent at 1:29-31, 1:32-47. In a computers, the data bits of "0's" and "1's" are represented through voltages with a "1" being transmitted using a positive voltage and a "0" being transmitted using a negative voltage. '187 Patent at 1:10-2:35. With de-emphasis, the magnitude

between the signal voltages is increased for the first "1" or "0" in each string of "1's" or "0's", while decreased (or de-emphasized) for the remainder of the 1's or 0's in the string. '187 Patent at 1:32-47. De-emphasis makes it easier to reduce signal loss and increase signal quality at high speeds. '187 Patent at 1:60-2:35.

A. Claim Terms at Issue

The parties disagree over the specific claim terms that must be construed. In its Patent L.R. 4-1 disclosures, ASUS identified "to serialize the parallel data into a serial data and a delayed serial data" as a proposed phrase for construction. Exh. 17 to Reply 3, ECF 133-4. At claims construction, ASUS seeks not only construction of that phrase but also the following terms found within this phrase: "parallel data," and "serial data." Opp. 14, ECF 126. VIA argues that ASUS waived construction of "parallel data" and "serial data" by not including these terms in their Patent L.R. 4-1 disclosures. Reply 5, ECF 133.

The Court agrees with VIA and finds ASUS did not properly disclose "parallel data" and "serial data" in its Patent L.R. 4-1 disclosures. Rule 4-1(a) requires parties to serve on each other a list of claim terms that should be construed by the Court. Parties may not attempt an end run around this rule by disclosing a large phrase and then seeking to construe specific terms within that phrase. Holding otherwise would allow parties to hide the ball and render the claim construction process meaningless. Accordingly, the Court will not construe "parallel data" and "serial data" because ASUS did not comply with the patent local rules.

B. Evidentiary Objections

VIA objects to Dr. Nelson's deposition testimony at 208:14-16, 208:17-212:11, 212:12-214:05 because opposing counsel "coached Dr. Nelson during his deposition, provided him with incomplete documents that omitted information contrary to their positions, and had him provide new opinions despite his earlier sworn testimony that all his opinions had already been disclosed." Reply 13, ECF 133. As an initial matter, ASUS cites to Exhibit 3 to its brief as containing Dr. Nelson's deposition testimony at 208:14-16, 208:17-212:11, 212:12-214:05. Opp. 11, ECF 126. However, Exhibit 3 does not contain these excerpts of Dr. Nelson's deposition. Bhakar Decl. ¶ 4, ECF 126-1 ("Attached hereto as Exhibit 3 are true and correct copies of excerpts from the January

8, 2016 Deposition of Dr. Brent E. Nelson including 61:02-68:09, 156:20-160:24."). In any event, VIA attached the relevant portions of Dr. Nelson's deposition at Exhibit 16 to its reply. ECF 133-3. The Court has reviewed Exhibit 16 and does not find Dr. Nelson was improperly coached, provided with incomplete documents, or otherwise violated the rules of evidence requiring excerpts of his testimony to be stricken. His transcript reveals nothing more than the ordinary interaction between parties engaged in a deposition. Accordingly, the Court OVERRULES VIA's objections.

ASUS objects to Mr. Gomez's opinions at paragraphs 31, 80-87, 89-93, 95-98, 102-106, 108 of his report as being conclusory. Opp. 25, ECF 126. ASUS argues that at his deposition, Mr. Gomez would not point to any specific intrinsic or extrinsic evidence that he relied upon in forming his opinions and instead stated he was relying on his "background as having 30 years of experience in the industry." *Id*. VIA responds that Mr. Gomez's testimony as a person of ordinary skill is relevant to the terms and that he also explained he reviewed the '187 Patent, its file history, references cited in the prosecution history, and other documents. Reply 11, ECF 133. The Court agrees with VIA and finds that Mr. Gomez adequately supported his opinions on claims construction through his experience and reliance on relevant documents. ASUS's reliance on *GPNE Corp. v. Apple, Inc.*, 2014 U.S. Dist. LEXIS 53234 (N.D. Cal. Apr. 16, 2014), is misplaced because *GPNE* excluded the testimony of a reasonable royalty expert who only relied upon his 30 years of experience, instead of a reliable and testable methodology. *Id*. at *18-19. In contrast, at claims construction, the perspective of a skilled artisan is relevant to construing terms. Accordingly, the Court OVERRULES ASUS's objections.[1]

II. LEGAL STANDARD

A. General Principles

Claim construction is a matter of law. *Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 387 (1996). "It is a 'bedrock principle' of patent law that 'the claims of a patent define the

[1] ASUS also notes that a motion to strike Mr. Gomez's testimony was pending when it filed its brief. Opp. 25, ECF 126. That motion was subsequently granted in part, with the Court denying ASUS's motion to strike Mr. Gomez's testimony but allowing ASUS to conduct an additional deposition of him. ECF 158.

invention to which the patentee is entitled the right to exclude," *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (internal citation omitted), and, as such, "[t]he appropriate starting point . . . is always with the language of the asserted claim itself," *Comark Commc'ns, Inc. v. Harris Corp.*, 156 F.3d 1182, 1186 (Fed. Cir. 1998).

Claim terms "are generally given their ordinary and customary meaning," defined as "the meaning . . . the term would have to a person of ordinary skill in the art in question . . . as of the effective filing date of the patent application." *Phillips*, 415 F.3d at 1313 (internal citation omitted). The court reads claims in light of the specification, which is "the single best guide to the meaning of a disputed term." *Id.* at 1315; *see also Lighting Ballast Control LLC v. Philips Elecs. N. Am. Corp.*, 744 F.3d 1272, 1284-85 (Fed. Cir. 2014) (en banc). Furthermore, "the interpretation to be given a term can only be determined and confirmed with a full understanding of what the inventors actually invented and intended to envelop with the claim." *Phillips*, 415 F.3d at 1316 (quoting *Renishaw PLC v. Marposs Societa' per Azioni*, 158 F.3d 1243, 1250 (Fed. Cir. 1998)). The words of the claims must therefore be understood as the inventor used them, as such understanding is revealed by the patent and prosecution history. *Id.* The claim language, written description, and patent prosecution history thus form the intrinsic record that is most significant when determining the proper meaning of a disputed claim limitation. *Id.* at 1315-17; *see also Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996).

Evidence external to the patent is less significant than the intrinsic record, but the court may also consider such extrinsic evidence as expert and inventor testimony, dictionaries, and learned treatises "if the court deems it helpful in determining 'the true meaning of language used in the patent claims.'" *Philips*, 415 F.3d at 1318 (quoting *Markman*, 52 F.3d at 980). However, extrinsic evidence may not be used to contradict or change the meaning of claims "in derogation of the 'indisputable public records consisting of the claims, the specification and the prosecution history,' thereby undermining the public notice function of patents." *Id.* at 1319 (quoting *Southwall Techs., Inc. v. Cardinal IG Co.*, 54 F.3d 1570, 1578 (Fed. Cir. 1995)).

B. Means-Plus-Function Claims

Paragraph 6 of 35 USC § 112 provides for means-plus-function claiming: "An element in a

claim for a combination may be expressed as a means . . . for performing a specified function . . . and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof." When a claim uses the term "means" to describe a limitation, it creates a presumption that the inventor used the term to invoke § 112 ¶ 6. *Biomedino v. Waters Technologies*, 490 F.3d 946, 950 (Fed. Cir. 2007). The "presumption can be rebutted when the claim, in addition to the functional language, recites structure sufficient to perform the claimed function in its entirety." *Id.*

If a court concludes that a claim limitation is a means-plus-function limitation, "two steps of claim construction remain: 1) the court must first identify the function of the limitation; and 2) the court must then look to the specification and identify the corresponding structure for that function." *Id.* The claim limitation will then be construed to cover that corresponding structure and equivalents thereof. 35 USC § 112 ¶ 6.

III. CONSTRUCTION OF DISPUTED TERMS

A. "a parallel-to-serial unit which receives a parallel data to serialize the parallel data into a serial data and a delayed serial data"

Via's Proposal	Asus's Proposal	Court's Construction
Plain and ordinary meaning Alternative: "a module that receives a parallel data to convert the parallel data into a serial data and a delayed data."	This phrase should be construed as a means plus function limitation governed by 35 U.S.C. § 112 paragraph 6: function: "(which) receives a parallel data to serialize the parallel data into a serial data and a delayed serial data" corresponding structure: serializers 212, 214 and register 216 of FIG. 3A	function: "(which) receives a parallel data to serialize the parallel data into a serial data and a delayed serial data" corresponding structure: serializers 212, 214 and register 216 of FIG. 3A

Via argues that no construction is necessary because a skilled artisan would readily understand the phrase "a parallel-to-serial unit which receives a parallel data to serialize the parallel data into a serial data and a delayed serial data." Mot. 5, ECF 116. Asus argues that this phrase should be construed as a means-plus-function limitation because it does not recite any

definite structure but rather recites functions. Opp. 6, ECF 126.

The Court agrees with Asus and finds that this term is in means-plus-function format. First, the Court recognizes that the term "a parallel-to-serial unit which receives a parallel data to serialize the parallel data into a serial data and a delayed serial data" does not include the word "means," and thus, there is a rebuttable presumption that the term is not subject to § 112(6). Therefore, the Court must analyze whether the term fails to "recite sufficiently definite structure" or recites "function without reciting sufficient structure for performing that function." *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1349 (Fed. Cir. 2015) (partially en banc). Here, the term recites function without reciting a sufficient structure for performing that function. The word "unit" is a generic descriptor and does not describe a sufficiently definite structure. *See, e.g. Williamson*, 792 F.3d at 1350-51. Attaching the pre-fix "parallel-to-serial" also does not impart structure on the term "parallel-to-serial unit." *Id*. at 1351 ("The prefix 'distributed learning control' does not impart structure into the term 'module.' These words do not describe a sufficiently definite structure."). The '187 Patent also depicts the "parallel-to-serial unit" as black boxes that do not connote any specific structure, '187 Patent at Fig. 2 boxes 210, 230, 250, unlike other components which are described using specialized shapes, '187 Patent at Fig. 2 boxes 212 and 214 (serializer) and 216 (register). Thus, the patent does not connote any specific structure to the "parallel-to-serial unit."

Via's arguments in opposition are not persuasive because their arguments revolve around describing the structure in terms of function. *See, e.g.*, Gomez Report (Exhibit 16) to Mot. ¶ 83, ECF 116-16 (A person of ordinary skill in the art would understand that the "a parallel-to-serial unit which receives a parallel data to serialize the parallel data into a serial data and a delayed serial data…."). As a result the term "parallel-to-serial unit" does not connote anything about its structure and the Court finds that the term "parallel-to-serial unit" would not be understood by a skilled artisan as having sufficient structure for performing the recited functions of "receiv[ing] a parallel data to serialize the parallel data into a serial data and a delayed serial data."

Under § 112(6), the Court must determine the claimed functions and then determine the corresponding structure that performs those functions. *See Med. Instrumentation & Diagnostics*

Corp. v. Elekta AB, 344 F.3d 1205, 1210 (Fed. Cir. 2003). Asus's proposed function of "receives a parallel data to serialize the parallel data into a serial data and a delayed serial data" is supported by the claim language and accurately describes the function of the "parallel-to-serial unit." Accordingly, the Court construes the term's function as "receives a parallel data to serialize the parallel data into a serial data and a delayed serial data."

As to structure, Asus argues that Fig. 3A and corresponding text at 3:13-25 of the '187 Patent describe the structure necessary to carry out the functions of the "parallel-to-serial unit." The specification indicates that the two serializers in Fig. 3A (box 212 and 214) receive parallel data. '187 Patent at 3:15-17 ("Serializer 212 receives parallel data…."). These two serializers and the register at box 216 carry out the second function "to serialize the parallel data into serial data and delayed data."). '187 Patent at 3:15-22 ("Serializer 212 receives parallel data, [D0, D1,...D9], serializes the parallel data and outputs serial data DT. Register 216 is used to store the last bit D9 in the parallel data and output it after one serial bit time."). As a result, based on the specification, serializers 212, 214, and register 216 are the corresponding structures for this means-plus-function term.

B. "to serialize the/serializing the parallel data into a serial data and a delayed serial data"

Via's Proposal	Asus's Proposal	Court's Construction
Plain and ordinary meaning. Alternative: "converting a parallel data into a serial data and a delayed serial data"	"the act of converting two or more lines of parallel data into a single-wire serial data signal where the individual bit values on the wires of the parallel data are output serially (one after another) on a single wire"	"the act of converting two or more streams of parallel data into a single stream serial data where the individual bit values of the parallel data are output serially (one after another)"

The disputed term "to serialize the/serializing a parallel data into a serial data and a delayed serial data" appears in independent claims 1 and 13 of the '187 Patent. Claim 1 is representative of how the term is used in the claim language:

1. A high-speed serial linking device with de-emphasis function, comprising:

a parallel-to-serial unit which receives a parallel data **to serialize the parallel data**

into a serial data and a delayed serial data, wherein the delayed serial data is one serial bit time lag behind the serial data;

a pre-driver which receives the serial data and the delayed serial data to output a data differential pair according to the serial data and output a delayed-and-inverted differential pair according to the delayed serial data, wherein the delayed-and-inverted differential pair is the inverse of and one serial bit time lag behind the data differential pair; and

an output driver unit which receives the data differential pair and the delayed-and-inverted differential pair to output a de-emphasized transmission differential pair.

'187 Patent at 5:51-67 (emphasis added).

At the *Markman* hearing, both parties agreed that "to serialize the/serializing the parallel data into a serial data and a delayed serial data" should be construed as "the act of converting two or more streams of parallel data into a single stream serial data where the individual bit values of the parallel data are output serially (one after another)." Accordingly, the Court adopts this construction.

C. "one serial bit time lag"

Via's Proposal	Asus's Proposal	Court's Construction
Plain and ordinary meaning Alternative: "delayed by a single serial bit"	"the amount of time required to transmit one serial bit"	"delayed by the duration of one serial bit"

The disputed term "one serial bit time lag" appears in independent claims 1 and 13 of the '187 Patent. Claim 1 is representative of how the term is used in the claim language:

1. A high-speed serial linking device with de-emphasis function, comprising:

a parallel-to-serial unit which receives a parallel data to serialize the parallel data into a serial data and a delayed serial data, wherein the delayed serial data is **one serial bit time lag** behind the serial data;

a pre-driver which receives the serial data and the delayed serial data to output a data differential pair according to the serial data and output a delayed-and-inverted differential pair according to the delayed serial data, wherein the delayed-and-inverted differential pair is the inverse of and one serial bit time lag behind the data differential pair; and

an output driver unit which receives the data differential pair and the delayed-and-inverted differential pair to output a de-emphasized transmission differential pair.

’187 Patent at 5:51-67 (emphasis added).

At the *Markman* hearing, both parties agreed that “one serial bit time lag” should be construed as “delayed by the duration of one serial bit.” Accordingly, the Court adopts this construction.

D. “differential pair”

Via’s Proposal	Asus’s Proposal	Court’s Construction
Plain and ordinary meaning Alternative: “a pair of complementary signals used to transmit information”	“a signal conveyed using two wires where the data value of the signal is represented by a voltage on one of the two wires and the inverse of that voltage on the other wire”	“a pair of complementary signals used to transmit information”

The disputed term “differential pair” appears in independent claims 1 and 13 and dependent claims 3, 6, 7, 10, 14, and 18 of the ’187 Patent. Claim 1 is representative of how the term is used in the claim language:

> 1. A high-speed serial linking device with de-emphasis function, comprising:
>
> a parallel-to-serial unit which receives a parallel data to serialize the parallel data into a serial data and a delayed serial data, wherein the delayed serial data is one serial bit time lag behind the serial data;
>
> a pre-driver which receives the serial data and the delayed serial data to output a data **differential pair** according to the serial data and output a delayed-and-inverted **differential pair** according to the delayed serial data, wherein the delayed-and-inverted **differential pair** is the inverse of and one serial bit time lag behind the data **differential pair**; and
>
> an output driver unit which receives the data **differential pair** and the delayed-and-inverted **differential pair** to output a de-emphasized transmission **differential pair**.

’187 Patent at 5:51-67 (emphasis added).

At the *Markman* hearing, both parties agreed that “differential pair” should be construed as a “pair of complementary signals used to transmit information.” Accordingly, the Court adopts this construction.

E. "[data] differentiator"

Via's Proposal	Asus's Proposal	Court's Construction
"module that outputs a data differential pair"	"an AND and NOR gate circuit combination that is controlled by a pair of control signals to convert a single wire serial signal into a differential pair signal"	"circuit that outputs a data differential pair"

The disputed term "[data] differentiator" appears in dependent claim 3 of the '187 Patent. Claim 3 states:

> 1. The high-speed serial linking device according to claim 1, wherein the pre-driver comprises:
>
> a **data differentiator** which receives the serial data and accordingly outputs the data differential pair; and;
>
> an inverse **data differentiator** which receives the delayed serial data and outputs the delayed-and-inverted differential pair.

'187 Patent at 6:11-17 (emphasis added).

VIA argues that "data differentiator" should be construed as a "module that outputs a data differential pair." Mot. 16, ECF 116. According to VIA, the specification describes a data differentiator broadly as something that receives serial data and outputs a data differential pair. *Id.* (citing '187 Patent at 3:39-44, 6:13-14). At the *Markman* hearing, VIA modified its proposal to a "circuit that outputs a differential pair."

Asus counters that the '187 Patent uses "differentiator" in a manner inconsistent with its ordinary meaning and therefore, the patentee has acted as his own lexicographer. Opp. 21-22, ECF 126. As a result, Asus argues that the term must be construed according to the special meaning given to "differentiator" in the patent. *Id.* Since the '187 Patent does not include an express definition for "differentiator," Asus relies upon Figure 4 of the '187 Patent to reach its proposed construction that the differentiator have "AND and NOR gate circuit combination that is controlled by a pair of control signals to convert a single wire serial signal into a differential pair signal." *Id.* at 22-23.

The Court agrees with VIA and finds that "[data] differentiator" should be construed as a

"circuit that outputs a data differential pair." The specification describes a data differentiator as a circuit that receives serial data, and outputs a data differential pair. '187 Patent at 3:39-40 ("Data differentiator 232 receives serial data DT, and thereby outputs a data differential pair, DP and DN.").

The Court does not agree with Asus's position that the patentee acted as his own lexicographer with respect to "differentiator." As the Federal Circuit recently reiterated "[t]he standards for finding lexicography and disavowal are exacting. To act as a lexicographer, a patentee must clearly set forth a definition of the disputed claim term and clearly express an intent to redefine the term." *Luminara Worldwide, LLC v. Liown Elects Co. Ltd.*, 814 F.3d 1343, 1353 (Fed. Cir. 2016) (internal quotations and citations omitted). Here, the '187 Patent does not express a clear intent to redefine "differentiator." Asus even concedes in its briefing that the '187 Patent does not expressly define "differentiator." Opp. 22, ECF 126 ("The '187 patent does not include an express definition for what it refers as a 'differentiator.'").

Asus relies upon *Int'l Rectifier Corp. v. IXYS Corp.*, 361 F.3d 1363 (Fed. Cir. 2004) to argue that the patentee acted as his own lexicographer with respect to "differentiator." "differentiator." However, *Int'l Rectifier* was decided under the Federal Circuit's then-existing approach to claim construction outlined in *Texas Digital Sys., Inc. v. Telegenix, Inc.*, 308 F.3d 1193 (Fed. Cir. 2002). In *Int'l Rectifier*, the claim construction began with an examination of the dictionary. That approach to claim construction was superseded by the Federal Circtui's *Phillips*'s decision. *Phillips*, 145 F.3d at 1320 (*Texas Digital* "placed too much reliance on extrinsic sources such as dictionaries, treatises, and encyclopedias and too little on intrinsic sources, in particular the specification and prosecution history.").

Since VIA did not act as its own lexicographer, ASUS's proposed construction improperly imports limitations from examples or embodiments in the '187 Patent. Although the claims are read "in view of the specification, of which they are a part, [the Court does] not read limitations from the embodiments in the specification into the claims." *See Hil-Rom Servs., Inc. v. Stryker Corp.*, 755 F.3d 1367, 1372 (Fed. Cir. 2014). The specification expressly states that Figure 4, from which Asus draws its proposed construction, is a "description of the preferred but *non-*

limiting embodiment[]." '187 Patent at 2:30-35 (emphasis added). Accordingly, the Court construes "[data] differentiator" as a "circuit that outputs a data differential pair."

IV. ORDER

As set forth above, the Court construes the disputed terms as follows:

Claim Term	Court's Construction
"a parallel-to-serial unit which receives a parallel data to serialize the parallel data into a serial data and a delayed serial data"	function: "(which) receives a parallel data to serialize the parallel data into a serial data and a delayed serial data" corresponding structure: serializers 212, 214 and register 216 of FIG. 3A
"to serialize the/serializing a parallel data into a serial data and a delayed serial data"	"the act of converting two or more streams of parallel data into a single stream serial data where the individual bit values of the parallel data are output serially (one after another)"
"one serial bit time lag"	"delayed by the duration of one serial bit"
"differential pair"	"a pair of complementary signals used to transmit information"
"[data] differentiator"	"circuit that outputs a data differential pair"

The Court also adopts the following constructions that the parties agreed to in their joint claim construction and prehearing statement.

U.S. Patent No. 7,313,187	
Claim Term	**Court's Construction**
"positive…differential signal"	"the complement of the negative signal of the differential pair"
"negative…differential signal"	"the complement of the positive signal of the differential pair"

U.S. Patent No. 8,476,747	
Claim Term	**Court's Construction**
"lead(s)"	Plain and ordinary meaning
"leadframe"	Plain and ordinary meaning
"pair of differential signal leads"	Plain and ordinary meaning

IT IS SO ORDERED.

Dated: August 19, 2016

BETH LABSON FREEMAN
United States District Judge