United States District Court
Northern District of California

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

ALPHA AND OMEGA SEMICONDUCTOR LIMITED, et al.,

Plaintiffs,

v.

FORCE MOS TECHNOLOGY CO., LTD.,

Defendant.

Case No. 22-cv-05448-PCP

ORDER DENYING MOTION TO STRIKE

Dkt. No. 59

Defendant Force MOS Technology Co., Ltd. has moved to strike plaintiffs' patent infringement contentions, filed pursuant to Patent Local Rules 3-1 and 3-2. For the reasons set forth below, the Court upon review concludes that each of the infringement contentions at issue is sufficient to provide reasonable notice to Force MOS. The motion is therefore denied.

I. Background

This is a patent case involving metal oxide semiconductor field effect transistors, or MOSFETs. The parties have filed several rounds of pleadings. As the case now stands, seven patents are at issue. Force MOS claims that plaintiffs Alpha and Omega Semiconductor Limited and Alpha and Omega Semiconductor Inc. (AOS) have infringed three of its U.S. patents, numbered 7,629,634; 7,847,346; and 7,646,058. AOS, in turn, claims that Force MOS has infringed four of AOS's patents, numbers 8,067,304; 7,511,361; 7,781,265; and 8,928,079. The parties also variously claim invalidity and seek declaratory judgments of non-infringement.

Pursuant to Patent Local Rules 3-1 and 3-2, AOS served its "Disclosure of Asserted Patent Claims and Infringement Contentions" as to its '304, '361, and '265 patents on January 31, 2023, and served supplemental infringement contentions as to its '079 patent on April 14, 2023. Force MOS believes that some of AOS's infringement contentions are deficient. After the parties failed

to resolve this dispute on their own, Force MOS filed this motion. Force MOS asks the Court to strike AOS's infringement contentions as to several of the claims of AOS's '304 and '079 patents.

MOSFETs are semiconductor chips. The fabrication process begins with a wafer, a thin disc of semiconductive material that can be used to produce many individual chips. AOS's '304 patent involves a method for forming a layer of metal 3–6 microns thick on the top surface of a wafer that has built-in "alignment marks." Alignment marks are indentations at specified locations around the wafer which are used to line up a mask for a later step in the fabrication process. But adding a layer of metal on top of the wafer can degrade the sharpness of the alignment marks, which in turn makes alignment for the masking process less precise—a problem as manufacturers aim to make chips smaller and smaller. Using "hot" metal (400° C) to create this layer is beneficial in some ways because hot metal has good "step coverage," or in other words, is better than "cold" metal (300° ± 50° C) at filling in voids in the surface of the wafer. But this same property means that using hot metal can degrade the sharpness of the alignment marks. Figure 1D from the '304 patent shows a cross section of an alignment mark before the metal layer is added, and Figure 2B illustrates how the alignment mark can be degraded when a layer of metal is added:

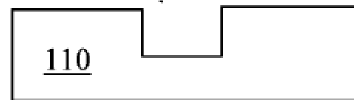


Fig. 1D

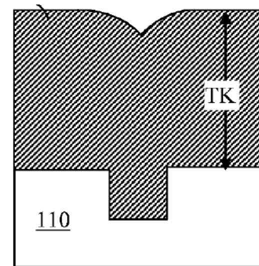
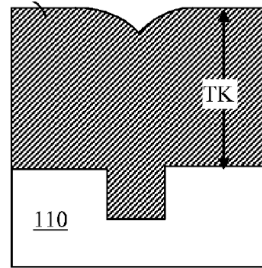


Fig. 2B

The gist of the '304 patent is that by adding two metallization layers—a thin hot one followed by a thicker cold one—instead of a single thick layer (as illustrated in Figure 2B), the beneficial properties of the hot layer's contact with the surface of the wafer can be taken advantage of while better preserving the sharpness of the alignment mark. Figure 3B illustrates the difference:



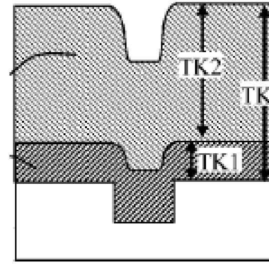


Fig. 2B **Fig. 3B**

There are some inherent tradeoffs between certain characteristics of MOSFETs, and depending on the intended application manufactures can seek to strike a different balance. One such characteristic is the resistance between the transistor's "source" and "drain" terminals when it is "on," or in other words, when a voltage is applied to the "gate" terminal. This resistance value is referred to as $R_{DS(on)}$ or the on-resistance. A MOSFET's on-resistance is typically proportional to the length of the channel between the source and drain terminals and inversely proportional to the concentration of individual cells in the chip. The MOSFET's gate capacitance is proportional to both channel length and cell concentration. If the goal is to minimize on-resistance, two options are to reduce channel length or increase cell concentration. But cell concentration is limited by the current state of manufacturing technology, and channel length is limited by what is known as the "punch-through" phenomenon. AOS's '079 patent outlines a MOSFET manufacturing process that aims to address some of these tradeoffs and reduce both the on-resistance and gate capacitance.

II. Legal Standard

Patent Local Rule 3-1 requires a party alleging patent infringement to serve a "Disclosure of Asserted Claims and Infringement Contentions." The infringement contentions must, for each claim allegedly infringed, identify "each accused apparatus, product, device, process, method, act, or other instrumentality." Next, for each accused instrumentality, the claimant must provide a "chart identifying specifically where and how each limitation of each asserted claim is found."

Rule 3-1 is essentially a discovery shortcut: It "takes the place of a series of interrogatories that defendants would likely have propounded had the patent local rules not provided for streamlined discovery." *Network Caching Tech. LLC v. Novell, Inc.*, No. 01-cv-02079-VRW, 2002 WL 32126128, at *4 (N.D. Cal. Aug. 13, 2002). "These rules require parties to crystallize

their theories of the case early in litigation," and they "provide structure to discovery" to enable efficient resolution of the dispute. *Creagri, Inc. v. Pinnaclife Inc., LLC*, No. 11-CV-06635-LHK-PSG, 2012 WL 5389775, at *2 (N.D. Cal. Nov. 2, 2012) (cleaned up). The rules do not "require the disclosure of specific evidence nor do they require a plaintiff to prove its infringement case." *Id.* Instead, "to the extent appropriate information is reasonably available," the rules require the plaintiff "to disclose the elements in each accused instrumentality that it contends practices each and every limitation of each asserted claim" *Id.* The minimum standard is that "the degree of specificity under Local Rule 3-1 must be sufficient to provide reasonable notice to the defendant why the plaintiff believes it has a reasonable chance of proving infringement," and the contentions "must map specific elements of Defendants' alleged infringing products onto the Plaintiff's claim construction." *Shared Memory Graphics LLC v. Apple, Inc.*, 812 F. Supp. 2d 1022, 1025 (N.D. Cal. 2010) (cleaned up).

"Where appropriate, courts treat a motion to strike as a motion to compel amendment to include additional information." *France Telecom, S.A. v. Marvell Semiconductor, Inc.*, No. 12-CV-04967-WHA-NC, 2013 WL 1878912, at *2 (N.D. Cal. May 3, 2013).

III. Analysis

Force MOS argues that several of AOS's infringement contentions are deficient. The contentions at issue are addressed in turn below. For the reasons set forth, the Court concludes that all of these contentions provide adequate notice and are sufficient under Patent Local Rule 3-1.

A. The '304 Patent

1. Claim 4

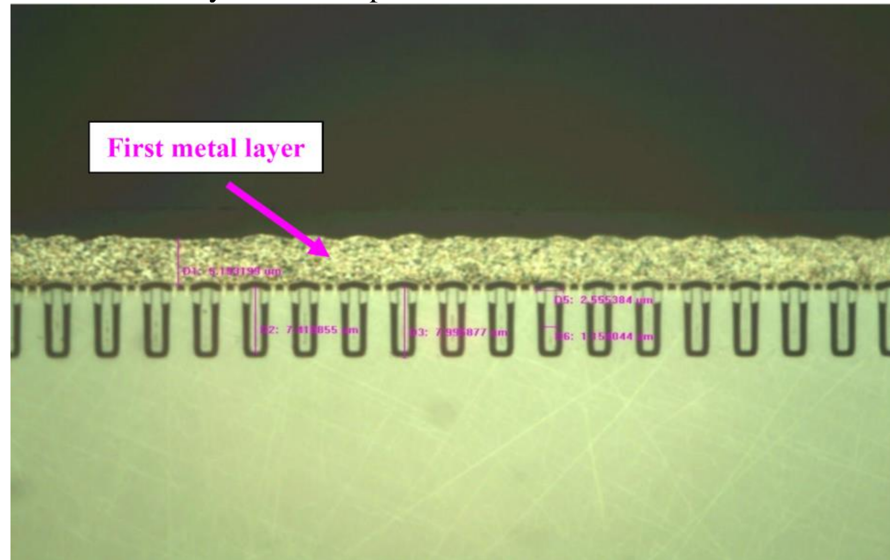
Claim 4 of the '304 patent states:

> The power semiconductor device of claim 1 wherein said first metal layer comprising a hot metallization layer in the bottom and a cold metallization layer on the top.

Dkt. No. 59-2, at 32. AOS provides the following infringement contention for this claim with respect to Force MOS's MEE7816AS-G device:

> The MEE7816AS-G is a power semiconductor device of claim 1. *See*

> claim 1 above.
>
> The MEE7816AS-G's first metal layer comprising a hot metallization layer in the bottom and a cold metallization layer on the top. *See, e.g.,*
>
> The cross-sectional image of the MEE7816AS-G below shows the first metal layer. On information and belief, the first metal layer comprises a hot metallization layer in the bottom and a cold metallization layer on the top.



Id. at 32–33.

Force MOS argues that this contention is deficient because AOS makes a "conclusory assertion that 'on information and belief' that [sic] this 'First metal layer' satisfies the hot metalization [sic] layer in the bottom and cold metallization layer on the top as additionally required of Claim 4" but fails to provide any "supporting commentary, analysis, images, additional evidence, or even mere identification to show how the first metal layer is [sic] comprises either a hot metalization layer or, a cold metalization, or and certainly not both simultaneously." Dkt. No. 59, at 10. Force MOS argues that AOS "merely provides improper 'information and belief' and an unhelpful image that does not even attempt to identify 'a hot metallization layer' nor 'a cold metallization layer,'" and "leaves Force MOS to guess where AOS contends the cold and hot metallization layers are." *Id.*

AOS counters that there is "nothing confusing" about its Claim 4 contentions and emphasizes that in addition to the image of the accused product, AOS has also included both a label and explanation. Dkt. No. 68, at 10.

This infringement contention is sufficient under Patent L.R. 3-1. AOS is not required to prove infringement at this stage, or to provide commentary, analysis, or evidence. AOS is simply required to provide reasonable notice to Force MOS as to why, based on the information available to AOS, it thinks it has reasonable chance of proving infringement. In context, AOS's assertion that the "first metal layer" identified in the accompanying image "comprises a hot metallization layer in the bottom and a cold metallization layer on the top" provides adequate notice. Force MOS is correct that AOS includes the phrase "on information and belief" in this contention, but AOS has gone beyond simply concluding based on information and belief that the accused product infringes the claim, or parroting the language of the claim without any further explanation or context. No great mental leap is required to deduce from the image which side of the identified first metal layer is the "top" and which is the "bottom," as Force MOS seems to fault AOS for failing to clarify. The Court will not strike this contention.

Force MOS argues that AOS's contentions for Force MOS's ME4435-G device, Dkt. No. 59-2, at 65, are essentially identical to its contentions for the MEE7816AS-G device. These contentions are sufficient for the same reasons.

2. Claim 5

Claim 5 states:

> The power semiconductor chip of claim 4 wherein said hot metallization layer has a thickness between 0.5-1 micron.

Dkt. No. 59-2, at 33. AOS provides the following infringement contention for this claim with respect to Force MOS's MEE7816AS-G device:

> The MEE7816AS-G is a power semiconductor device of claim 4. *See* claim 4 above.
>
> The MEE7816AS-G's hot metallization layer has a thickness between 0.5-1 micron.
>
> For example, on information and belief, the MEE7816AS-G's hot metallization layer has a thickness between 0.5-1 micron, as a result of Force MOS's MOSFET manufacturing processes.

Id. AOS's contentions for the Force MOS ME4435-G device are similar. *See id.* at 64.

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Force MOS argues that these contentions are deficient because they are "essentially identical" to the language of the claim, and AOS "does not even provide an image or any other evidentiary citation." Dkt. No. 59, at 11. In response, AOS emphasizes that it is not required to disclose specific evidence or prove its infringement case at this stage. Dkt. No. 68, at 11.

Force MOS is correct that courts in other cases have sometimes found infringement contentions that simply repeat claim language to be insufficient. But the ultimate inquiry is still whether the contentions provide reasonable notice of why a plaintiff thinks a defendant's products may infringe. Here, Claim 5 is extremely straightforward. All it adds to Claim 4 is the specific dimension of one element: the hot metallization layer. Indeed, given the simplicity of this claim, it is hard to imagine how infringement could be alleged without to some extent parroting the language or at least the essential structure of the claim. In addition, Claim 5 is tied to Claim 4, and AOS's infringement contentions for Claim 5 refer back to its contentions for Claim 4, including the image it included. Taken in context, AOS's contentions are clear enough to provide adequate notice. Requiring AOS to reinclude the image from its Claim 4 contention in its Claim 5 contention as a matter of box-checking would not be useful and would not further the purposes of Patent L.R. 3-1. These contentions suffice and will not be stricken.

3. Claim 7

Claim 7 states:

> The power semiconductor chip of claim 4 wherein a ratio of the cold metallization thickness to hot metallization thickness ranges from about 3:1 to about 7:1.

Dkt. No. 59-2, at 34. AOS provides the following infringement contention for this claim with respect to Force MOS's MEE7816AS-G device:

> The MEE7816AS-G is a power semiconductor device of claim 4. *See* claim 4 above.
>
> In the MEE7816AS-G, a ratio of the cold metallization thickness to hot metallization thickness ranges from about 3:1 to about 7:1.
>
> For example, on information and belief, the ratio of the MEE7816AS-G's cold metallization thickness to hot metallization thickness ranges

> from about 3:1 to about 7:1, as a result of Force MOS's MOSFET manufacturing processes.

Id. AOS's contentions for the Force MOS ME4435-G device are similar. *See id.* at 66.

As with Claim 5, although AOS's infringement contention does parallel the language of the claim, the simplicity of the claims makes this inevitable and the contention is sufficient to provide notice to Force MOS, especially since this claim is dependent. Force MOS faults AOS for failing to indicate "what aspect of the manufacturing process causes this limitation to be satisfied" or specifying "where or how AUS is measuring the thickness of the respective layers." Dkt. No. 59, at 12. That level of specificity is not required at this stage. AOS contends that the accused product has cold and hot metallization layers whose thicknesses satisfy the ratio set out in the claim. AOS does not need to know or specify how that ratio is manufactured in order to contend that it occurs. These contentions are also sufficient and will not be stricken.

4. Claim 10

Claim 10 states:

> The power semiconductor chip of claim 9 further comprising:
>
> 10[a]: a second metal layer overlaying the dielectric layer contacting the insulated gate through the gate contact openings, and
>
> 10[b]: said second metal layer further comprising a hot metallization layer at the bottom and a cold metallization layer on the top.

Dkt. No. 59-2, at 37. AOS provides the following infringement contentions for these claims with respect to Force MOS's MEE7816AS-G device:

> The MEE7816AS-G power semiconductor chip of claim 9. *See* claim 9.
>
> The MEE7816AS-G includes a second metal layer overlaying the dielectric layer contacting the insulated gate through the gate contact openings. *See* limitation 2[b].
>
> The MEE7816AS-G's second metal layer comprises a hot metallization layer at the bottom and a cold metallization layer on the top.
>
> For example, when manufacturing MOSFETs, it is common to use a substantially similar process to form both the first metal layer and the

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> second metal layer. On information and belief, this is true for the MEE7816AS-G. Thus, the analysis for the "first metal layer" for claim 4 also applies for this limitation. *See* claim 4.

Id. AOS's contentions for Force MOS's ME4435-G device are similar. *See id.* at 69–70.

Force MOS argues that this contention, which ties back to the contention for Claim 4, is deficient for similar reasons. Force MOS also faults AOS for basing this contention on its understanding of "common" practices without providing any "documentation or citation to evidence." Dkt. No. 59, at 13. As explained above, however, AOS's infringement contention for Claim 4 is sufficient under the Local Rules. This contention is as well. Documentation and evidence, while helpful if available, are not required.

5. Claim 11

Claim 11 states:

> The power semiconductor chip of claim 10 wherein said hot metallization layer has a thickness between 0.5-1 micron.

Dkt. No. 59-2, at 37. AOS provides the following infringement contention for this claim with respect to Force MOS's MEE7816AS-G device:

> The MEE7816AS-G is a power semiconductor device of claim 10. *See* claim 10 above.
>
> The MEE7816AS-G's hot metallization layer has a thickness between 0.5-1 micron.
>
> For example, when manufacturing MOSFETs, it is common to use a substantially similar process to form both the first metal layer and the second metal layer. On information and belief, this is true for the MEE7816AS-G. Thus, the analysis for the "hot metallization layer" for claim 5 also applies for this claim. *See* claim 5.

Id. AOS's contentions for the Force MOS ME4435-G device are similar. *See id.* at 70.

This claim largely parallels Claim 5 except that it applies to the hot metallization layer of the second metal layer rather than the first metal layer. AOS's Claim 11 infringement contentions are sufficient for the same reasons its Claim 5 contentions are.

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6. Claim 13

Claim 13 states:

> The power semiconductor chip of claim 10 wherein a ratio of the cold metallization thickness to hot metallization thickness ranges from about 3:1 to about 7:1.

Dkt. No. 59-2, at 38. AOS provides the following infringement contention for this claim with respect to Force MOS's MEE7816AS-G device:

> The MEE7816AS-G is a power semiconductor device of claim 10. *See* claim 10 above.
>
> In the MEE7816AS-G, a ratio of the cold metallization thickness to hot metallization thickness ranges from about 3:1 to about 7:1.
>
> For example, when manufacturing MOSFETs, it is common to use a substantially similar process to form both the first metal layer and the second metal layer. On information and belief, this is true for the MEE7816AS-G. Thus, the analysis for the "hot metallization layer" and the "cold metallization layer" for claim 7 also applies for this claim. *See* claim 7.

Id. AOS's contentions for the Force MOS ME4435-G device are similar. *See id.* at 70–71.

This claim largely parallels Claim 7. AOS's Claim 13 contentions are sufficient for the same reasons its Claim 7 contentions are.

7. Claim 14

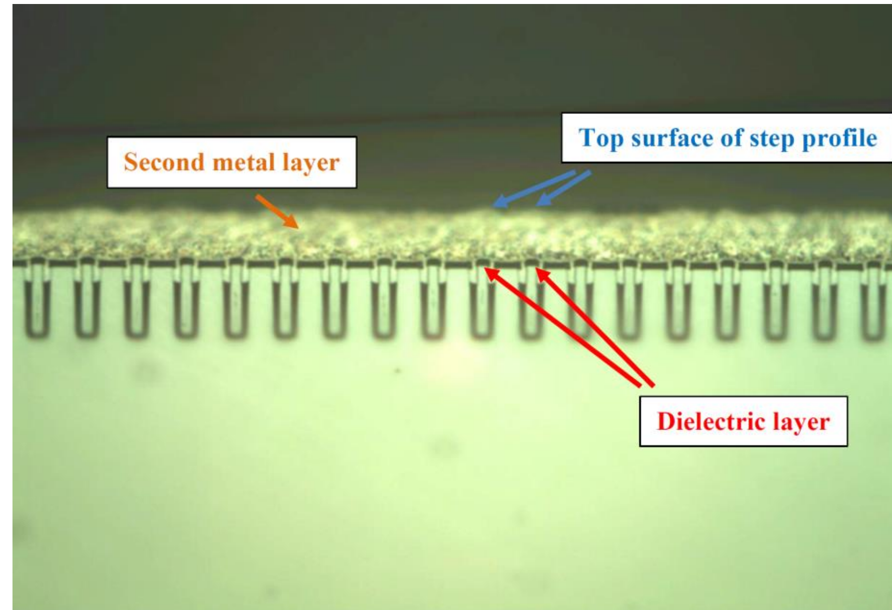
Claim 14 states:

> The power semiconductor chip of claim 10 wherein said second metal layer has a top surface of step profile substantially conforming to a topography of its underlying dielectric layer.

Dkt. No. 59-2, at 38. AOS provides the following infringement contention for this claim with respect to Force MOS's MEE7816AS-G device:

> The MEE7816AS-G is a power semiconductor device of claim 10. *See* claim 10 above.
>
> The MEE7816AS-G's second metal layer has a top surface of step

> profile substantially conforming to a topography of its underlying dielectric layer. *See, e.g.,*
>
> As shown in the optical microscopic image below, the MEE7816AS-G's second metal layer has a top surface of step profile substantially conforming to a topography of its underlying dielectric layer.



Id. at 38–39. AOS's contentions for Force MOS's ME4435-G device are similar. *See id.* at 71–72.

Force MOS argues that AOS's contentions for Claim 14 are deficient for the same reasons as its Claim 13 contentions. Force MOS faults AOS for basing its contentions on "common" techniques and asserting infringement based on "information and belief." Dkt. No. 59, at 15. AOS's contention for Claim 14 does not use these terms, however, as shown above. It is possible this argument may have been intended for another of AOS's contentions. Regardless, the Claim 14 contentions are sufficient.

B. The '079 Patent

1. Claims 8 and 18

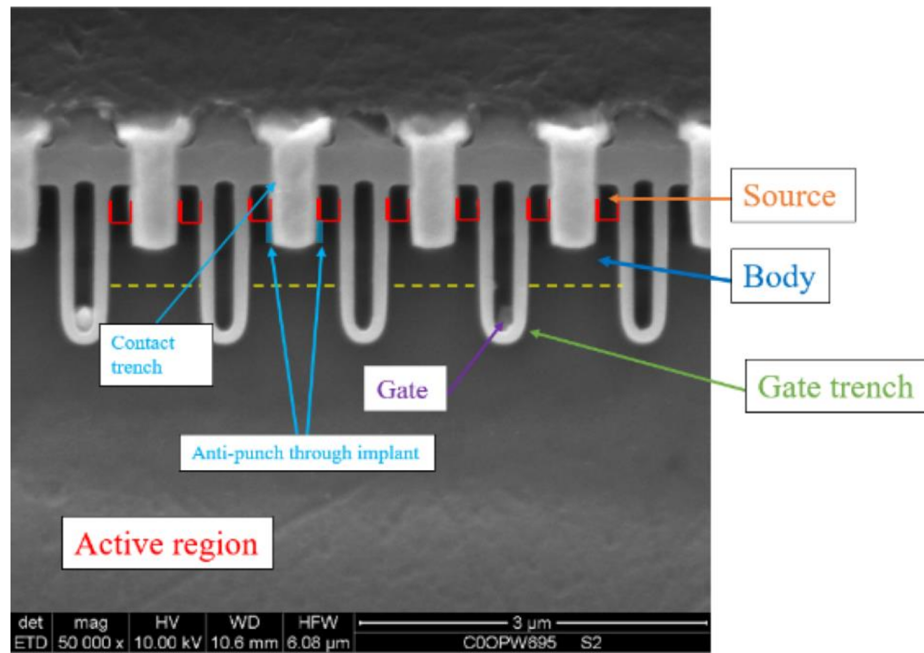
Claim 8 of the '079 patent states:

> The semiconductor device of claim 1, further comprising an anti-punch through implant disposed on a sidewall of the active region contact trench.

Dkt. No. 59-3, at 38–39. AOS provides the following infringement contention for this claim with

respect to Force MOS's ME2N70026D2KW device:

> The ME2N70026D2KW includes the semiconductor device of claim 1. *See* claim 1 above.
>
> The ME2N70026D2KW includes an anti-punch through implant disposed on a sidewall of the active region contact trench. *See, e.g.,*
>
> The following SEM image of ME2N70026D2KW shows the E2N70026D2KW active region contact trench. On information and belief, the ME2N70026D2KW has an anti-punch through implant disposed on a sidewall of the active region contact trench.



Id. at 38–39. AOS's contentions for Force MOS's ME4435 device are similar. *See id.* at 79–80.

According to Force MOS, AOS's contentions are insufficient because AOS simply points to the location of a sidewall on an image and asserts "on information and belief" that the accused product has an anti-punch through implant disposed on the sidewall. *See* Dkt. No. 59, at 16. Force MOS argues that the image does not actually show the anti-punch through implant, that the sides of the contact trench do not appear visually distinct from other areas of the contact trench in the image, and that Force MOS has no way of knowing what parts of its manufacturing process AOS contends generate those implants. *Id.* AOS counters that its contentions are clear, and that because Claim 8 is an apparatus claim, it does not need to identify the parts of Force MOS's manufacturing process that could generate such an implant.

AOS's Claim 8 contentions are adequate. The annotated image that AOS has provided is clear enough to provide reasonable notice. Even if the anti-punch through implants do not appear visually distinct in the image standing alone, AOS has supplemented the image by pointing out specifically where it believes the implants are located. That is clear enough. The case Force MOS relies on does not support its argument. In *Infineon Technologies AG v. Volterra Semiconductor Corp.*, the plaintiffs "reference[d] a birds-eye image" of an accused product asserted as "show[ing] a metal layer," but the Court concluded that the image did "not allow the viewer to discern whether [it] depicts one or multiple layers, let alone which specific layer(s) are shown," and that the "Defendant … is entitled to know which layer or layers allegedly infringe." No. 11-cv-06239-MMC-DMR, 2013 WL 322570, at *3 (N.D. Cal. Jan. 28, 2013). Here, even if the image alone might not be clear enough to enable Force MOS to discern which portions showed the alleged infringement, AOS has done exactly what *Infineon* suggests is required by clearly annotating and labeling the image. These contentions are sufficient and will not be stricken.

Force MOS argues that the same analysis applies to Claim 18 because AUS replies on its Claim 8 contentions. Because the Court concludes that the Claim 8 contentions are sufficient, the Claim 18 contentions are similarly acceptable.

2. Claims 9 and 19

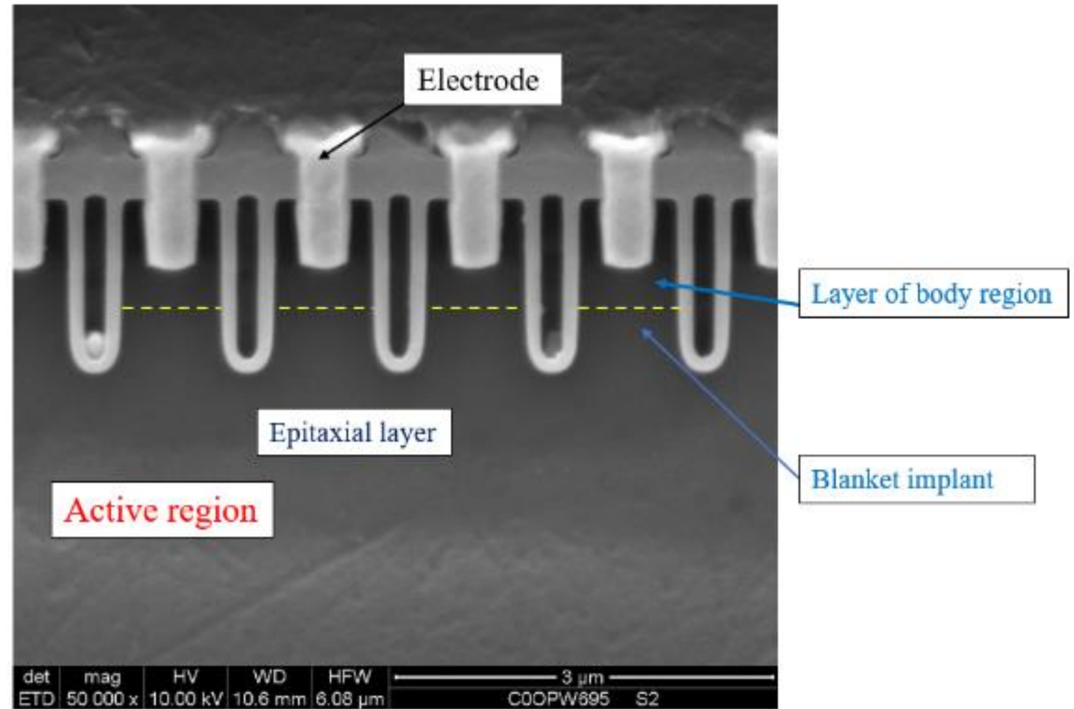
Claim 9 states:

> The semiconductor device of claim 1, further comprising a blanket implant deposited throughout the epitaxial layer, wherein the blanket implant has opposite polarity as the epitaxial layer.

Dkt. No. 59-3, at 39–40. AOS provides the following infringement contention for this claim with respect to Force MOS's ME2N70026D2KW device:

> The ME2N70026D2KW includes the semiconductor device of claim 1. *See* claim 1 above.
>
> The ME2N70026D2KW includes a blanket implant deposited throughout the epitaxial layer, wherein the blanket implant has opposite polarity as the epitaxial layer. *See, e.g.,*
>
> The following SEM image of ME2N70026D2KW shows the

> ME2N70026D2KW epitaxial layer. On information and belief, the ME2N70026D2KW has a blanket implant deposited throughout the epitaxial layer. On information and belief, the blanket implant has opposite polarity as the epitaxial layer.



Id. at 39–40. AOS's contentions for the Force MOS ME4435-G device are similar. *See id.* at 81.

Force MOS argues that AOS's contentions are "not based on an analysis of the Force MOS product," but rather merely an "information and belief" guess. Force MOS also complains that the arrow labeling the "blanket implant" does not point to any identifiable structure and the various regions in the image are "visually indistinct." Dkt. No. 59, at 18–19.

AOS's contentions are again sufficient. Here, as with Claim 8, the image alone might be insufficient for the reasons that Force MOS has pointed out: It is difficult to tell without more where the various alleged regions are delineated. But AOS has provided more, in the form of a dotted line showing where the blanket implant is asserted to be and labels indicating the regions on either side. This is clear enough in context to provide reasonable notice to Force MOS. Force MOS seems to want a better image that clearly depicts the various regions of its product. But that is the kind of evidentiary showing that is not required at this stage by Patent Rule 3-1. These contentions are adequate and will not be stricken.

As with Claim 18, AOS's contentions for Claim 19 refer back to Claim 9. The limitation added to Claim 13 by Claim 19 is similar to the limitation added to Claim 1 by Claim 9. The Claim 19 contentions are therefore acceptable for the same reasons the Claim 9 contentions are.

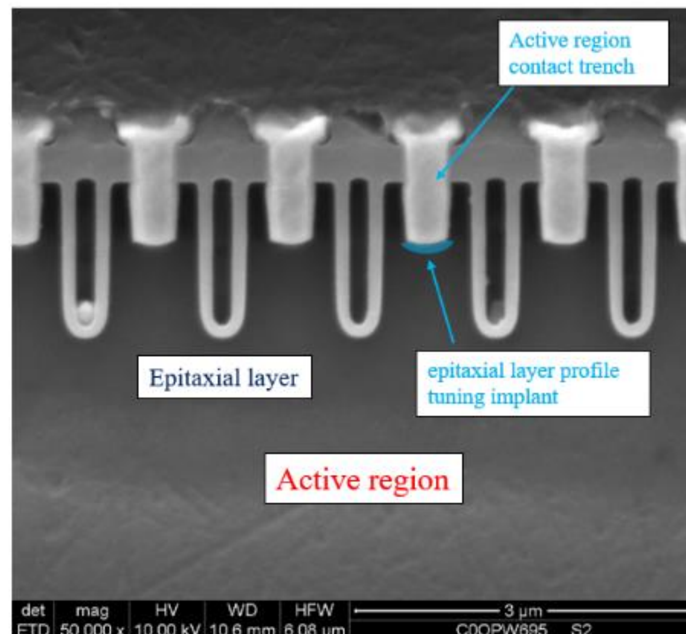
3. Claims 10 and 20

Claim 10 states:

> The semiconductor device of claim 1, further comprising an epitaxial layer profile tuning implant deposited under the active region contact trench.

Dkt. No. 59-3, at 40–41. AOS provides the following infringement contention for this claim with respect to the Force MOS ME2N70026D2KW device:

> The ME2N70026D2KW includes the semiconductor device of claim 1. *See* claim 1 above.
>
> The ME2N70026D2KW includes an epitaxial layer profile tuning implant deposited under the active region contact trench. *See, e.g.,*
>
> The following SEM image of ME2N70026D2KW shows the E2N70026D2KW active region contact trench and epitaxial layer. On information and belief, the ME2N70026D2KW has an epitaxial layer profile tuning implant deposited under the active region contact trench.



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Id. AOS's contentions for Force MOS's ME4435-G device are similar. *See id.* at 81–82.

Force MOS again faults AOS for including assertions on "information and belief" without additional support, arguing that AOS merely "guesses" that the indicated region includes the epitaxial layer profiling tuning implant even though the region is not visually distinct in the image. But again, AOS has done all that is required here. Whether AOS is correct in its belief is a question for later in the case. But *what* AOS believes with respect to infringement of this claim is clear enough to provide notice to Force MOS. These contentions will not be stricken.

AOS's contentions for Claim 20 refer back to Claim 10. And the limitation added to Claim 13 by Claim 20 is similar to the limitation added to Claim 1 by Claim 10. The Claim 20 contentions are acceptable for the same reasons the Claim 10 contentions are.

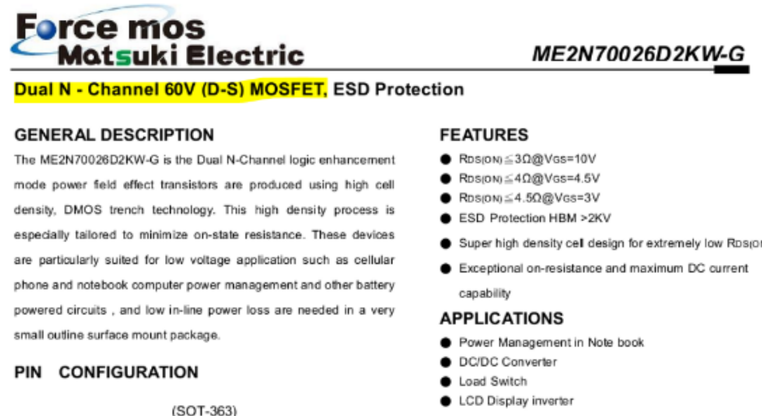
4. Claims 12 and 22

Claim 12 states:

> The semiconductor device of claim 1, wherein the body and the semiconductor substrate have opposite polarities.

Dkt. No. 59-3, at 42. AOS provides the following infringement contention for this claim with respect to the Force MOS ME2N70026D2KW device:

> The ME2N70026D2KW includes the semiconductor device of claim 1. *See* claim 1 above.
>
> The ME2N70026D2KW includes the body and the semiconductor substrate have opposite polarities. *See, e.g.,*
>
> As shown in the datasheet below, ME2N70026D2KW is a dual N-Channel MOSFET.



Force mos
Matsuki Electric

ME2N70026D2KW-G

Dual N - Channel 60V (D-S) MOSFET, ESD Protection

GENERAL DESCRIPTION

The ME2N70026D2KW-G is the Dual N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits , and low in-line power loss are needed in a very small outline surface mount package.

PIN CONFIGURATION

(SOT-363)

FEATURES

- $R_{DS(ON)} \leq 3\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 4\Omega @ V_{GS}=4.5V$
- $R_{DS(ON)} \leq 4.5\Omega @ V_{GS}=3V$
- ESD Protection HBM >2KV
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

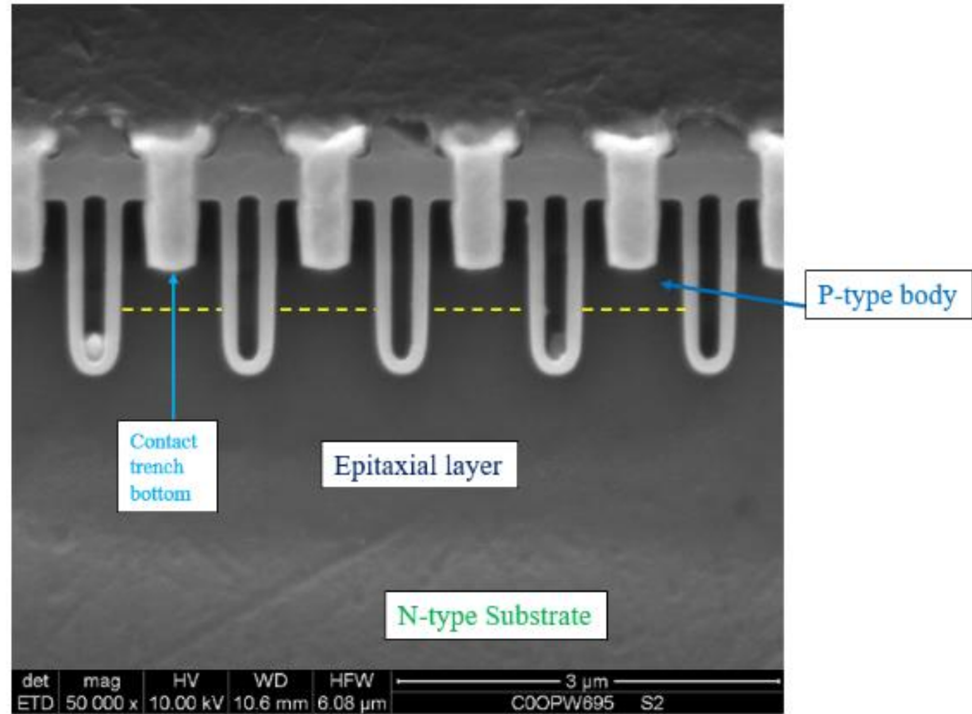
APPLICATIONS

- Power Management in Note book
- DC/DC Converter
- Load Switch
- LCD Display inverter

Ex. GG to AOS's Second Amended Complaint.

On information and belief, ME2N70026D2KW's semiconductor substrate is N-type and its body is P-type.

The following SEM image of ME2N70026D2KW shows the body and the semiconductor substrate. On information and belief, the semiconductor substrate and body have opposite polarities.



Id. at 42–44. AOS's contentions for Force MOS's ME4435-G device are similar. *See id.* at 83–85.

Force MOS again faults AOS for asserting the polarities of the P-type body and N-type substrate on "information and belief." But here, as before, AOS's assertions are more than clear enough to explain its infringement contentions and provide notice to Force MOS. No further "supporting discussion or analysis" is required to support AOS's contentions at this stage. *See* Dkt. No. 59, at 23. These contentions are sufficient and will not be stricken.

AOS's contentions for Claim 22 refer back to Claim 12. And the limitation added to Claim 13 by Claim 22 is similar to the limitation added to Claim 1 by Claim 12. The Claim 22 contentions are acceptable for the same reasons the Claim 12 contentions are.

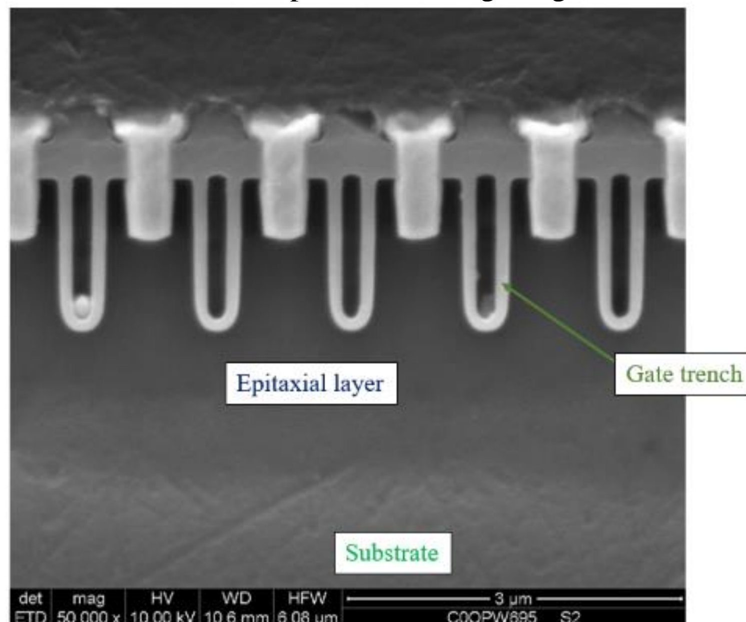
5. Claim 21

Claim 21 states:

> The method of claim 13, further comprising: forming a hard mask on the substrate prior to forming the gate trench;
>
> removing a hard mask to leave a gate structure that extends above the body top surface.

Dkt. No. 59-3, at 48–49. AOS provides the following infringement contention for this claim with respect to the Force MOS ME2N70026D2KW device:

> The ME2N70026D2KW is manufactured using the method of claim 3, further comprising forming a hard mask on the substrate prior to forming the gate trench. *See* claim 13 above.
>
> *See, e.g.*,
>
> The following SEM image of ME2N70026D2KW shows that ME2N70026D2KW has a gate trench and substrate. On information and belief, the ME2N70026D2KW is manufactured by forming a hard mask on the substrate prior to forming the gate trench.



Id. at 42–44. AOS's contentions for Force MOS's ME4435-G device are similar. *See id.* at 91–92.

Force MOS argues that AOS does not provide adequate support for its contention that the accused products are manufactured by forming a hard mask on the substrate prior to forming the gate trench. Force MOS also argues that the included image does not disclose the relevant steps

and structures of its manufacturing process.

As AOS points out, this contention is distinct from all of the others at issue in this motion, because it involves a step in the production process of the device rather than an aspect of the final product. As a result, the "precise masking information is solely in the possession of Force MOS." Dkt. No. 68, at 13. AOS argues that it has supplied all of the information it has at this point, and that this suffices under the standard set out in *Creagri* that disclosures are only required "to the extent appropriate information is reasonably available." Dkt. No. 68, at 13 (citing *Creagri,* 2012 WL 5389775, at *3); *see also France Telecom,* 2013 WL 1878912, at *4 (ruling that plaintiff "must identify how … products infringe with as much specificity as possible *with the information currently available to it*" (cleaned up)). Force MOS asserts that its request to strike this contention is consistent with *France Telecom* because AOS has allegedly provided "no substantive disclosure." Dkt. No. 69, at 15. But Force MOS does not suggest that there is any other information that is (or should be) currently available to AOS about Force MOS's manufacturing processes on which AOS could base its contentions.

AOS's contention is clearly insufficient to establish that Force MOS's manufacturing process actually does infringe. But that is not required in an infringement contention. AOS has provided adequate notice of its theory of infringement, and it is hard to see what further detail it could have provided at this stage in the litigation about Force MOS's proprietary processes. These contentions are sufficient and may remain.

IV. Conclusion

For the reasons set forth above, Force MOS's motion to strike is denied.

IT IS SO ORDERED.

Dated: December 13, 2023

P. Casey Pitts
United States District Judge

United States District Court
Northern District of California