Nokia Corporation v. Apple Inc.
Doc. 408 Att. 1

EXHIBIT 1

Dockets.Justia.com

UNITED STATES DISTRICT COURT

for the

Northern District of California

Nokia Corporation
Plaintiff
v.
Apple Inc.
Defendant

Civil Action No. 1:09-cv-00791-GMS

(If the action is pending in another district, state where: District of Delaware)

SUBPOENA TO TESTIFY AT A DEPOSITION IN A CIVIL ACTION

To: ARM Inc.
150 Rose Orchard Way, San Jose, CA 95134-1358

☑ *Testimony:* **YOU ARE COMMANDED** to appear at the time, date, and place set forth below to testify at a deposition to be taken in this civil action. If you are an organization that is *not* a party in this case, you must designate one or more officers, directors, or managing agents, or designate other persons who consent to testify on your behalf about the following matters, or those set forth in an attachment:

See Attachment B for topics.

Place:	Date and Time:
Alston & Bird LLP, 275 Middlefield Rd, Suite 150, Menlo Park, CA 94025-4004	06/17/2011 9:00 am

The deposition will be recorded by this method: court reporter and videographer

☑ *Production:* You, or your representatives, must also bring with you to the deposition the following documents, electronically stored information, or objects, and permit their inspection, copying, testing, or sampling of the material:

See Attachment A for document requests. Please mail these by June 10, 2011 to the attention of Matthew Urbanawiz, Alston & Bird LLP, One Atlantic Center, 1201 West Peachtree Street, Atlanta, GA 30309-3424.

The provisions of Fed. R. Civ. P. 45(c), relating to your protection as a person subject to a subpoena, and Rule 45 (d) and (e), relating to your duty to respond to this subpoena and the potential consequences of not doing so, are attached.

Date: 05/27/2011

CLERK OF COURT

OR

Signature of Clerk or Deputy Clerk

/s/ Matthew Urbanawiz
Attorney's signature

The name, address, e-mail, and telephone number of the attorney representing *(name of party)* Nokia Corporation and Nokia Inc. , who issues or requests this subpoena, are:

Matthew Urbanawiz, Alston & Bird LLP, One Atlantic Center, 1201 West Peachtree St., Atlanta, GA 30309-3424, matt.urbanawiz@alston.com, 404-881-7000

Civil Action No. 1:09-cv-00791-GMS

PROOF OF SERVICE

(This section should not be filed with the court unless required by Fed. R. Civ. P. 45.)

This subpoena for *(name of individual and title, if any)* _____

was received by me on *(date)* _____ .

❒ I served the subpoena by delivering a copy to the named individual as follows: _____

_____

_____ on *(date)* _____ ; or

❒ I returned the subpoena unexecuted because: _____

_____ .

Unless the subpoena was issued on behalf of the United States, or one of its officers or agents, I have also tendered to the witness fees for one day's attendance, and the mileage allowed by law, in the amount of $ _____ .

My fees are $ _____ for travel and $ _____ for services, for a total of $ 0.00 .

I declare under penalty of perjury that this information is true.

Date: _____ _____

Server's signature

_____

Printed name and title

_____

Server's address

Additional information regarding attempted service, etc:

Federal Rule of Civil Procedure 45 (c), (d), and (e) (Effective 12/1/07)

(c) Protecting a Person Subject to a Subpoena.

(1) ***Avoiding Undue Burden or Expense; Sanctions.*** A party or attorney responsible for issuing and serving a subpoena must take reasonable steps to avoid imposing undue burden or expense on a person subject to the subpoena. The issuing court must enforce this duty and impose an appropriate sanction — which may include lost earnings and reasonable attorney's fees — on a party or attorney who fails to comply.

(2) ***Command to Produce Materials or Permit Inspection.***

(A) *Appearance Not Required.* A person commanded to produce documents, electronically stored information, or tangible things, or to permit the inspection of premises, need not appear in person at the place of production or inspection unless also commanded to appear for a deposition, hearing, or trial.

(B) *Objections.* A person commanded to produce documents or tangible things or to permit inspection may serve on the party or attorney designated in the subpoena a written objection to inspecting, copying, testing or sampling any or all of the materials or to inspecting the premises — or to producing electronically stored information in the form or forms requested. The objection must be served before the earlier of the time specified for compliance or 14 days after the subpoena is served. If an objection is made, the following rules apply:

(i) At any time, on notice to the commanded person, the serving party may move the issuing court for an order compelling production or inspection.

(ii) These acts may be required only as directed in the order, and the order must protect a person who is neither a party nor a party's officer from significant expense resulting from compliance.

(3) ***Quashing or Modifying a Subpoena.***

(A) *When Required.* On timely motion, the issuing court must quash or modify a subpoena that:

(i) fails to allow a reasonable time to comply;

(ii) requires a person who is neither a party nor a party's officer to travel more than 100 miles from where that person resides, is employed, or regularly transacts business in person — except that, subject to Rule 45(c)(3)(B)(iii), the person may be commanded to attend a trial by traveling from any such place within the state where the trial is held;

(iii) requires disclosure of privileged or other protected matter, if no exception or waiver applies; or

(iv) subjects a person to undue burden.

(B) *When Permitted.* To protect a person subject to or affected by a subpoena, the issuing court may, on motion, quash or modify the subpoena if it requires:

(i) disclosing a trade secret or other confidential research, development, or commercial information;

(ii) disclosing an unretained expert's opinion or information that does not describe specific occurrences in dispute and results from the expert's study that was not requested by a party; or

(iii) a person who is neither a party nor a party's officer to incur substantial expense to travel more than 100 miles to attend trial.

(C) *Specifying Conditions as an Alternative.* In the circumstances described in Rule 45(c)(3)(B), the court may, instead of quashing or modifying a subpoena, order appearance or production under specified conditions if the serving party:

(i) shows a substantial need for the testimony or material that cannot be otherwise met without undue hardship; and

(ii) ensures that the subpoenaed person will be reasonably compensated.

(d) Duties in Responding to a Subpoena.

(1) ***Producing Documents or Electronically Stored Information.*** These procedures apply to producing documents or electronically stored information:

(A) *Documents.* A person responding to a subpoena to produce documents must produce them as they are kept in the ordinary course of business or must organize and label them to correspond to the categories in the demand.

(B) *Form for Producing Electronically Stored Information Not Specified.* If a subpoena does not specify a form for producing electronically stored information, the person responding must produce it in a form or forms in which it is ordinarily maintained or in a reasonably usable form or forms.

(C) *Electronically Stored Information Produced in Only One Form.* The person responding need not produce the same electronically stored information in more than one form.

(D) *Inaccessible Electronically Stored Information.* The person responding need not provide discovery of electronically stored information from sources that the person identifies as not reasonably accessible because of undue burden or cost. On motion to compel discovery or for a protective order, the person responding must show that the information is not reasonably accessible because of undue burden or cost. If that showing is made, the court may nonetheless order discovery from such sources if the requesting party shows good cause, considering the limitations of Rule 26(b)(2)(C). The court may specify conditions for the discovery.

(2) ***Claiming Privilege or Protection.***

(A) *Information Withheld.* A person withholding subpoenaed information under a claim that it is privileged or subject to protection as trial-preparation material must:

(i) expressly make the claim; and

(ii) describe the nature of the withheld documents, communications, or tangible things in a manner that, without revealing information itself privileged or protected, will enable the parties to assess the claim.

(B) *Information Produced.* If information produced in response to a subpoena is subject to a claim of privilege or of protection as trial-preparation material, the person making the claim may notify any party that received the information of the claim and the basis for it. After being notified, a party must promptly return, sequester, or destroy the specified information and any copies it has; must not use or disclose the information until the claim is resolved; must take reasonable steps to retrieve the information if the party disclosed it before being notified; and may promptly present the information to the court under seal for a determination of the claim. The person who produced the information must preserve the information until the claim is resolved.

(e) Contempt. The issuing court may hold in contempt a person who, having been served, fails without adequate excuse to obey the subpoena. A nonparty's failure to obey must be excused if the subpoena purports to require the nonparty to attend or produce at a place outside the limits of Rule 45(c)(3)(A)(ii).

Attachment A

ATTACHMENT "A" TO SUBPOENA

DEFINITIONS

A. "ARM" means ARM Inc., and any of its present or former affiliates, predecessors, successors, subsidiaries (whether owned directly or indirectly), assigns, divisions and operating units thereof, employees, agents, representatives, directors, officers, and entities under common control with ARM Inc..

B. "Nokia" means Nokia Corporation and Nokia Inc., including their predecessors, successors, parents, subsidiaries (whether owned directly or indirectly), affiliates, divisions and operating units thereof, agents and entities under common control with them.

C. "Apple" means Apple Inc., including its predecessors, successors, parents, subsidiaries (whether owned directly or indirectly), affiliates, divisions and operating units thereof, agents and entities under common control with it.

D. "Including" or any variant thereof means "including without limitation."

E. "And" and "or" shall mean "and/or," and shall be construed both conjunctively as well as disjunctively in order to maximize their scope.

F. "Any" and "all" mean "any and all."

G. "Each" and "every" mean "each and every."

H. "You," "your" or "yours" shall mean ARM, as defined herein.

I. "Thing(s)" has the broadest meaning allowable under Federal Rule of Civil Procedure 34 and includes any tangible object other than a document and, without limitation, objects of every kind and nature, as well as prototypes, models, or physical specimens thereof.

J. "Document" has the broadest meaning allowable under Federal Rules of Civil Procedure 34, and includes, without limitation, any thing or any written or graphic matter or any medium of any type or description upon which intelligence or information is recorded, or from which intelligence or information can be perceived, including computer, electronic, magnetic and optical media of all kinds, which is or has been in your possession, custody or control, or of which you have knowledge, including the original and any non-identical copy (whether different from the original because of notes made on said copy or otherwise) of any advertising literature; agreement; bank record or statement; blueprint; book; book of account; booklet; brochure; calendar; chart; circuit diagram; circular; coding form; communication (intra- or inter-company); components listing; computer data; computer printout; computer software and supporting indices; data; documentation; flow charts; comments; object code; source code and computer programs; contract; copy; correspondence; data base; design document; diary; die; display; draft of any document; drawing; electronic mail (e-mail); engineering change order; engineering specification; film; film transparency; flyer; forecast; graph; index; instruction; instruction manual or sheet; internet pages; invoice; job requisition; letter; license; log; machine readable form; manual; manufacturing data; manufacturing drawing; map; marketing plan; mask; memoranda; minutes; model; newspaper or other clippings; notes; notebook; opinion; packing checklist; packing list; pamphlet; paper; periodical or other publications; photograph; physical object; press release; price list; print; printed circuit board; product brochure; product specification; promotional literature; prototype; receipt; record; recorded read-only memory (ROM); recording; report; sales data; schematic; sketch; solicitation; statement; statistical compilation;

stenographic note; study; summary (including any memoranda, minutes, notes, records or summary of any (a) telephone or intercom conversation or message, (b) conversation or interview, or (c) meeting or conference); technical, service or operational manual; technical specification; telegram; telephone log; timing diagram; travel or expense records; video recording; videotape; voice recording; voucher; worksheet or work paper; and/or any other documentary material of any nature.

K. "Technical Reference Manual" shall mean all documents that refer or relate to a description of a product's technical specifications, features, design, components, troubleshooting, setup, operation, use, and/or general technical maintenance.

L. "Person" or "persons" shall mean an individual, corporation, proprietorship, partnership, association, or any other entity.

M. "Concerning" means concerning, regarding, describing, comprising, referring to, related to, supporting, favoring, opposing, bolstering, detracting from, located in, considered in connection with, bearing on, evidencing, indicating, reporting on, recording, alluding to, responding to, connected with, commenting on, in respect of, about, in relation to, discussing, showing, describing, reflecting, analyzing constituting, and being.

N. "Entity" means any natural person, corporation, partnership, sole proprietorship, firm, board, joint venture, association, agency, authority, commission or other business entity or juristic person.

O. "Communication" means any contact between two or more entities by which any information or knowledge is transmitted or conveyed or attempted to be transmitted or conveyed, including written contact including letters, memoranda, telegrams,

telefaxes, telecopies, telexes or e-mails, text messages and oral contact including face-to-face meetings, telephone conversations, voicemails, answering machine messages and telephonic notes.

P. "Relating to" or "related to" when referring to any given subject matter shall mean, without limitation, any document that constitutes, comprises, involves, contains, embodies, reflects, identifies, states, refers directly or indirectly to, or is in any way relevant to the particular subject matter identified.

Q. The term "identify" when used in conjunction with a person means to provide, to the extent known, the person's full name, present or last known address, and telephone number, and when referring to a natural person, additionally, the present or last known place of employment and, when referring to your current or former director, officer, manager or other employee, additionally the title(s) or position(s) held by such person, the time periods during which such person held such position(s), and a description of the responsibilities of such person to those position(s).

R. The term "identify" when used in conjunction with a document or other thing means to specify the document or thing in sufficient detail to permit Nokia to locate the document or thing.

INSTRUCTIONS

1. You are to search all documents within your possession, custody, or control, wherever located, including but not limited to any documents placed in storage facilities or in the possession of any employee, agent, representative, attorney, investigator, or other person acting or purporting to act on your behalf (whether located at his/her residence or place of business), in order to fully respond to the requests herein.

2. You are to produce documents from any single file in the same order as they were found in such file, including any labels, files, folders and/or containers in which such documents are located in or associated with. If copies of documents are produced in lieu of the originals, such copies should be legible and bound or stapled in the same manner as the original.

3. If you do not produce each document or thing requested herein as they are kept in the usual course of business, you must organize and label the documents or things produced to correspond with the particular document request to which the document or thing is responsive.

4. You are to produce all documents which are responsive in whole or in part to any of the requests herein in full, without abridgement, abbreviation, or expurgation of any sort, and regardless of whether you deem such documents to be irrelevant to the issues in the investigation for which such documents are being sought. If any such documents cannot be produced in full, produce the document to the extent possible and indicate in your written response what portion of the document is not produced and why it could not be produced.

5. You are required to produce not only the original or an exact copy of the original of all documents or things responsive to any of the requests herein, but also all copies of such documents or things which bear any notes or markings not found on the originals and all preliminary, intermediate, final, and revised drafts or embodiments of such documents or things. You are also required to produce all versions of the foregoing documents stored by a computer internally, on disk, on CD-ROM, or on tape.

6. You are to produce any purportedly privileged document containing non-privileged matter, with the purportedly privileged portion excised or redacted.

7. If any of the documents requested herein are no longer in your possession, custody, or control, you are requested to identify each such requested document by date, type of document, person(s) from whom sent, person(s) to whom sent, and person(s) receiving copies, and to provide a summary of its pertinent contents.

8. If any document responsive to these requests has been destroyed, describe the content of such document, the location of any copies of such document, the date of such destruction, and the name of the person who ordered or authorized such destruction.

9. Electronic and computerized materials must be produced in an intelligible format or together with a description of the system from which it was derived sufficient to permit tendering of the material intelligible.

10. If production of any document listed and described herein is withheld on the basis of a claim of privilege, each withheld document shall be separately identified in a

privileged document list. The privileged document list must identify each document separately, specifying for each document at least: (1) the date; (2) author(s)/sender(s); (3) recipient(s), including copy recipients; and (4) general subject matter of the document. The sender(s) and recipient(s) shall be identified by position and entity (corporation or firm, etc.) with which they are employed or associated. If the sender or the recipient is an attorney or a foreign patent agent, he or she shall be so identified. The type of privilege claimed must also be stated, together with a certification that all elements of the claimed privilege have been met and have not been waived with respect to each document.

DOCUMENT REQUESTS

REQUEST FOR PRODUCTION NO. 1:

The first release of the Technical Reference Manual for the ARM1020

REQUEST FOR PRODUCTION NO. 2:

Documents regarding the power management features of the Intel StrongARM SA-1100 and SA-1110.

REQUEST FOR PRODUCTION NO. 3:

Documents reflecting communications between ARM and any third-party, including Apple, regarding proposed or actual power managements features of the ARM10 or ARM11 core, including dormant mode, prior to April 29, 2002.

REQUEST FOR PRODUCTION NO. 4:

Documents reflecting communications between ARM and any third-party, including Apple, regarding proposed or actual power managements features later incorporated into the ARM10 or ARM11 core, including dormant mode, prior to April 29, 2002.

REQUEST FOR PRODUCTION NO. 5:

Documents reflecting communications between ARM and any third party, including Apple, regarding the dormant mode of any ARM-based core prior to April 29, 2002

REQUEST FOR PRODUCTION NO. 6:

Documents disclosed publicly by ARM prior to April 29, 2002 describing any ARM core with a dormant power mode.

REQUEST FOR PRODUCTION NO. 7:

Documents disclosed publicly by ARM prior to April 29, 2002 describing ways to

reduce leakage power losses, including presentations by ARM at industry conferences such as the International Solid-State Circuits Conferences or Hot Chips Symposium on High Performance Chips.

REQUEST FOR PRODUCTION NO. 8:

Documents sufficient to identify the first ARM core supporting dormant mode.

REQUEST FOR PRODUCTION NO. 9:

Prior art to U.S. Patent 7,383,453

Attachment B

ATTACHMENT "B" TO SUBPOENA

DEFINITIONS

The definitions set forth in Attachment A are incorporated by reference.

TOPICS

You are required to provide one or more individuals who are knowledgeable and competent to provide testimony about the following topics:

1. ARM's policies and practices involving the documents produced in response to Attachment A, including, but not limited to:

   a. The authenticity of the documents produced in response to Attachment A.

   b. Whether the documents produced in response to Attachment A are true and correct copies of the originals.

   c. Whether the documents produced in response to Attachment A are what they purport to be.

   d. Whether the documents produced in response to Attachment A were created by the people listed as the author, and, if no author is listed, who the author is.

   e. Whether the documents produced in response to Attachment A were created in the normal course of business and/or a regularly conducted business activity.

   f. Whether the creation of the documents produced in response to Attachment A was a regular part of the business activity.

   g. The dates on or about which the documents produced in response

to Attachment A were created.

h. The reasons for creating the documents produced in response to Attachment A.

i. Whether the documents produced in response to Attachment A were created by or based on information from people with knowledge of the activity recorded.

j. Whether the documents produced in response to Attachment A are the types of documents that are normally relied upon as a record of the activity recorded.

k. The subject matter of any of the documents produced in response to Attachment A.

2. The history, design, operation, and public disclosure of the power management features of the ARM1020 core, including public disclosures prior to April 29, 2002.

3. The power management features of the Intel StrongARM SA-1100 and SA-1110.

4. The authenticity and public disclosure of Exh. 1, a HOT CHIPS 2001 presentation regarding the ARM10 core.

5. The authenticity and public disclosure of Exh. 2, a 2001 ICCSS presentation regarding power management.

6. Communications between ARM and any third-party, including Apple, regarding proposed or actual power managements features of the ARM10 or ARM11 core prior to April 29, 2002.

7. Communications between ARM and any third party, including Apple, regarding the dormant mode of any ARM core prior to April 29, 2002

8. ARM public disclosure, prior to April 29, 2002, describing ways to reduce leakage power losses, including presentations by ARM at industry conferences such as the International Solid-State Circuits Conferences or Hot Chips Symposium on High Performance Chips.

9. Identification of ARM cores implementing or supporting a dormant power mode prior to April 29, 2002.

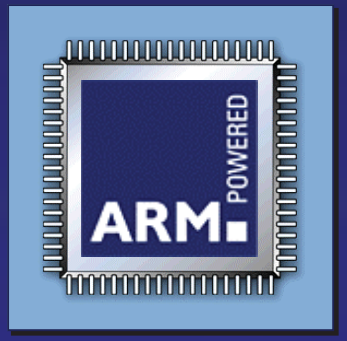
10. The history, design operation, and public disclosure of the power management features of ARM cores identified in response to Topic 9, including (i) the nature of different power modes, (ii) the conditions and events that cause entry into or exit from a different power modes.

11. Prior art to U.S. Patent 7,383,453

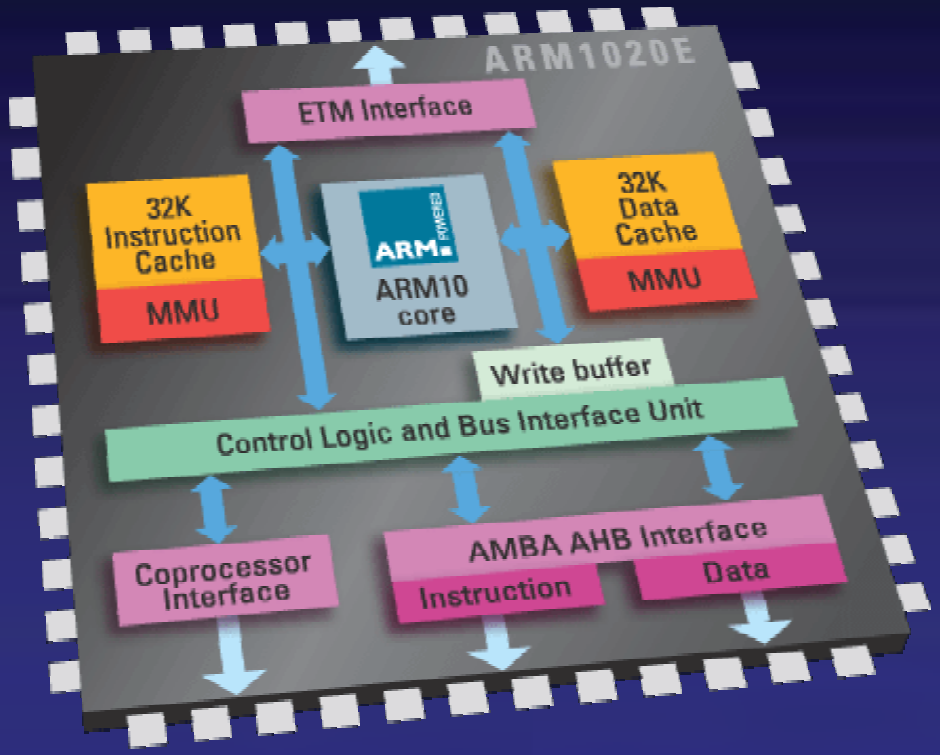
EXHIBIT 1

The ARM10 Family of Advanced Microprocessor Cores

Stephen Hill
ARM Austin Design Center



Agenda

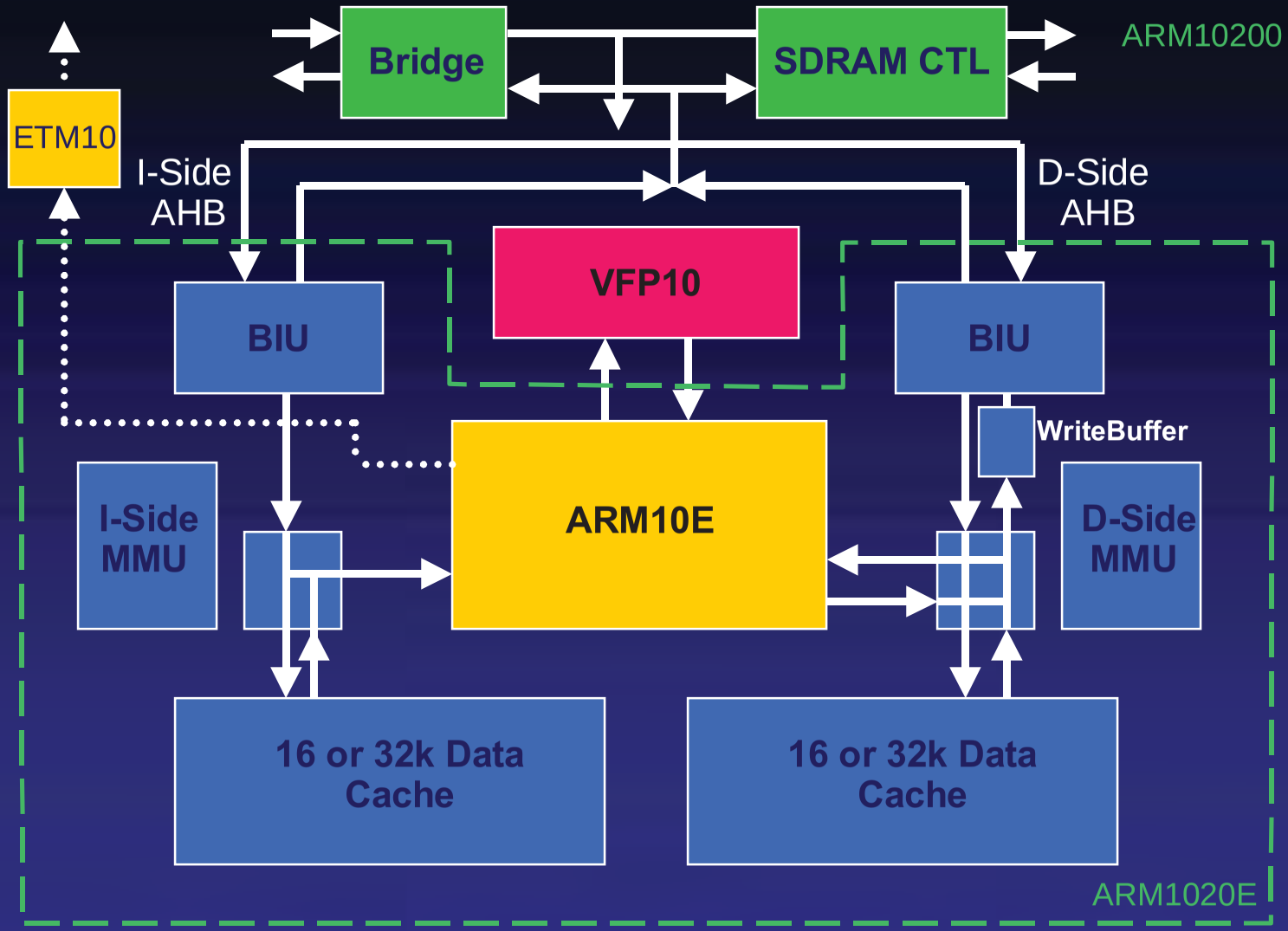


- Design overview
- Microarchitecture
  - ARM10
    - Memory System
    - Interrupt response
3. Power
   - Dynamic power
   - Power down modes
4. VFP10
- ETM10
- Summary

ARM1020E Overview

- Max frequency: 400MHz
  - 0.9*V*, worst case
  - TSMC 0.13um LV
- MIPS/MHz: 1.25
  - 500 MIPS @ 400MHz
  - Dhrystone 2.1
- Active power consumption: 0.51mA/MIPS
  - Room Temp / Typical / 1.1V
  - Average when running Dhrystone 2.1
- Area
  - ARM1022E (2x16KB): 6.9mm^2
  - ARM1020E (2x32KB): 10.3mm^2

ARM10200 System Overview



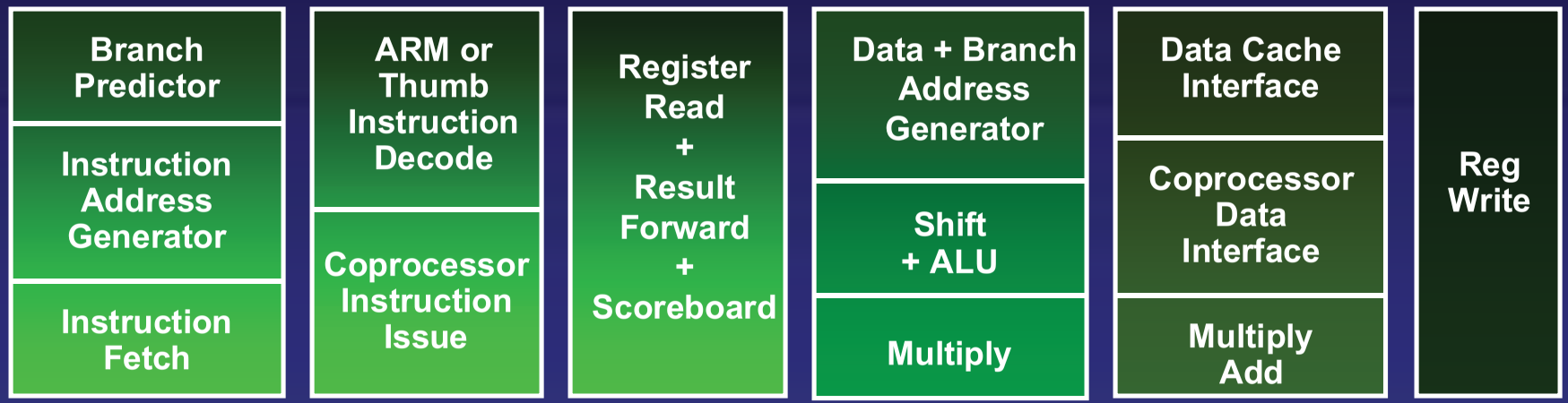
ARM10E Microarchitecture

- 64-bit instruction and data interfaces
- Static branch prediction with branch folding
- Parallel load/store pipeline
  - Dedicated machine for LDM/STM execution; all but the first cycle of these instructions are hidden if no dependencies are encountered
- Parallel execution of multi-cycle coprocessor operations
- Multiply 16 bits per cycle
  - 1-3 cycle throughput and 2-4 cycle latency
  - No data-dependent MUL cycle counts

ARM7 Pipeline versus ARM10

ARM7TDMI

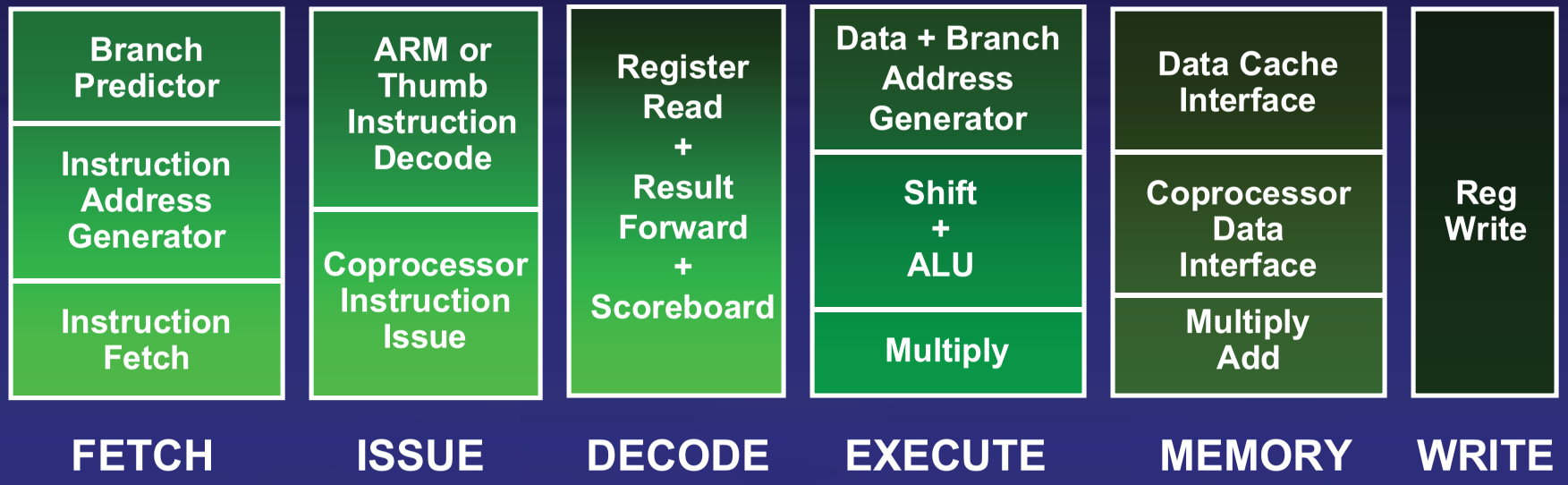
ARM10



ARM9 Pipeline versus ARM10

ARM9TDMI

ARM10



ARM1020E Memory System

- Instruction & Data Caches
  - 32Kbyte Instruction and Data caches
  - Virtually addressed, 64-way set-associative, 32-byte lines, 64-bit R/W
  - Configurable for Write Through or Write Back operation
  - Lockable by line (1/64 of the cache)
- MMUs
  - Two fully associative (I and D) 64-entry TLBs
  - Lockable by entry
  - Support for software loadable TLBs
- Write Buffer
  - Eight 64-bit entries, plus 32-byte cache line castout buffer
- AHB Bus Interface
  - 64-bit wide data transfers, split transactions
  - Multi-layer AHB support (separate I and D-side system interfaces)

ARM1020E Memory System

Performance features:

- Critical word first
- Non-blocking data cache
- Hit-under-miss (H-U-M)
- Data cache streaming (forwarding) from linefills
- Data cache store merging into linefills

ARM1020E Interrupts

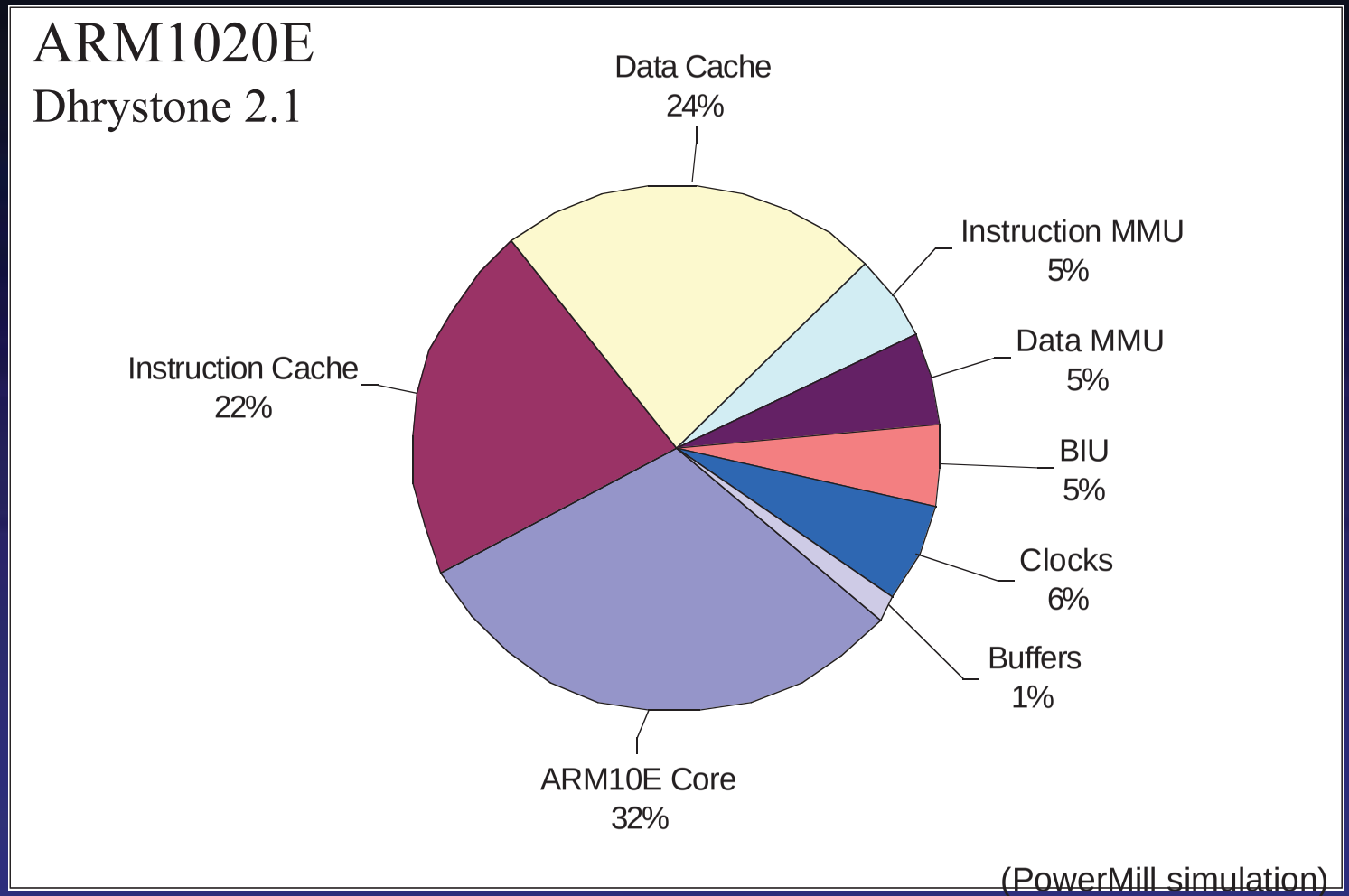
- Interrupts taken in Execute stage
- Fast interrupt mode:
  - First load miss stops further memory ops but not other instructions
  - Limit write buffer depth
- Recommended measures for fast interrupt response:
  - Lock handler code into Caches and TLB
  - Set data cache to write-though (no cast outs)
  - Limit LDM length to 9 registers (spans only 2 cache lines)

ARM1020E Interrupts

- Worst case Interrupt response time to enter handler (G:H Clock 1:1)
  - Worst case of outstanding memory operations (LDM just started)
  - 3 table walks needed (unless TLB locked down)
  - Write buffer full, bus not granted by default

CYCLES (approx)	Fast Interrupt mode	Max Regs in LDM	Write through D cache	TLB locked down
171		16		
148	✓	16		
129	✓	9		
63	✓	16	✓	✓
48	✓	9	✓	✓

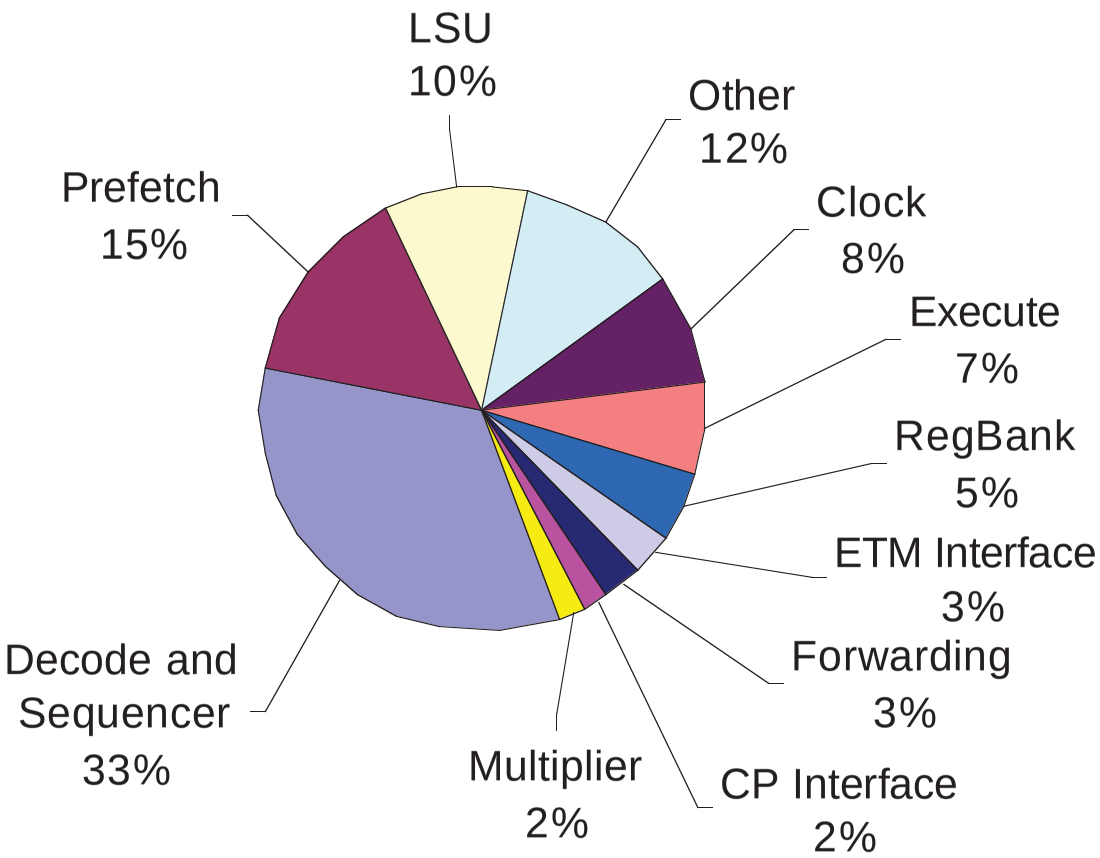
ARM1020E Dynamic Power



ARM10E Dynamic Power

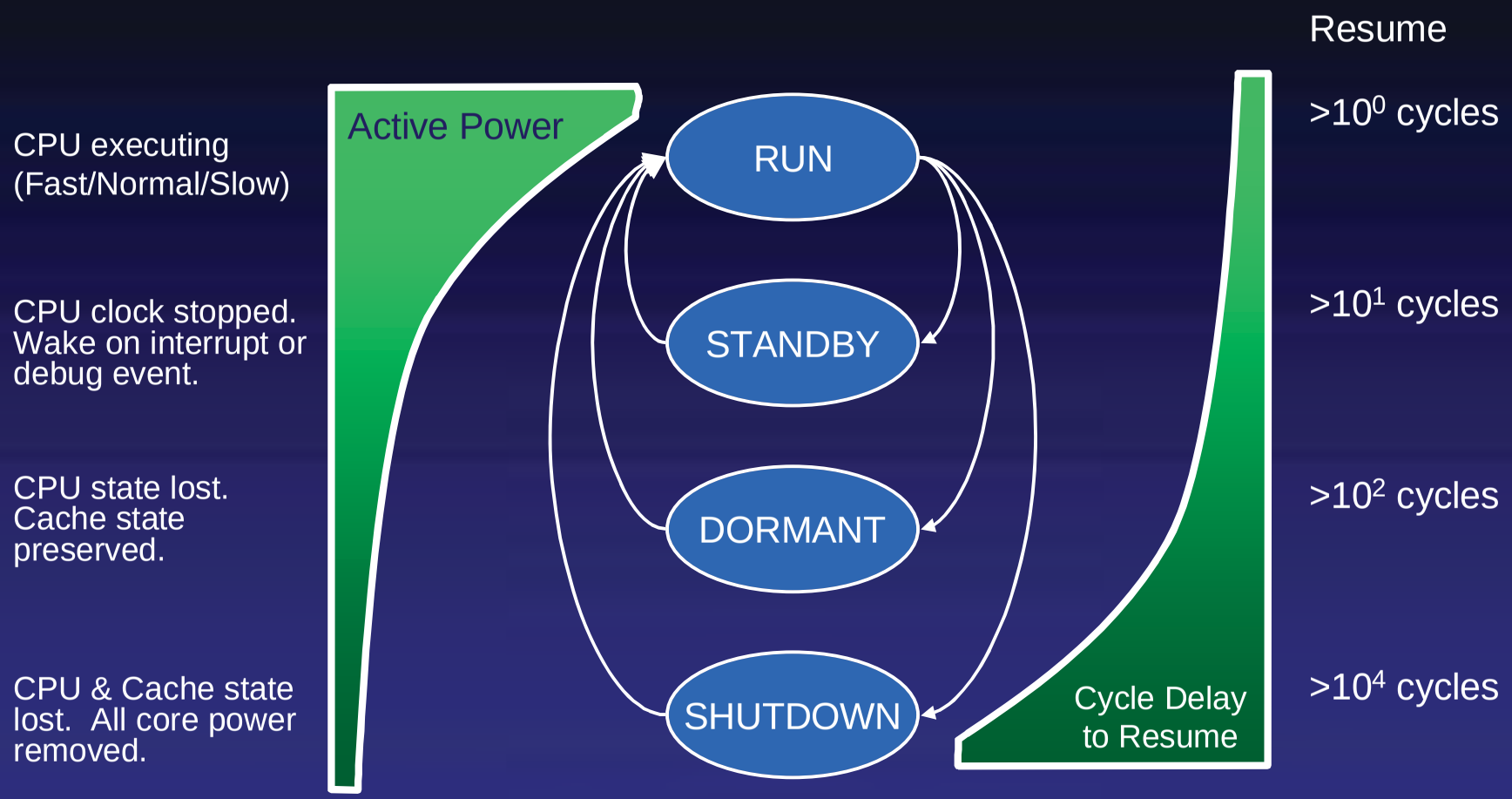
ARM10E Core

Dhrystone 2.1

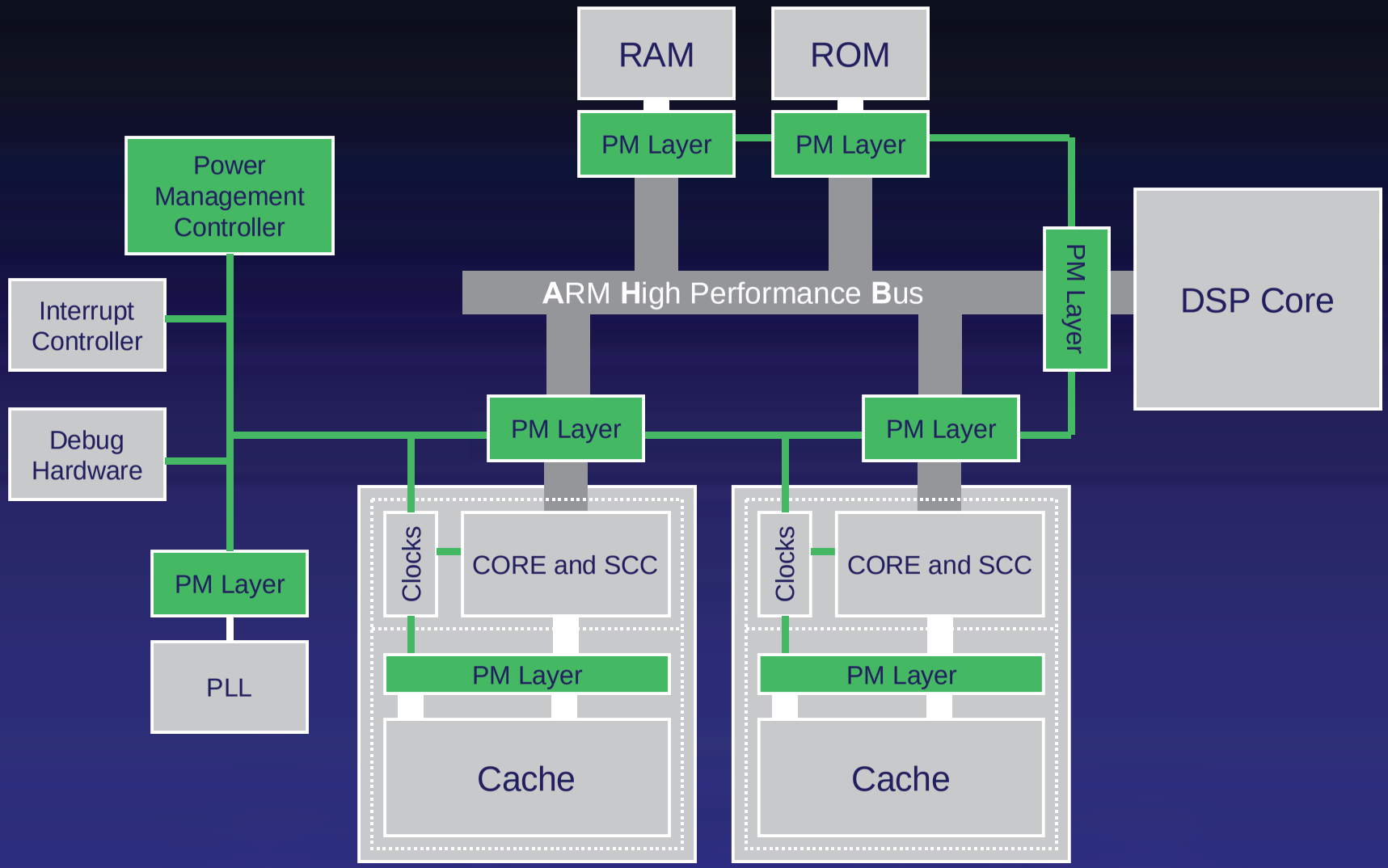


(PowerMill simulation)

Power Down


Resume
CPU executing (Fast/Normal/Slow)
Active Power
RUN
>10^0 cycles
CPU clock stopped. Wake on interrupt or debug event.
STANDBY
>10^1 cycles
CPU state lost. Cache state preserved.
DORMANT
>10^2 cycles
CPU & Cache state lost. All core power removed.
SHUTDOWN
>10^4 cycles
Cycle Delay to Resume

Power Down


RAM
ROM
PM Layer
PM Layer
Power Management Controller
Interrupt Controller
Debug Hardware
ARM High Performance Bus
PM Layer
DSP Core
PM Layer
PM Layer
PM Layer
PLL
Clocks
CORE and SCC
Clocks
CORE and SCC
PM Layer
PM Layer
Cache
Cache

VFP10

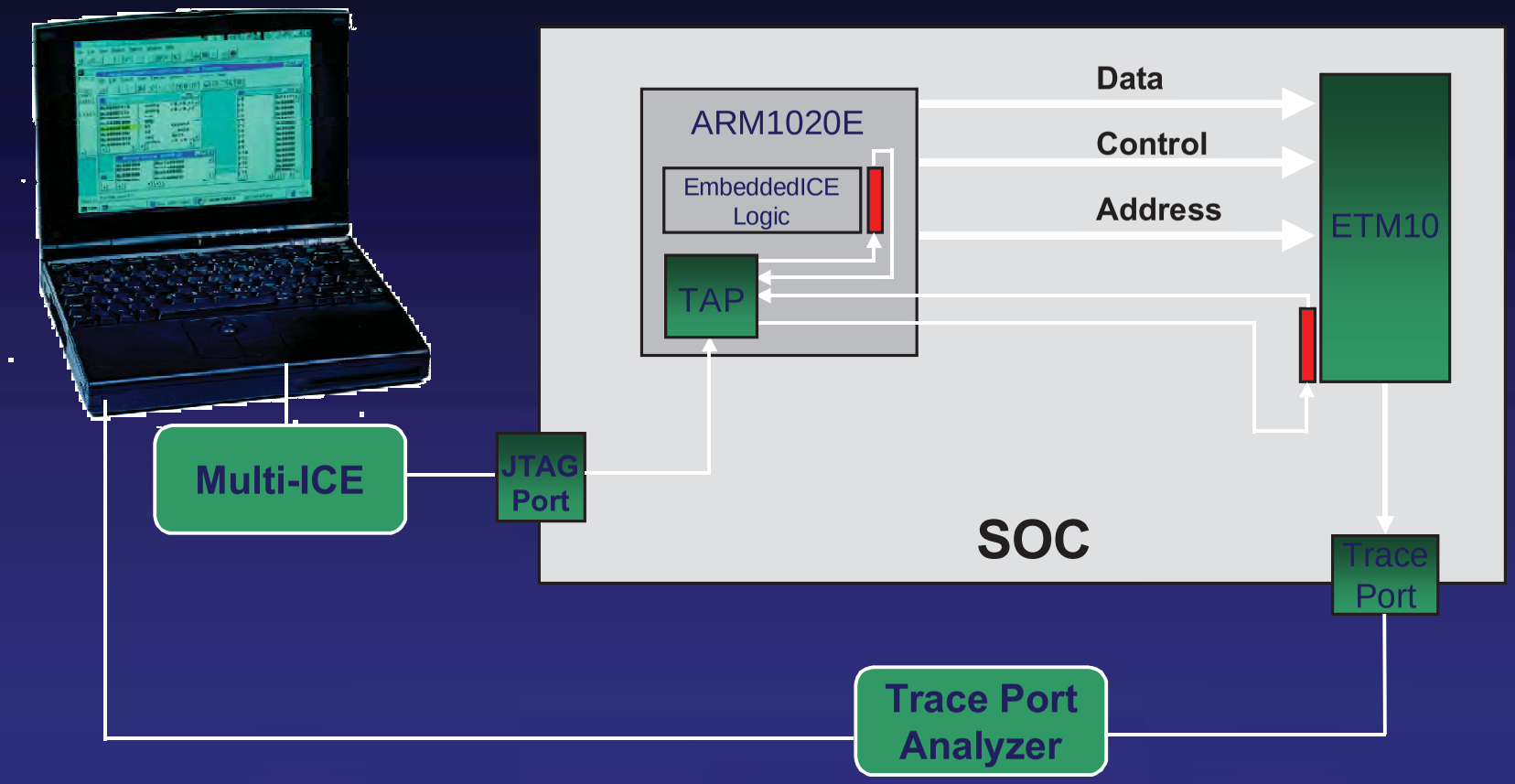
- Full IEEE 754 compliant (with SW support)
- Performance:
  - 236 MFLOPS Linpack (SAxPY) @ 400MHz
  - 400M FIR Taps (800 Peak MFLOPS) @ 400MHz
- Functions supported in hardware
  - Multiply, add, multiply-add, subtract, multiply-subtract, negate, negate multiply, negate multiply-add, negate multiply-subtract, absolute value, compare, convert, divide and square root, conversions
- Most IEEE 754 exceptions handled in hardware
- RunFast mode
  - No trapping enabled (Denormals flush to +0)
  - NaN fractions not propagated (not typical)

VFP10

- 7 Stage pipeline
  - Fetch - Issue - Decode - Execute (E 1) - E 2 - E 3 - E 4/WB
- 32 Single precision / 16 Double precision registers
- High performance short vector operations
  - Register banks operate as hardware circular queues and can be addressed as short vectors (up to 8 values)
- Separate divide/square root unit
  - Supports load/store, and arithmetic operation in parallel with divide/square root operation
- Separate load/store unit
  - Load/store operations may be done in parallel with data processing operations
  - 64-bit unidirectional data interfaces
- Area: ~1.6mm^2 in 0.13um

ETM10

Embedded Trace Macrocell



ETM10

- Full real-time instruction and data tracing
- Monitors the core's *internal* buses
- Zero performance overhead
  - Supports high frequency trace with demux-port
- Configurable synthesis for optimum:
  - area
  - features
  - pin count
- Programmed non-intrusively through JTAG

ARM1020E Family Summary

ARM1020E:

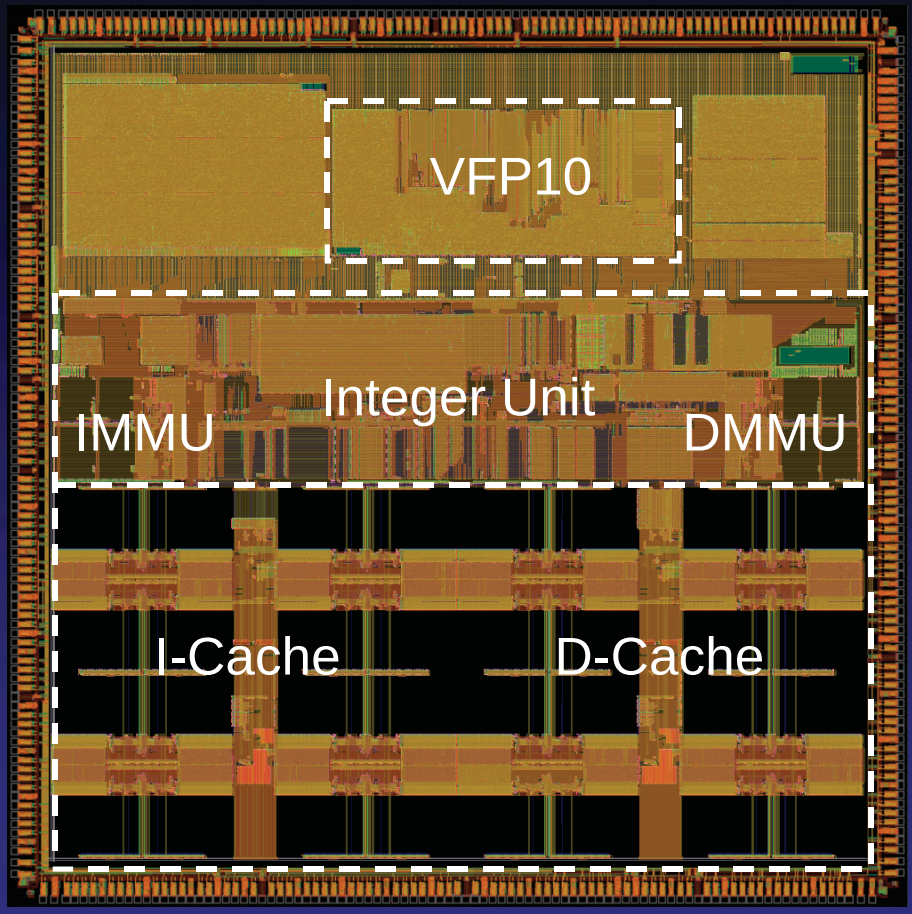
- 500 DMIPS @400 MHz
- 0.51 mA/MIPS
- 10.3mm^2 / 6.9mm^2

VFP10:

- 236 MFLOPS @400MHz
- IEEE 754 Compatible

ETM10:

- Full speed, real time embedded trace



(ARM10200r1)

EXHIBIT 2

Low Power Design Techniques for Microprocessors

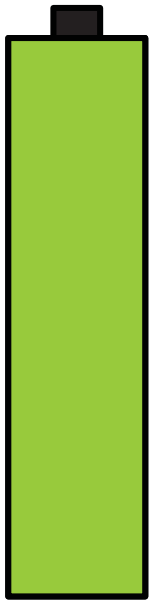
ISSCC, Feb 4th 2001

Simon Segars

VP Engineering, ARM Inc.

Agenda

- Introduction
  - why is power consumption an important design criteria of a microprocessor?
- System design
- CPU microarchitecture
- Where does the power go?
  - A look at ARM920T and ARM9TDMI
- Design tools
- Conclusions
  - References



Why should a microprocessor designer care about power consumption ?

Isn’t it all just about performance?

The digital age

- The internet and wireless services are getting married
- Their offspring are handheld digital communication devices that will rapidly evolve in complexity
  - microprocessors becoming pervasive
- Darwinian theory will hold true
  - species which are too big, too heavy, have poor performance or need regular recharging will die..

Microprocessors Everywhere..

Harzoom
MP3 Player

In-Car Digital Player

Ericsson
Screenphone

Nintendo
Gameboy Advance

Linux watch

Litronic Forté Card

Battery technology

- Battery technology moves very slowly
  - Moore's law does not seem to apply
- Li-Ion and NiMh still the dominant technologies
- Batteries still contribute significantly to the weight of a mobile device
  - Nokia 61xx - 33%
  - Toshiba Portage 3110 - 20%
  - Handspring - 10%
- This is getting better over time, but due mainly to advances in other technology

Its not just about mobile devices

- Power consumption important in ‘tethered applications’ too
- Dissipating heat has a large impact on packaging technology and cost
- Excessive switching currents effect reliability
- Cooling fans create noise and add to cost
- Energy Star partnership created to promote lower power devices for environmental reasons

Impacts for Microprocessors

- Processing requirements for portable devices are rapidly increasing
  - functional integration going up
- But power requirements are even more stringent
  - who wants to spend time plugged into the wall?
- The life of the microprocessor designer has got harder

How do we measure Power?

- As with processing performance, there are no good power consumption metrics
- MIPS per Watt is the most common
  - this tells you nothing about performance
- $MIPS^2$ per Watt tells you more
  - but how useful are MIPS?
- Motorola invented 'Powerstone'(1) for Mcore
  - collection of 15 embedded applications
- EEMBC(2) scores per Watt may be better

Other power Metrics

- At the circuit or device level, power-delay-product often used
  - measure the power consumption, measure the propagation delay and multiply
- Useful comparative metric between devices of identical functionality
- Often used in D-Type, adder or multiplier analysis
  - not much use for an entire CPU

Use power metrics wisely...

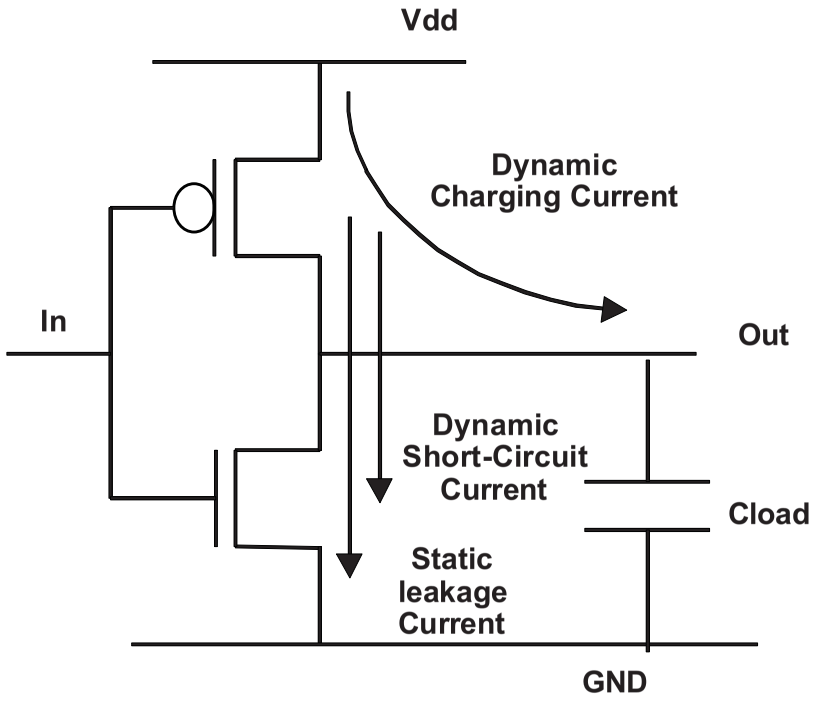
- MIPS per Watt is likely to have no meaning for the application you are running
- The best way to determine the power consumption of a processor in your application is to run your application
- Cache modes, bus activity, data usage all have large bearing on power consumption
- System designers require high-level power models of processors to make system tradeoffs
  - which no one has...

Dynamic and Static Power

- Switching the capacitance is a dominant source of power consumption

  $P=CV^2F$

- F is the *effective* frequency
- So, to reduce your power consumption:
  - Lower your supply voltage
  - Minimise your capacitance
  - Switch your circuit only when you need to
- Static leakage current is now becoming a significant effect in low voltage processes



Process Technology

- As process shrinks, dynamic power is reduced
- Lower Vt transistors mean that Vdd can be less and switching speed is maintained
  - Power consumption reduced by Vdd^2
- Shrinking die size also reduces capacitance as wires get shorter
  - Thinner in one dimension reduces capacitance
  - Thicker in the other dimension and closer together increases capacitance
  - Capacitance reduction not proportional to area
- But, with low Vt, leakage becomes a problem

So why should you care?

- High functionality devices means your processors have to deliver more performance
- Size, weight, packaging, battery life mean that your devices have to become more power efficient
- Battery technology is not helping much
- Process technology helps but introduces new issues
  - static leakage power is becoming as big a problem as dynamic power
- So where do you start?

System design

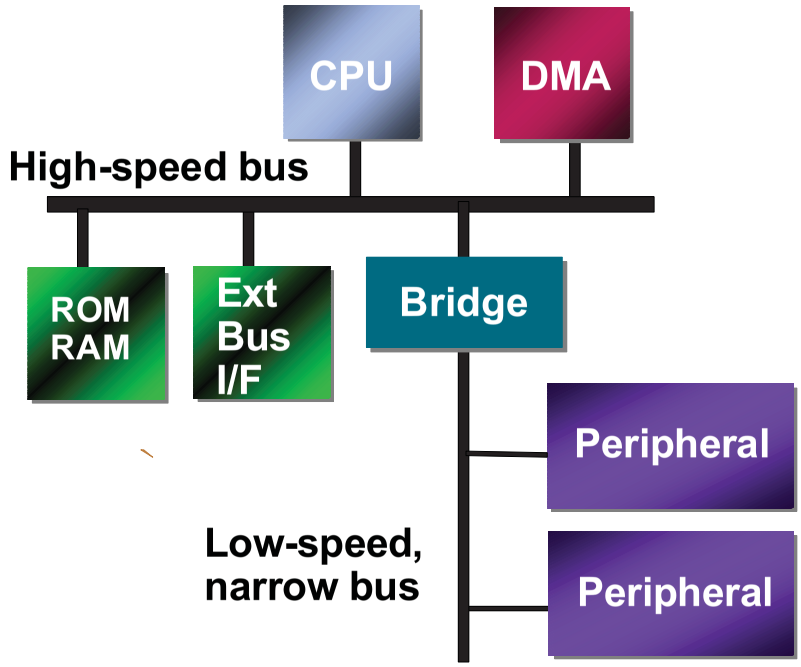
The higher the level of abstraction, the more scope there is for saving power

System Issues

- Choice of algorithm, ISA, system partitioning, data representation etc. have largest impact on overall system power
- The processor designer needs to optimize those factors under his control
- Operating systems are becoming more power aware and this impacts the CPU
- A low power processor is no use if a low power system cannot be built around it

System Partitioning

- By isolating high and low bandwidth devices, system power can be reduced
- The CPU's bus interface needs facilitate different speed responses
  - split transactions
  - fire and forget
  - wait for critical response

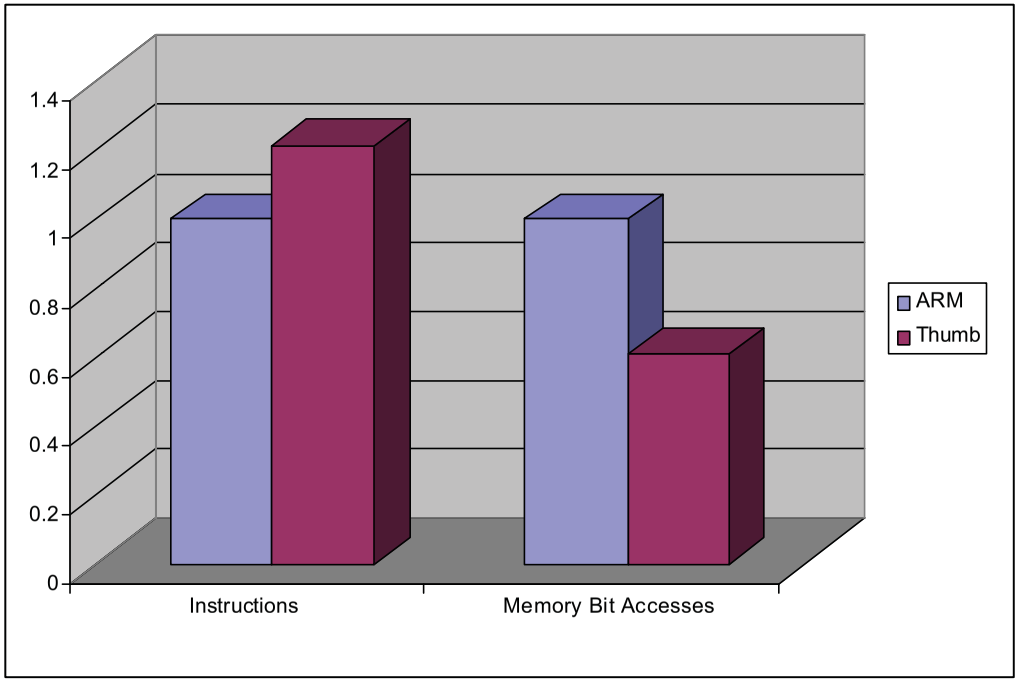


Instruction Sets

- Instruction set efficiency has large impact on system power
  - the fewer memory accesses taken to complete a given function the better
- The higher your code density the better
  - more code in your cache prevents costly external accesses
- Therefore, RISC is potentially bad for power consumption, and CISC is good!

System Power vs CPU Power

- The 16 bit Thumb[3] instruction set is an encoding of a subset of the 32 bit ARM instruction set
- Dhrystone 2.1:
  - 21% more Thumb instruction fetches
  - 39% less memory bit references
- Saving in system power outweighs increased CPU power



Dedicated hardware vs programmable microprocessors

- Dedicated hardware functions can be more efficient than a very flexible microprocessor
- Hardware multipliers are more efficient than software routines due to reduced instruction fetches and register reads
  - Dedicated DSP functions such as Viterbi very efficient
- Reconfigurable processors can offer power savings
  - instructions and functionality can be added on a case by case basis allowing the system designer to trade off hardware and software complexity

System-level Power control

- Complex systems require power-aware operating systems to minimize power consumption
- The processor needs to provide functionality to interact with the system and the OS
- Functions can range from static ‘sleep’ modes to dynamic voltage scaling
- Sleep modes commonplace in embedded systems
  - On/off power control
  - clocks stopped
  - state saved then power removed

Dynamic Voltage Scaling

- Voltage scaling appearing in mobile x86 market
  - Intel - SpeedStep
  - AMD - PowerNow
  - Transmeta - Longrun
- By optimizing voltage and frequency for a given work load, power may be reduced
- Introduces a new challenge - designers need to ensure that their circuits will operate linearly across the voltage range[4]

LongRun[5]

- Combined software/hardware approach
- Software monitors the processing requirement and adjusts voltage and frequency to match
  - frequency range 200-700MHz
  - voltage range 1.1 - 1.6V
- On chip power management hardware uses an external interface to communicate with a system level voltage regulator
- The result is significant temperature and average power reductions

System design - summary

- The CPU designer will always consider system performance when designing the external interfaces
  - But power is equally important
- A top down approach must be taken to achieve low power end systems
  - interaction between software and hardware becoming critical
- Allowing for voltage scaling changes how you must design your circuits

CPU microarchitecture

Pipelines, parallelism and prediction

Microarchitecure effects on power

- Complexity = Power
- Pipeline depth
  - more stages increase D-type count and clock load
- Parallelism/Scalarity
  - parallel execution units increase overall capacitance
- Speculation
  - guessing wrong wastes power
- But, performance requirements are going up
  - so we need to work out how to increase microarchitectural complexity without sacrificing power

Pipeline depth

- Deep pipelines involve large numbers of clocked registers throughout a design
- More D-types = greater clock load = higher power
  - D-type design activity for low power has increased significantly over the last few years
- Pentium4 has a 20 stage pipeline, 42M transistors and consumes 66W(6)
- Driving the clock in a CPU forms a significant proportion of the overall power in a CPU
  - clock power accounts for 30-40% of the total consumption in Alpha 21264(7)

D-type power issues

- Power consumption within a D-type arises from clock load and data activity
  - designs can be optimised for low clock power, low data power or speed, but hard to optimise for all three
- Therefore different D-types should be used in different areas of the design
  - only use fast, power hungry designs on critical paths
- Stojanovic et al[8] compare D-type designs
  - large spread of power, delay, and power-delay product
- D-type selection critical in heavily pipelined designs

Speculation bad, simplicity good

- Branch prediction often added to a processor to improve CPI
- Complex schemes involving history tables are expensive on power
  - effectively there is another cache in the system
- Simple static schemes yield lower performance yet have low power cost
- In both cases guessing wrong cost power
  - any speculative processing has to be thrown away an original machine state restored

Scalarity

- Superscalar and VLIW cores add ‘C’ to increase instruction throughput
  - parallel execution units
  - hardware resolution of resource constraints
- But the added complexity can significantly increase power consumption
  - out-of-order issue logic in Alpha 21264 consumes 18% of the total chip power
- VLIW cores also suffer from poor code density
  - leads to high power consumption in the memory system

So simpler is better?

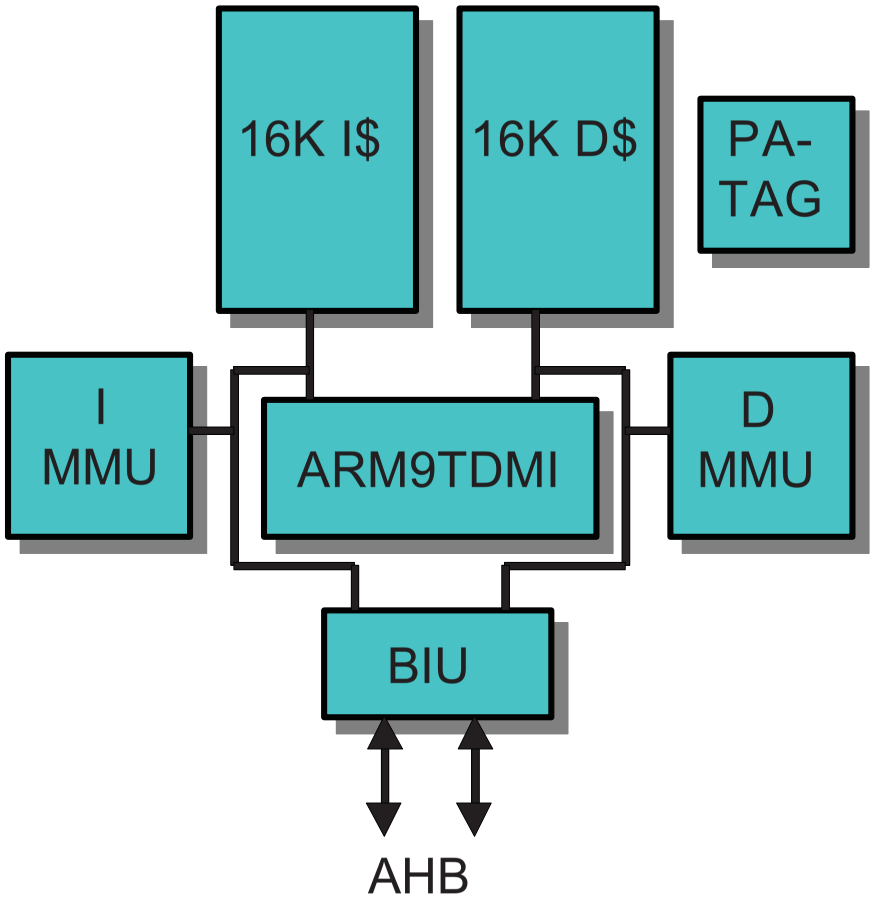
- Yes and no
- If you are able to adjust operating voltage then:
  - build the highest performance processor you can given the area budget,
    - but take care to control effective Frequency
    - make sure your circuits can handle low voltages
  - and run it at the lowest possible voltage
  - The savings in V^2 will outweigh the increase in C and F
- However, cost and system issues often don't allow variable operating voltages
  - in which case, keep it simple

Where does the power go?

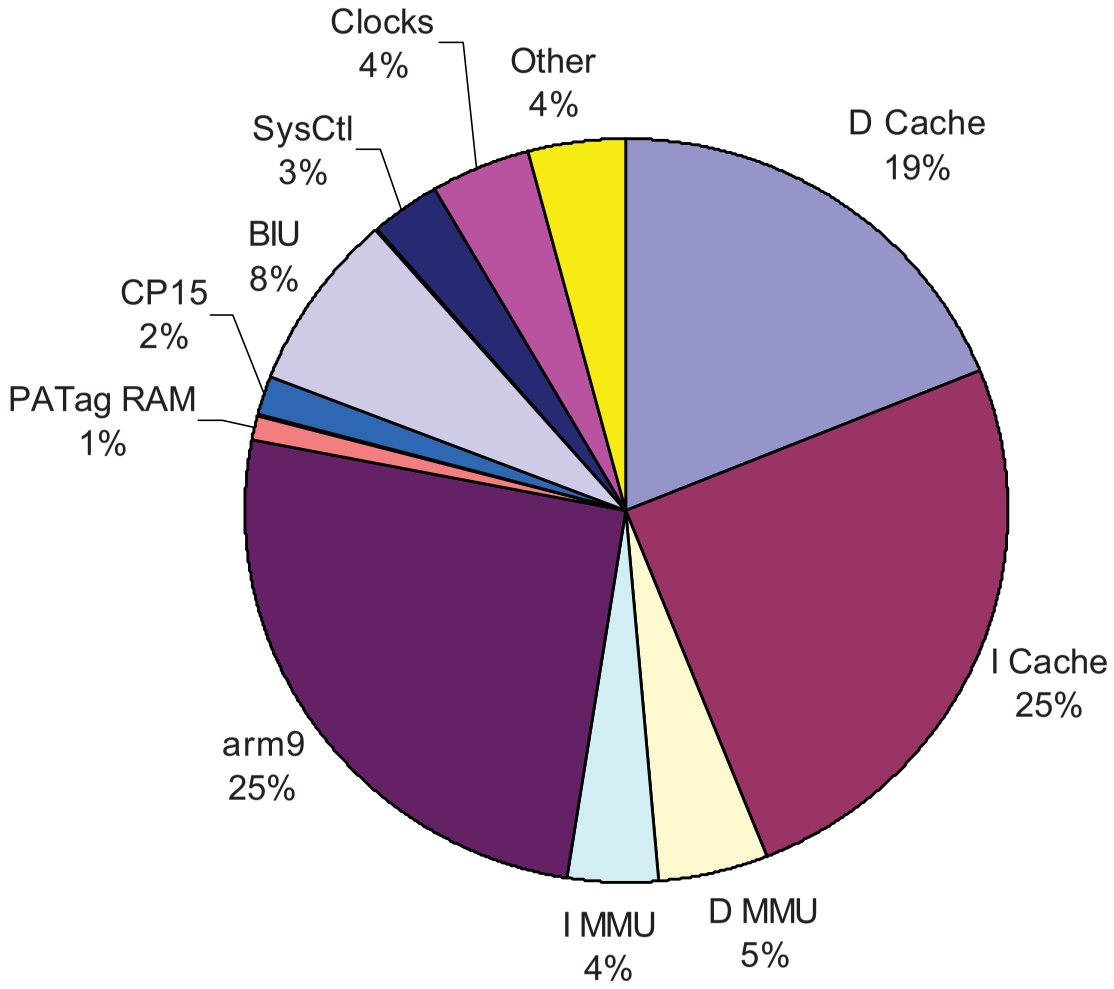
An analysis of ARM920T

ARM920T

- Harvard cached processor
  - ARM9TDMI core
  - 2x16K caches
  - MMU support for VM
- Support for write-back and write-through caches
  - write-through for coherency
  - write-back for low power
- 2.5 Million transistors
- TSMC 0.18μm:
  - 1mW/MHz (1.8V)
  - 200MHz (1.65V)
  - 11.8mm^2



Power Analysis of ARM920T

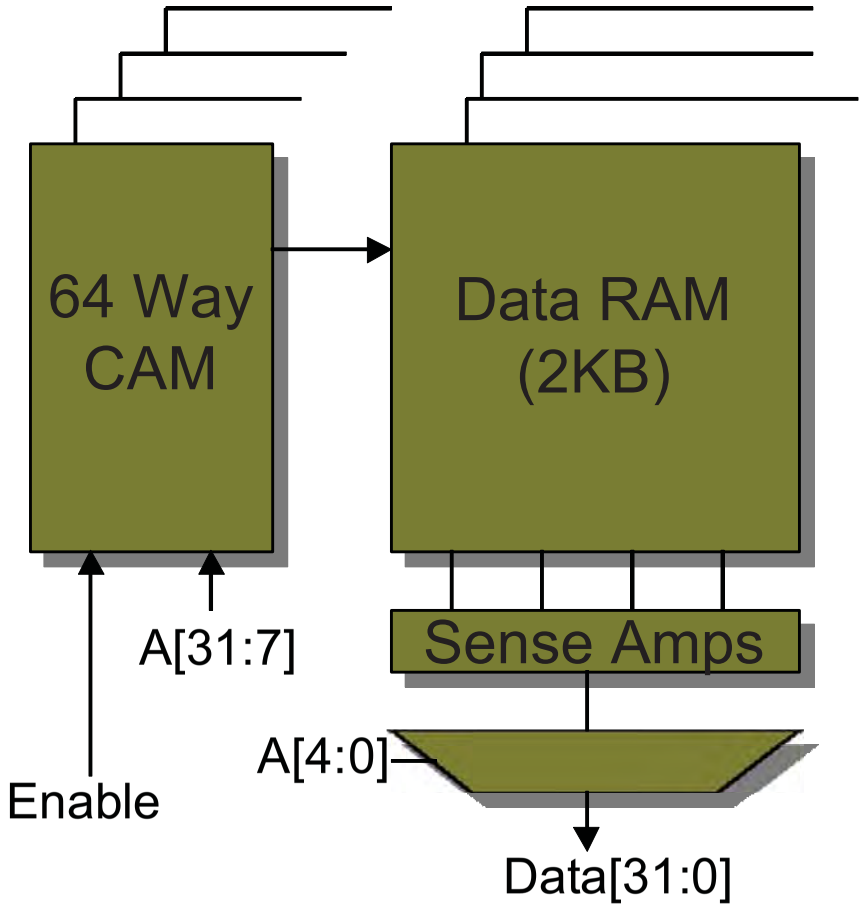


Low Power Caches

- Almost half the total power is consumed by the caches
- ARM920T uses a high-associativity cache segment
  - modular approach allows cache size reconfiguration
  - careful layout provides low power implementation
- Many other processors use low (2 or 4 way) set associative caches
  - including ARM's soft cores
- Sequentiality can be used to reduce cache power for both types of cache

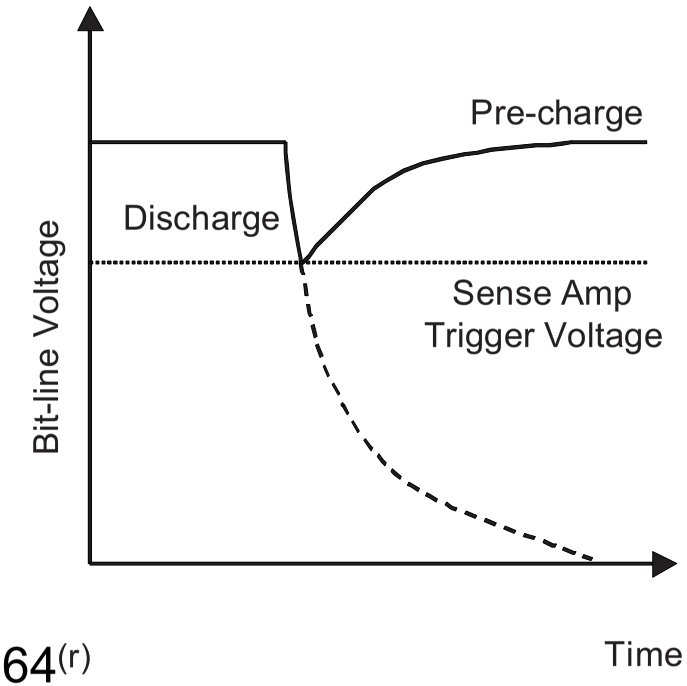
High associativity cache

- Low order address bits select the segment on a non-sequential access
- A pair of words are read
- Data is taken from the word-pair if sequential
  - saves CAM and RAM power
- Data RAM is not activated on a cache miss
- Self-timed, full custom, high performance yet low power



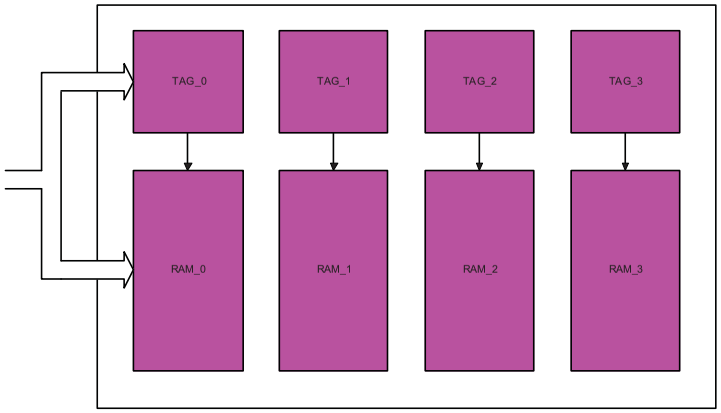
Low-swing bit lines

- The cache bit lines only discharge to the point where the sense amp triggers and then recharges
  - self-timed feedback path
  - bit-lines only drop ~15% of full rail value
- Low swing lines applicable to other areas of CPUs
  - particularly long interconnect busses eg. core ↔ cache
  - 10x saving in bus power in Alpha 21264(r)
  - Also helps improve performance

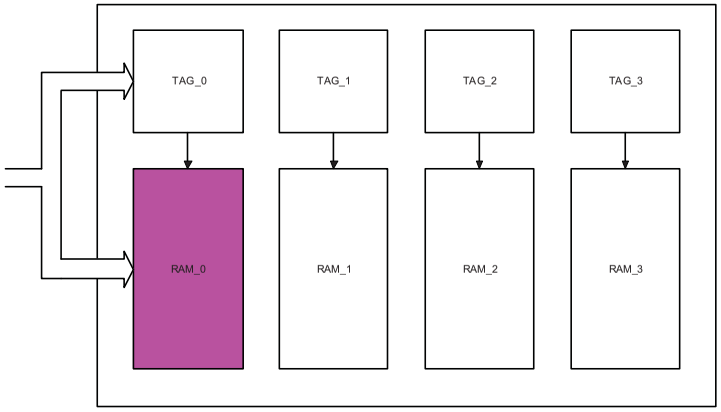


Low associativity caches

- More suitable for ASIC flows
- All TAG arrays looked up every non-sequential access
- RAMs often looked up speculatively in parallel for performance
- Only addressed set accessed on sequential cycles
- Again, whole line can be latched



Non-sequential Access



Sequential Access

Associativity effect on power

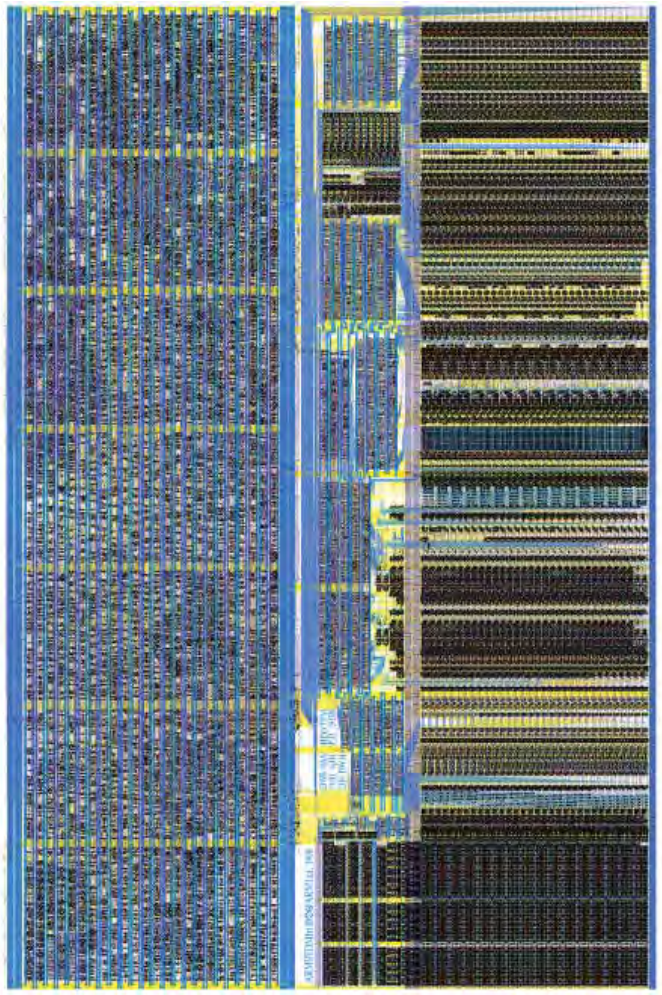
- Higher number of cache ways increase power
  - more capacitance switched per cache access
- Most CPUs fix the associativity
  - but best cache architecture is algorithm dependant
- MCore M340 provides cache reconfiguration to alter the number of active ways[9] in its cache
- Results show that by enabling the optimum number of ways power can be reduced by up to 50%
  - requires an RTOS to reprogram the cache control register on a task switch

Virtually addressed caches

- ARM920T uses a virtually addressed cache
  - address translation only occurs on a cache miss
- In write-back mode, the physical address needs to be recalculated when writing dirty data to memory
  - need to re-access the TLB which may miss
- A ‘physical address TAG’ is used to cache translated data addresses to accelerate the process and save power
  - no need for TLB look up or external page table walk

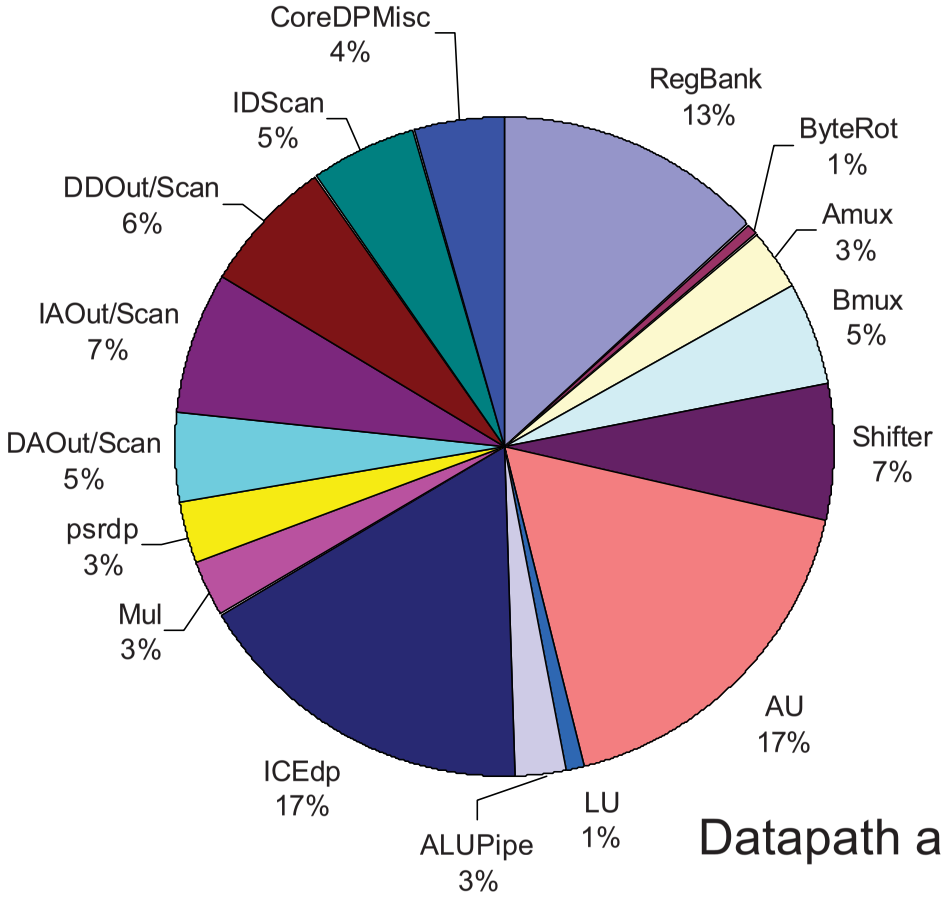
The CPU Core - ARM9TDMI

- 5 stage pipeline
- Harvard architecture
- ARM v4T compliant
  - ARM and Thumb instruction decoders
- 110,000 transistors
- TSMC 0.18μm:
  - 0.3mW/MHz (1.8V)
  - 220MHz (1.65V)
  - 1mm^2



Power Analysis of ARM9TDMI

- Datapath: 43%
  - RegBank+AU+ Debug = 47%
- Control logic: 53%
- Clock driver:4%



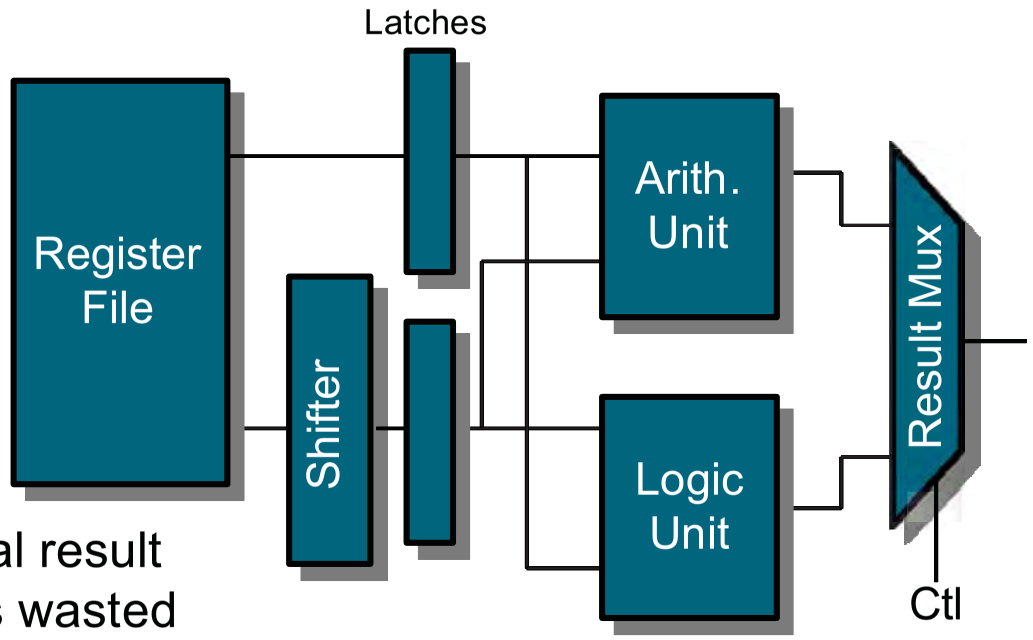
Datapath analysis

Controlling Sub-block power

- The golden rule of low power design:
  - *don't clock or toggle the inputs of an inactive block*
- Partition your functional blocks so that they can be isolated
- Derive control signals early in your instruction decode to allow blocks to be isolated
- Don't take this too far
  - make sure the power saved is not spent generating control signals

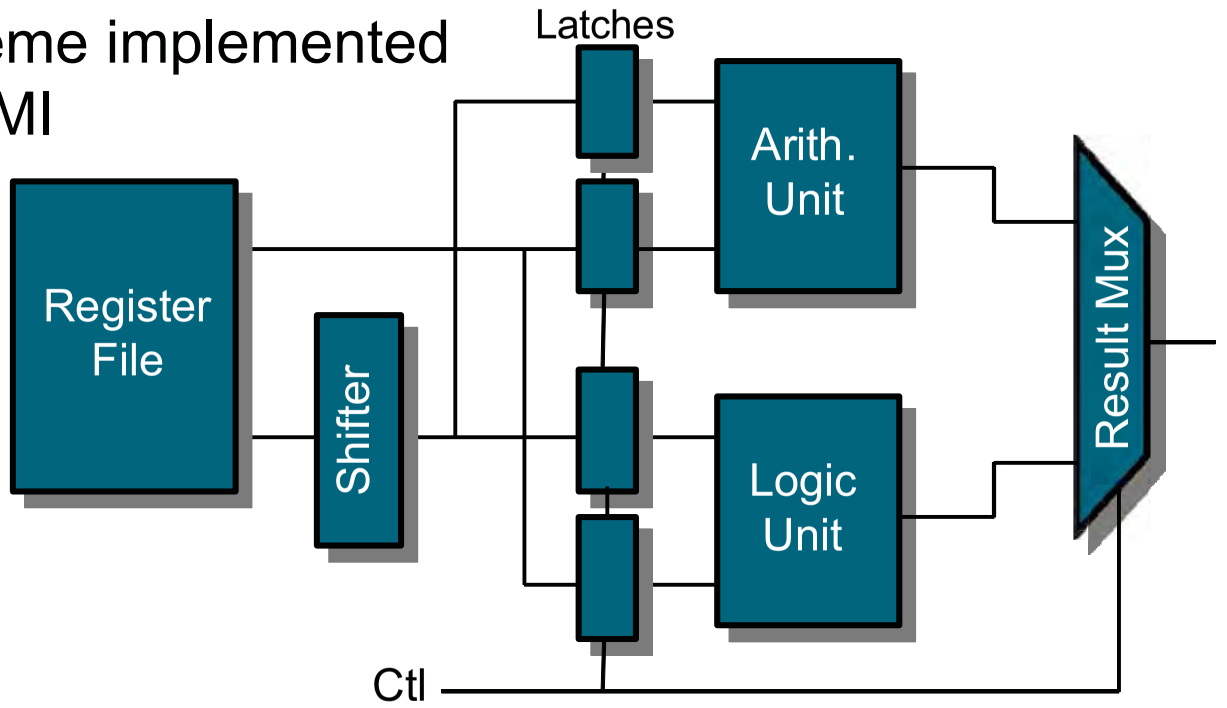
ARM7 Core ALU

- Analysis shows
  - AU used 61% of cycles
  - LU used 39% of cycles
- When LU in use the AU is unnecessarily driven
  - when calculating a logical result 40% of the total power is wasted by the adder
- Therefore isolating the AU can save significant power



Modified Design

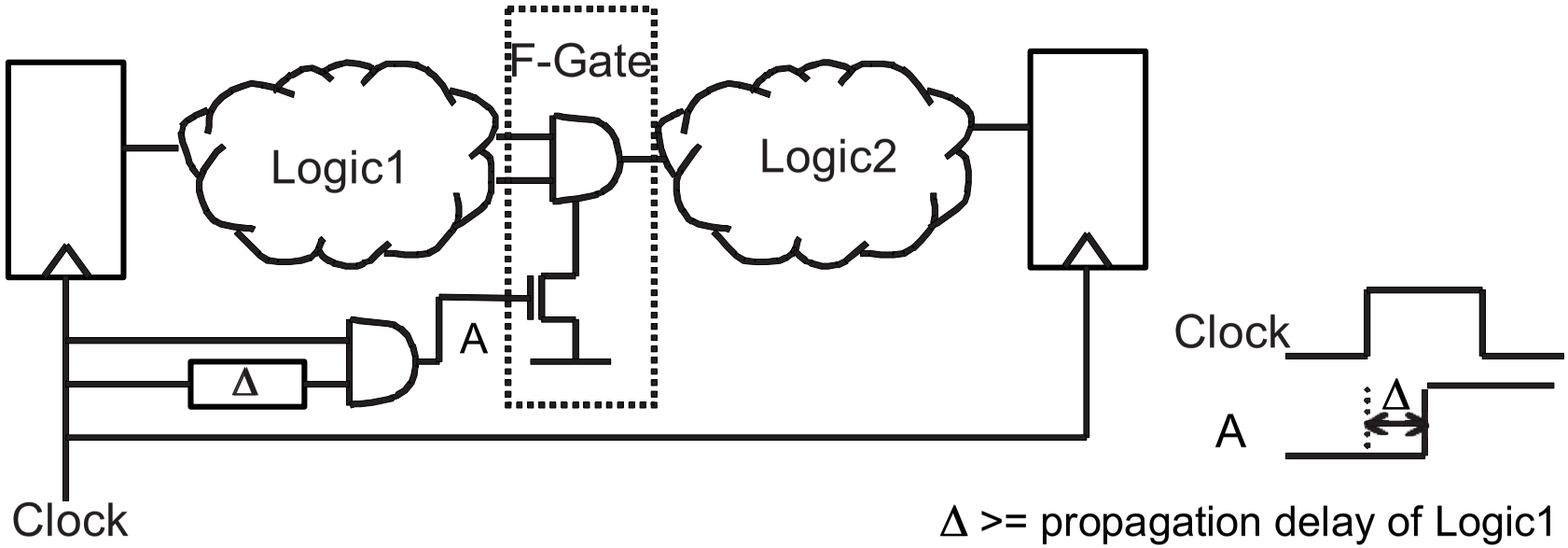
- Potential for 20% saving in power in the ALU
  - no cost in performance
  - extra 64 latches
- Similar scheme implemented in ARM9TDMI



Glitch control

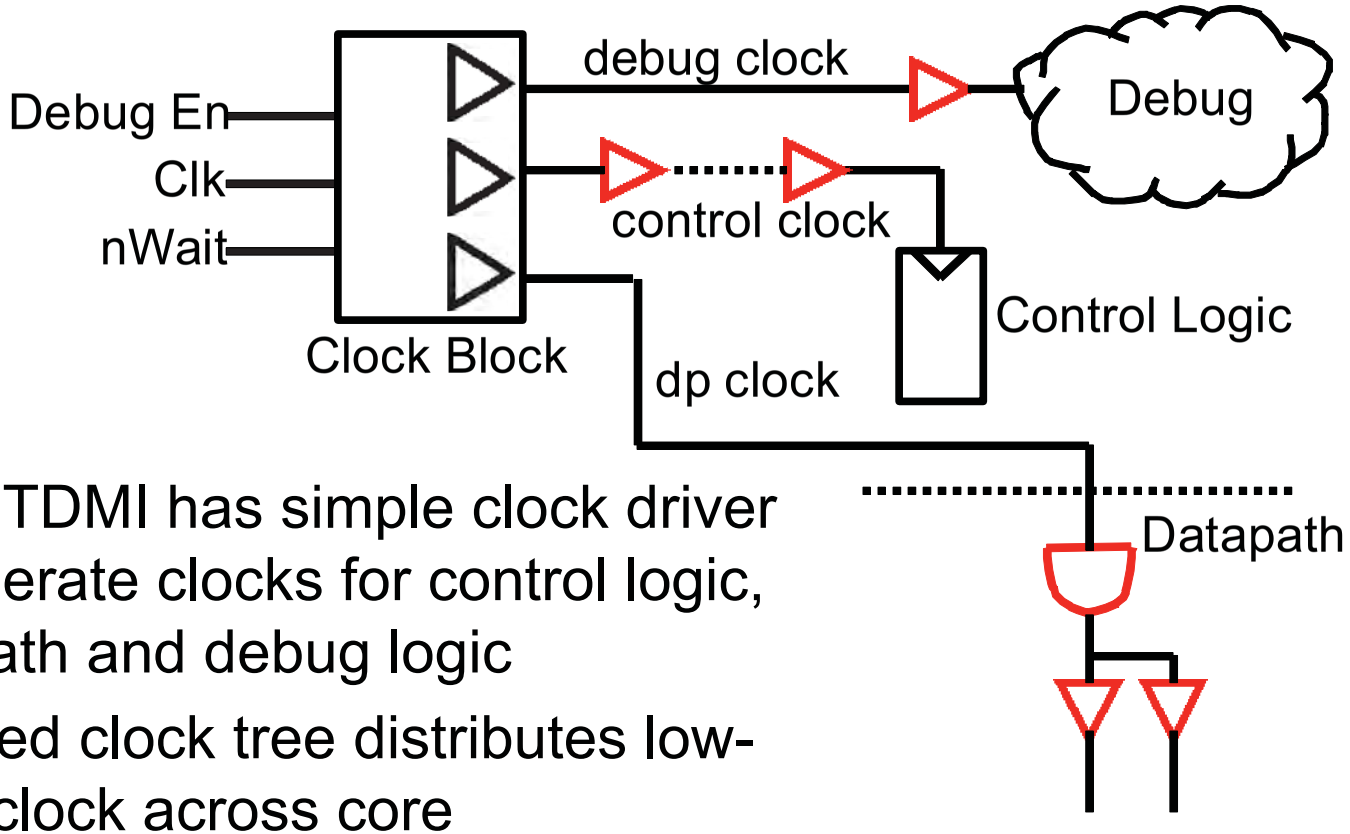
- Within combinatorial logic blocks 15-20% of the power can be caused by glitches[10]
- Logic optimisation can reduce this
  - wide gates have low switching probabilities
- Path matching very difficult as signal arrival times highly layout dependant
- Latches can be used to isolate blocks of logic[11]
  - but expensive in terms of area
- Benini et al[12] suggest modifying gates to isolate stages of logic until inputs are stable

Freeze Gates



- Logic2's inputs frozen while Logic1 evaluates
- Cells grouped together under common delayed clock signal
- Minimal impact on speed and area

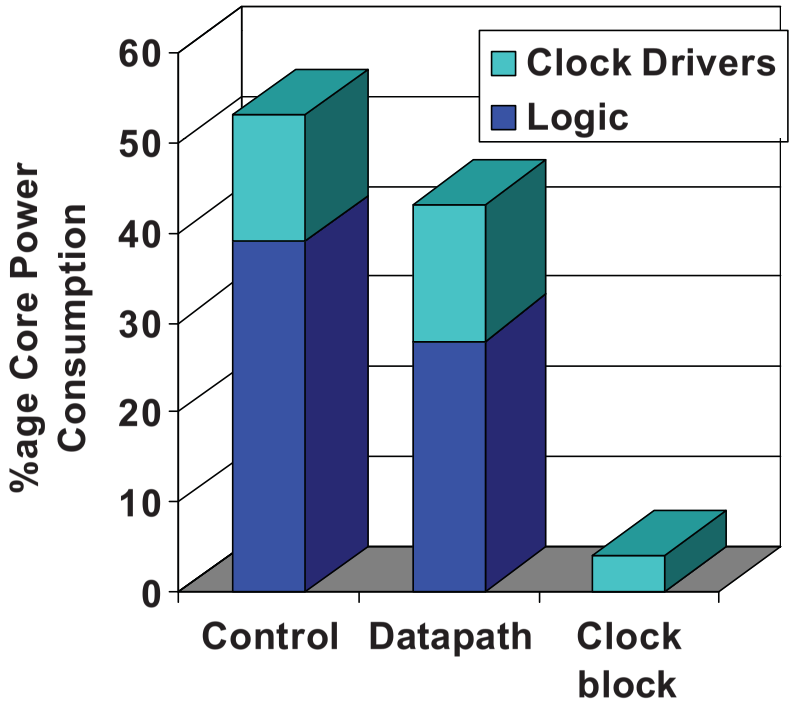
ARM9TDMI Clock Domains



- ARM9TDMI has simple clock driver to generate clocks for control logic, datapath and debug logic
- Buffered clock tree distributes low-skew clock across core
- Global wait signal factored into all clocks

Clock Power

- Clock driver power only 4% of total core consumption
- Power for entire clock tree totals 32% of core
  - excludes clk logic within latches
- Early gating of debug clock allows all debug logic to be frozen when not in use
  - saves ~10% of total core power
- Global wait signal factored into all clocks



So why have a clock?

- Processors built using asynchronous design styles offer the potential for low power implementations
  - No clock, so no clock-tree power
  - side benefit is low electro-magnetic radiation
- Functional units automatically power up depending on which instruction is in execution
  - much finer resolution and no explicit idle-state decode logic
- Manchester University leading with AMULET3i[13]
  - Latest in family with performance similar to ARM9TDMI
  - First commercial use in DRACO wireless DECT chip

Future of Asynchronous

- Mainly still a research activity
- Few implementations to show that the technology can be employed in a commercially interesting way
- Designers brought up on synchronous techniques
- No commercial design tools to help
- But, great potential
  - low power, low emissions, no clock to distribute
- Using asynchronous interfaces between synchronous processing elements on a large SoC could provide a home for this technology

Leakage

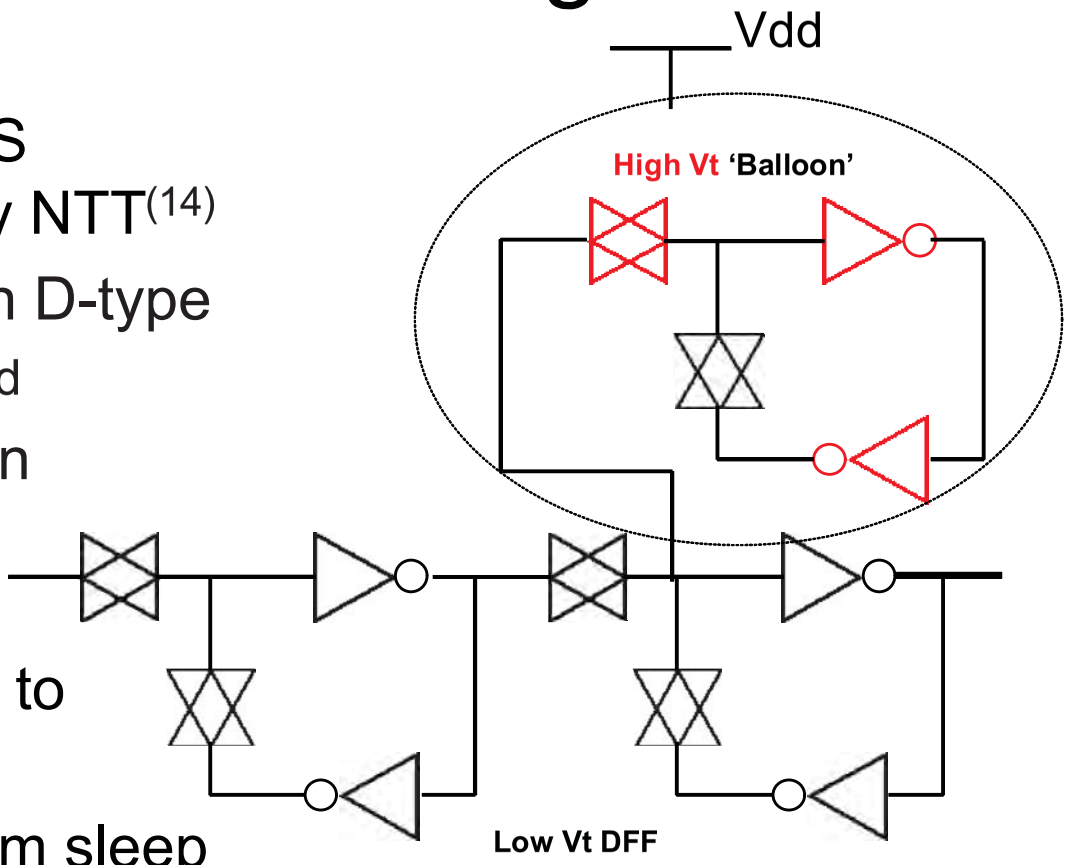
- On low voltage (low Vt) processes leakage currents can become significant to the overall power consumption
  - typically 10-20pA/transistor when Vt~0.7V
  - increases to 10-20nA/transistor when Vt~0.2-0.3V
- Combination of microarchitecture and circuit techniques required to control leakage currents
- Very real problem - leakage becoming common problem even on commodity processes
  - many designs in progress today targeting leaky processes

Leakage control strategies

- Processor sleep modes remove power to leaky sections of the design when not in use
  - eg a multiplier or a cache
- State often needs to be saved to memory
  - system trade off of power cost to write out to memory and then reload vs leakage power saved
  - need OS to determine how long the sleep period is likely to be
- At circuit level substrate biasing and MTCMOS are main approaches in addition to careful transistor sizing

Local State saving

- Balloon logic MTCMOS technique proposed by NTT[14]
- Low Vt devices used in D-type
  - Connected to gated Vdd
- High Vt devices used in 'balloon'
  - Connected to Vdd
- 'Balloon' enabled prior to entering sleep mode
- Allows rapid switch from sleep to regular mode with no loss of state



Summary

- Understand where the power goes in your CPU from historical data and then optimise your design
- Caches, ALUs and register files are big power burners
- Clocks contribute significantly to the power so choose your d-types well and clock gate early
  - or design out the clock all together!
- Ensure that infrequently used logic is clock-frozen, isolated from input activity and even remove Vdd
- Leakage is now a significant issue which affects your microarchitecture and your circuits

Design tools

The EDA industry needs to help

The design space

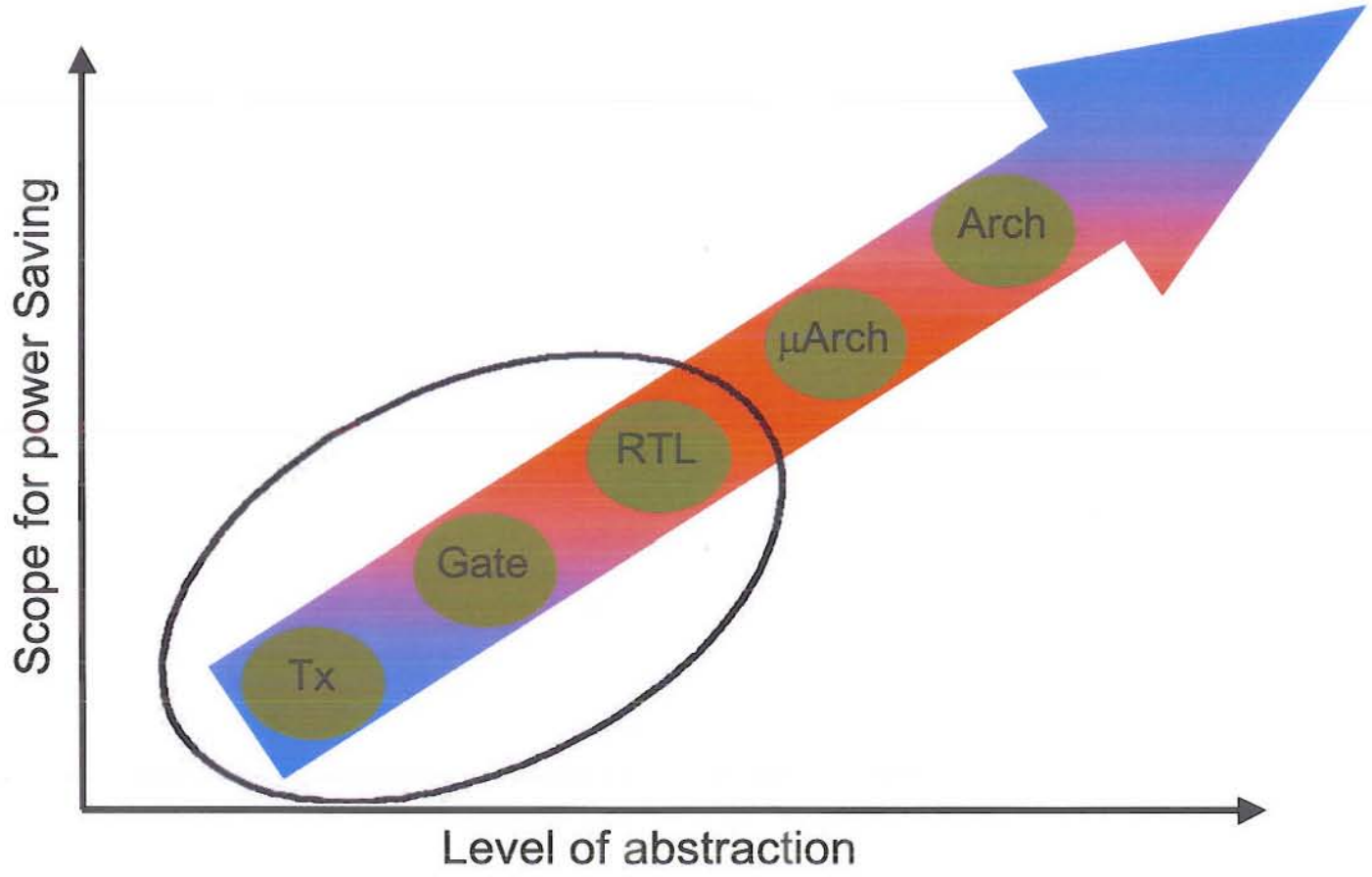


EXHIBIT 2

UNITED STATES DISTRICT COURT

for the

Southern District of New York

Nokia Corporation
Plaintiff
v.
Apple Inc.
Defendant

Civil Action No. 1:09-cv-00791-GMS

(If the action is pending in another district, state where: District of Delaware)

SUBPOENA TO TESTIFY AT A DEPOSITION IN A CIVIL ACTION

To: International Business Machines Corporation, Attn: Corporate Legal
1 New Orchard Road, Armonk, NY 10504

☑ *Testimony:* **YOU ARE COMMANDED** to appear at the time, date, and place set forth below to testify at a deposition to be taken in this civil action. If you are an organization that is *not* a party in this case, you must designate one or more officers, directors, or managing agents, or designate other persons who consent to testify on your behalf about the following matters, or those set forth in an attachment:

Place:	Date and Time:
Alston & Bird LLP, 90 Park Avenue, New York, NY 10016	06/20/2011 9:00 am

The deposition will be recorded by this method: court reporter and videographer

☑ *Production:* You, or your representatives, must also bring with you to the deposition the following documents, electronically stored information, or objects, and permit their inspection, copying, testing, or sampling of the material:

See Attachment A for document requests. Please mail these by June 10, 2011 to the attention of Matthew Urbanawiz, Alston & Bird LLP, One Atlantic Center, 1201 West Peachtree Street, Atlanta, GA 30309-3424.

The provisions of Fed. R. Civ. P. 45(c), relating to your protection as a person subject to a subpoena, and Rule 45 (d) and (e), relating to your duty to respond to this subpoena and the potential consequences of not doing so, are attached.

Date: 05/27/2011

CLERK OF COURT

OR

Signature of Clerk or Deputy Clerk

/s/ Matthew Urbanawiz
Attorney's signature

The name, address, e-mail, and telephone number of the attorney representing *(name of party)* Nokia Corporation and Nokia Inc., who issues or requests this subpoena, are:

Matthew Urbanawiz, Alston & Bird LLP, One Atlantic Center, 1201 West Peachtree St., Atlanta, GA 30309-3424, matt.urbanawiz@alston.com, 404-881-7000

Civil Action No. 1:09-cv-00791-GMS

PROOF OF SERVICE

(This section should not be filed with the court unless required by Fed. R. Civ. P. 45.)

This subpoena for *(name of individual and title, if any)* _____

was received by me on *(date)* _____ .

❒ I served the subpoena by delivering a copy to the named individual as follows: _____

_____

_____ on *(date)* _____ ; or

❒ I returned the subpoena unexecuted because: _____

_____ .

Unless the subpoena was issued on behalf of the United States, or one of its officers or agents, I have also tendered to the witness fees for one day's attendance, and the mileage allowed by law, in the amount of $ _____ .

My fees are $ _____ for travel and $ _____ for services, for a total of $ 0.00 .

I declare under penalty of perjury that this information is true.

Date: _____ _____

Server's signature

_____

Printed name and title

_____

Server's address

Additional information regarding attempted service, etc:

Federal Rule of Civil Procedure 45 (c), (d), and (e) (Effective 12/1/07)

(c) Protecting a Person Subject to a Subpoena.

(1) ***Avoiding Undue Burden or Expense; Sanctions.*** A party or attorney responsible for issuing and serving a subpoena must take reasonable steps to avoid imposing undue burden or expense on a person subject to the subpoena. The issuing court must enforce this duty and impose an appropriate sanction — which may include lost earnings and reasonable attorney's fees — on a party or attorney who fails to comply.

(2) ***Command to Produce Materials or Permit Inspection.***

(A) *Appearance Not Required.* A person commanded to produce documents, electronically stored information, or tangible things, or to permit the inspection of premises, need not appear in person at the place of production or inspection unless also commanded to appear for a deposition, hearing, or trial.

(B) *Objections.* A person commanded to produce documents or tangible things or to permit inspection may serve on the party or attorney designated in the subpoena a written objection to inspecting, copying, testing or sampling any or all of the materials or to inspecting the premises — or to producing electronically stored information in the form or forms requested. The objection must be served before the earlier of the time specified for compliance or 14 days after the subpoena is served. If an objection is made, the following rules apply:

(i) At any time, on notice to the commanded person, the serving party may move the issuing court for an order compelling production or inspection.

(ii) These acts may be required only as directed in the order, and the order must protect a person who is neither a party nor a party's officer from significant expense resulting from compliance.

(3) ***Quashing or Modifying a Subpoena.***

(A) *When Required.* On timely motion, the issuing court must quash or modify a subpoena that:

(i) fails to allow a reasonable time to comply;

(ii) requires a person who is neither a party nor a party's officer to travel more than 100 miles from where that person resides, is employed, or regularly transacts business in person — except that, subject to Rule 45(c)(3)(B)(iii), the person may be commanded to attend a trial by traveling from any such place within the state where the trial is held;

(iii) requires disclosure of privileged or other protected matter, if no exception or waiver applies; or

(iv) subjects a person to undue burden.

(B) *When Permitted.* To protect a person subject to or affected by a subpoena, the issuing court may, on motion, quash or modify the subpoena if it requires:

(i) disclosing a trade secret or other confidential research, development, or commercial information;

(ii) disclosing an unretained expert's opinion or information that does not describe specific occurrences in dispute and results from the expert's study that was not requested by a party; or

(iii) a person who is neither a party nor a party's officer to incur substantial expense to travel more than 100 miles to attend trial.

(C) *Specifying Conditions as an Alternative.* In the circumstances described in Rule 45(c)(3)(B), the court may, instead of quashing or modifying a subpoena, order appearance or production under specified conditions if the serving party:

(i) shows a substantial need for the testimony or material that cannot be otherwise met without undue hardship; and

(ii) ensures that the subpoenaed person will be reasonably compensated.

(d) Duties in Responding to a Subpoena.

(1) ***Producing Documents or Electronically Stored Information.*** These procedures apply to producing documents or electronically stored information:

(A) *Documents.* A person responding to a subpoena to produce documents must produce them as they are kept in the ordinary course of business or must organize and label them to correspond to the categories in the demand.

(B) *Form for Producing Electronically Stored Information Not Specified.* If a subpoena does not specify a form for producing electronically stored information, the person responding must produce it in a form or forms in which it is ordinarily maintained or in a reasonably usable form or forms.

(C) *Electronically Stored Information Produced in Only One Form.* The person responding need not produce the same electronically stored information in more than one form.

(D) *Inaccessible Electronically Stored Information.* The person responding need not provide discovery of electronically stored information from sources that the person identifies as not reasonably accessible because of undue burden or cost. On motion to compel discovery or for a protective order, the person responding must show that the information is not reasonably accessible because of undue burden or cost. If that showing is made, the court may nonetheless order discovery from such sources if the requesting party shows good cause, considering the limitations of Rule 26(b)(2)(C). The court may specify conditions for the discovery.

(2) ***Claiming Privilege or Protection.***

(A) *Information Withheld.* A person withholding subpoenaed information under a claim that it is privileged or subject to protection as trial-preparation material must:

(i) expressly make the claim; and

(ii) describe the nature of the withheld documents, communications, or tangible things in a manner that, without revealing information itself privileged or protected, will enable the parties to assess the claim.

(B) *Information Produced.* If information produced in response to a subpoena is subject to a claim of privilege or of protection as trial-preparation material, the person making the claim may notify any party that received the information of the claim and the basis for it. After being notified, a party must promptly return, sequester, or destroy the specified information and any copies it has; must not use or disclose the information until the claim is resolved; must take reasonable steps to retrieve the information if the party disclosed it before being notified; and may promptly present the information to the court under seal for a determination of the claim. The person who produced the information must preserve the information until the claim is resolved.

(e) Contempt. The issuing court may hold in contempt a person who, having been served, fails without adequate excuse to obey the subpoena. A nonparty's failure to obey must be excused if the subpoena purports to require the nonparty to attend or produce at a place outside the limits of Rule 45(c)(3)(A)(ii).

Attachment A

ATTACHMENT "A" TO SUBPOENA

DEFINITIONS

A. A. "IBM" means International Business Machines Corporation, and any of its present or former affiliates, predecessors, successors, subsidiaries (whether owned directly or indirectly), assigns, divisions and operating units thereof, employees, agents, representatives, directors, officers, and entities under common control with International Business Machines Corporation..

B. "Nokia" means Nokia Corporation and Nokia Inc., including their predecessors, successors, parents, subsidiaries (whether owned directly or indirectly), affiliates, divisions and operating units thereof, agents and entities under common control with them.

C. "Apple" means Apple Inc., including its predecessors, successors, parents, subsidiaries (whether owned directly or indirectly), affiliates, divisions and operating units thereof, agents and entities under common control with it.

D. "Including" or any variant thereof means "including without limitation."

E. "And" and "or" shall mean "and/or," and shall be construed both conjunctively as well as disjunctively in order to maximize their scope.

F. "Any" and "all" mean "any and all."

G. "Each" and "every" mean "each and every."

H. "You," "your" or "yours" shall mean Intel, as defined herein.

I. "Thing(s)" has the broadest meaning allowable under Federal Rule of Civil Procedure 34 and includes any tangible object other than a document and, without

limitation, objects of every kind and nature, as well as prototypes, models, or physical specimens thereof.

J. "Document" has the broadest meaning allowable under Federal Rules of Civil Procedure 34, and includes, without limitation, any thing or any written or graphic matter or any medium of any type or description upon which intelligence or information is recorded, or from which intelligence or information can be perceived, including computer, electronic, magnetic and optical media of all kinds, which is or has been in your possession, custody or control, or of which you have knowledge, including the original and any non-identical copy (whether different from the original because of notes made on said copy or otherwise) of any advertising literature; agreement; bank record or statement; blueprint; book; book of account; booklet; brochure; calendar; chart; circuit diagram; circular; coding form; communication (intra- or inter-company); components listing; computer data; computer printout; computer software and supporting indices; data; documentation; flow charts; comments; object code; source code and computer programs; contract; copy; correspondence; data base; design document; diary; die; display; draft of any document; drawing; electronic mail (e-mail); engineering change order; engineering specification; film; film transparency; flyer; forecast; graph; index; instruction; instruction manual or sheet; internet pages; invoice; job requisition; letter; license; log; machine readable form; manual; manufacturing data; manufacturing drawing; map; marketing plan; mask; memoranda; minutes; model; newspaper or other clippings; notes; notebook; opinion; packing checklist; packing list; pamphlet; paper; periodical or other publications; photograph; physical object; press release; price list; print; printed circuit board; product brochure; product specification; promotional

literature; prototype; receipt; record; recorded read-only memory (ROM); recording; report; sales data; schematic; sketch; solicitation; statement; statistical compilation; stenographic note; study; summary (including any memoranda, minutes, notes, records or summary of any (a) telephone or intercom conversation or message, (b) conversation or interview, or (c) meeting or conference); technical, service or operational manual; technical specification; telegram; telephone log; timing diagram; travel or expense records; video recording; videotape; voice recording; voucher; worksheet or work paper; and/or any other documentary material of any nature.

K. "Technical Reference Manual" shall mean all documents that refer or relate to a description of a product's technical specifications, features, design, components, troubleshooting, setup, operation, use, and/or general technical maintenance.

L. "Person" or "persons" shall mean an individual, corporation, proprietorship, partnership, association, or any other entity.

M. "Concerning" means concerning, regarding, describing, comprising, referring to, related to, supporting, favoring, opposing, bolstering, detracting from, located in, considered in connection with, bearing on, evidencing, indicating, reporting on, recording, alluding to, responding to, connected with, commenting on, in respect of, about, in relation to, discussing, showing, describing, reflecting, analyzing constituting, and being.

N. "Entity" means any natural person, corporation, partnership, sole proprietorship, firm, board, joint venture, association, agency, authority, commission or other business entity or juristic person.

O. "Communication" means any contact between two or more entities by which any information or knowledge is transmitted or conveyed or attempted to be transmitted or conveyed, including written contact including letters, memoranda, telegrams, telefaxes, telecopies, telexes or e-mails, text messages and oral contact including face-to-face meetings, telephone conversations, voicemails, answering machine messages and telephonic notes.

P. "Relating to" or "related to" when referring to any given subject matter shall mean, without limitation, any document that constitutes, comprises, involves, contains, embodies, reflects, identifies, states, refers directly or indirectly to, or is in any way relevant to the particular subject matter identified.

Q. The term "identify" when used in conjunction with a person means to provide, to the extent known, the person's full name, present or last known address, and telephone number, and when referring to a natural person, additionally, the present or last known place of employment and, when referring to your current or former director, officer, manager or other employee, additionally the title(s) or position(s) held by such person, the time periods during which such person held such position(s), and a description of the responsibilities of such person to those position(s).

R. The term "identify" when used in conjunction with a document or other thing means to specify the document or thing in sufficient detail to permit Nokia to locate the document or thing.

INSTRUCTIONS

1. You are to search all documents within your possession, custody, or control, wherever located, including but not limited to any documents placed in storage facilities or in the possession of any employee, agent, representative, attorney, investigator, or other person acting or purporting to act on your behalf (whether located at his/her residence or place of business), in order to fully respond to the requests herein.

2. You are to produce documents from any single file in the same order as they were found in such file, including any labels, files, folders and/or containers in which such documents are located in or associated with. If copies of documents are produced in lieu of the originals, such copies should be legible and bound or stapled in the same manner as the original.

3. If you do not produce each document or thing requested herein as they are kept in the usual course of business, you must organize and label the documents or things produced to correspond with the particular document request to which the document or thing is responsive.

4. You are to produce all documents which are responsive in whole or in part to any of the requests herein in full, without abridgement, abbreviation, or expurgation of any sort, and regardless of whether you deem such documents to be irrelevant to the issues in the investigation for which such documents are being sought. If any such documents cannot be produced in full, produce the document to the extent possible and indicate in your written response what portion of the document is not produced and why it could not be produced.

5. You are required to produce not only the original or an exact copy of the original of all documents or things responsive to any of the requests herein, but also all copies of such documents or things which bear any notes or markings not found on the originals and all preliminary, intermediate, final, and revised drafts or embodiments of such documents or things. You are also required to produce all versions of the foregoing documents stored by a computer internally, on disk, on CD-ROM, or on tape.

6. You are to produce any purportedly privileged document containing non-privileged matter, with the purportedly privileged portion excised or redacted.

7. If any of the documents requested herein are no longer in your possession, custody, or control, you are requested to identify each such requested document by date, type of document, person(s) from whom sent, person(s) to whom sent, and person(s) receiving copies, and to provide a summary of its pertinent contents.

8. If any document responsive to these requests has been destroyed, describe the content of such document, the location of any copies of such document, the date of such destruction, and the name of the person who ordered or authorized such destruction.

9. Electronic and computerized materials must be produced in an intelligible format or together with a description of the system from which it was derived sufficient to permit tendering of the material intelligible.

10. If production of any document listed and described herein is withheld on the basis of a claim of privilege, each withheld document shall be separately identified in a

privileged document list. The privileged document list must identify each document separately, specifying for each document at least: (1) the date; (2) author(s)/sender(s); (3) recipient(s), including copy recipients; and (4) general subject matter of the document. The sender(s) and recipient(s) shall be identified by position and entity (corporation or firm, etc.) with which they are employed or associated. If the sender or the recipient is an attorney or a foreign patent agent, he or she shall be so identified. The type of privilege claimed must also be stated, together with a certification that all elements of the claimed privilege have been met and have not been waived with respect to each document.

DOCUMENT REQUESTS

REQUEST FOR PRODUCTION NO. 1:

Documents sufficient to show the first sale of the IBM PowerPC 405LP.

REQUEST FOR PRODUCTION NO. 2:

Documents sufficient to show the first public distribution of Exh. 1 (posted at http://www.research.ibm.com/arl/papers/405lp.pdf).

REQUEST FOR PRODUCTION NO. 3:

Documents, including user guides, technical reference manuals, data sheets, and programming guides, sufficient to show the power management features of the IBM PowerPC 405LP, including documents describing the sleep and hibernation modes of the IBM PowerPC 405LPand the wakeup conditions of those modes.

REQUEST FOR PRODUCTION NO. 4:

The first version of the IBM PowerPC 405LP user guide provided to third-parties outside IBM.

REQUEST FOR PRODUCTION NO. 5:

The first version of the IBM PowerPC 405LP datasheet provided to third-parties outside IBM.

REQUEST FOR PRODUCTION NO. 6:

Documents related to or reflecting any presentations made by IBM at the 2001 Microprocessor Forum related to the PowerPC 405LP or power management.

REQUEST FOR PRODUCTION NO. 6:

Document sufficient to identify IBM processors or instruction processing systems sold before April 29, 2002 that include both (i) a low power mode where the clock to the instruction processing core is gated off and (ii) a mode where power to the instruction

processing core is either gated off while power to other parts is gated on or power to the instruction processing core is reduced below normal operational levels.

REQUEST FOR PRODUCTION NO. 7:

Documents sufficient to show the power management features of IBM processors or instruction processing systems identifiable in documents produced in response to Request for Production No. 6.

REQUEST FOR PRODUCTION NO. 8:

Communications between IBM and Apple regarding the IBM PowerPC 405LP, including communications from IBM employees, such as David Appenzeller, Matthew Mehalic, Norman Rohrer, Mike Mayfield, Peter Sandon, Pradip Bose, Chekib Akrout, and Tim Vonreyn, to Apple employees, including Bill Athas, Hope Chambers, and Lynn Youngs.

REQUEST FOR PRODUCTION NO. 9:

Communications between IBM and Apple, including the employees identified above in topic 6, prior to April 29, 2002 regarding any "nap," "deep nap," or "cryo mode" processor states implemented or contemplated for IBM or Apple products.

REQUEST FOR PRODUCTION NO. 10:

Prior art to U.S. Patent 7,383,453

Attachment B

ATTACHMENT "B" TO SUBPOENA

DEFINITIONS

The definitions set forth in Attachment A are incorporated by reference.

TOPICS

You are required to provide one or more individuals who are knowledgeable and competent to provide testimony about the following topics:

1. IBM's policies and practices involving the documents produced in response to Attachment A, including, but not limited to:

    a. The authenticity of the documents produced in response to Attachment A.

    b. Whether the documents produced in response to Attachment A are true and correct copies of the originals.

    c. Whether the documents produced in response to Attachment A are what they purport to be.

    d. Whether the documents produced in response to Attachment A were created by the people listed as the author, and, if no author is listed, who the author is.

    e. Whether the documents produced in response to Attachment A were created in the normal course of business and/or a regularly conducted business activity.

    f. Whether the creation of the documents produced in response to Attachment A was a regular part of the business activity.

    g. The dates on or about which the documents produced in response

to Attachment A were created.

h. The reasons for creating the documents produced in response to Attachment A.

i. Whether the documents produced in response to Attachment A were created by or based on information from people with knowledge of the activity recorded.

j. Whether the documents produced in response to Attachment A are the types of documents that are normally relied upon as a record of the activity recorded.

k. The subject matter of any of the documents produced in response to Attachment A.

2. The authenticity and public disclosure of Exhibits 1.

3. The history, design, configuration, or structure of the IBM PowerPC 405LP, including power management related functionality, first sale, and public disclosure prior to April 29, 2002.

4. The date of the first public distribution of documents describing the IBM PowerPC 405LP including any datasheets, user guides, and the presentation attached as Exh. 1.

5. Communications prior to April 29, 2002 between IBM and Apple regarding the IBM PowerPC 405LP, including communications from IBM employees, such as David Appenzeller, Matthew Mehalic, Norman Rohrer, Mike Mayfield, Peter Sandon, Pradip Bose, Chekib Akrout, and Tim Vonreyn, to Apple employees, including Bill Athas, Hope Chambers, and Lynn Youngs.

6. Communications prior to April 29, 2002 between IBM and Apple, including the employees identified above in topic 6, regarding any "nap," "deep nap," or "cryo mode" processor states implemented or contemplated for IBM or Apple products.

7. The identification of IBM processors or instruction processing systems sold or publicly disclosed prior to April 29, 2002 that include both (i) a mode where the clock to the instruction processing core is gated off and (ii) a mode where power to the instruction processing core is either gated off while power to other parts is gated on or power to the instruction processing core is reduced below normal operational levels.

8. The power management features of processors or instruction processing systems identified in Topics 7 including (i) the nature of different power modes, (ii) the conditions and events that cause entry into or exit from a low power mode.

EXHIBIT 1

Low Power SOC for IBM's PowerPC® Information Appliance Platform

Gary Carpenter
Chief Architect Scalable Processors
IBM® Corporation

All information in these materials is subject to change without notice. All information is provided on an "as is" basis, without any warranty of any kind. All performance data contained in these materials was obtained in a specific environment and is presented for illustration purposes only. Results obtained in other operating environments may vary.

Power Efficiency Benefits Multiple Markets

New technologies that deliver high performance and greater power efficiency benefit a wide range of customers

- **Energy Constrained Wireless Devices**
  - Web Pads
  - PDAs
  - Cell Phones
  - Notebook PCs
- **Power Sensitive Wired Devices**
  - Cable/DSL Modems
  - Routers/Switches
  - Cellular Base Stations
  - Line Cards

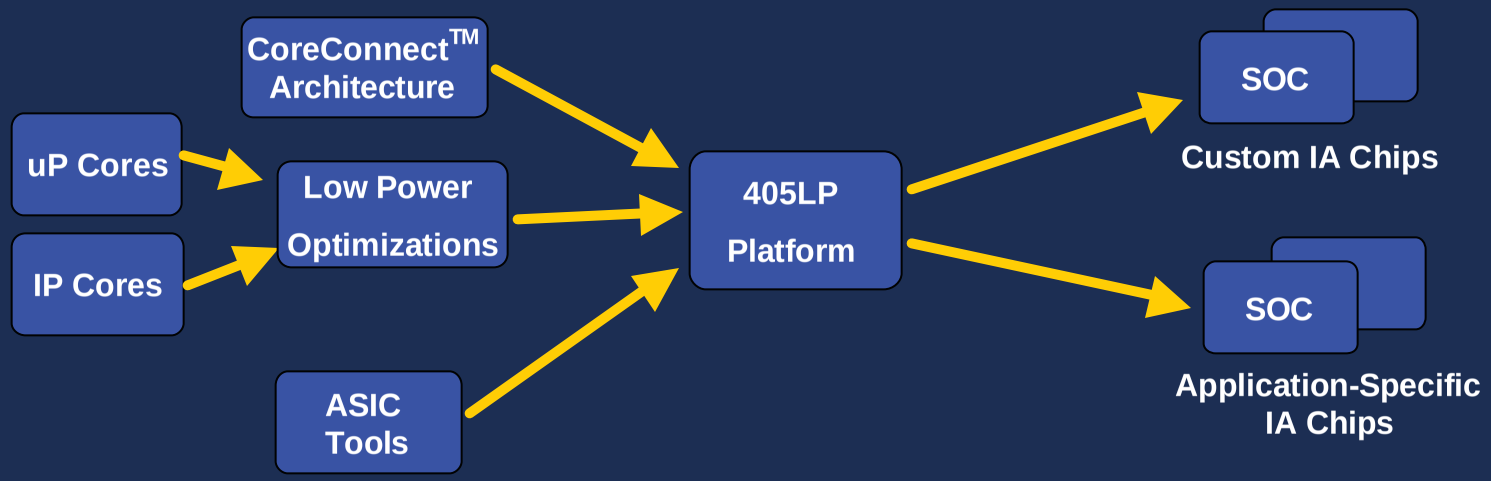
(power was never free and it's not getting cheaper)

PowerPC®

IBM®

Platform for Information Appliances

405LP platform enables highly integrated, power efficient custom and application-specific Information Appliance (IA) chips

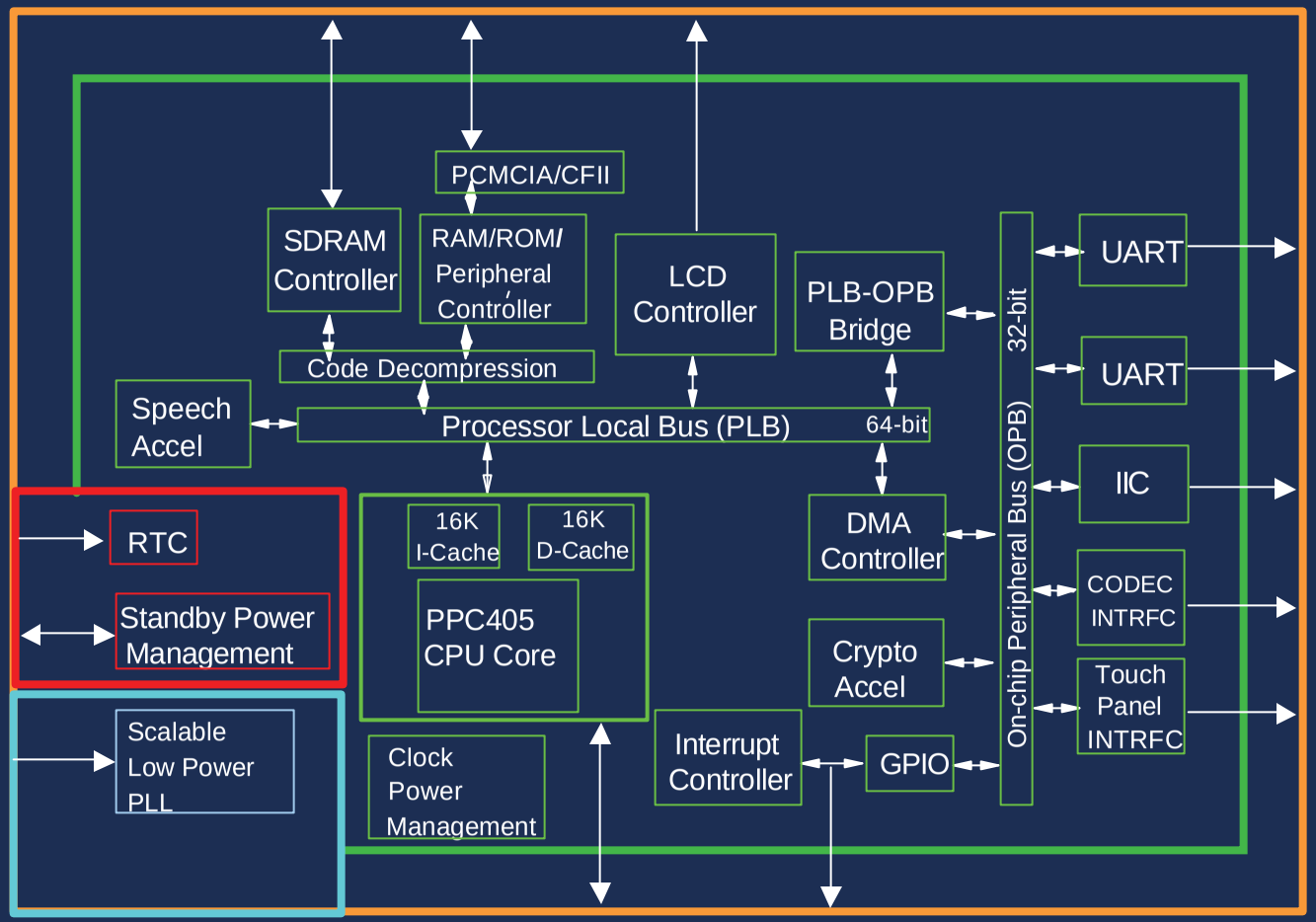


PowerPC®

IBM®

405LP System On a Chip

405LP integrates a rich set of functions for Information Appliances



PowerPC®

IBM®

Low Power Optimizations

The 405LP includes a wide range of low power optimizations to reduce both active and standby power

Active Power Reductions

- Voltage Scaling
- Frequency Scaling
- Flexible Clock Distribution
- Clock Gating
- Hardware Accelerators

Standby Power Reductions

- Clock Freezing
- Hibernation
- Voltage Reduction

PowerPC®

IBM®

Voltage Scaling in CMOS

Reducing operating voltage greatly reduces active power in CMOS

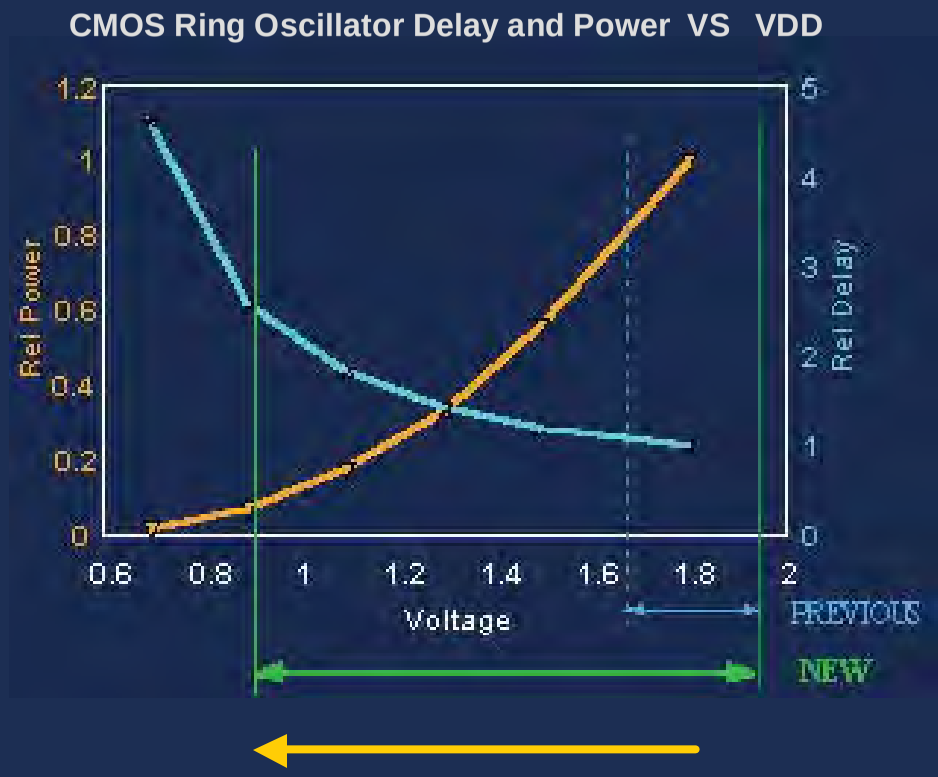
Voltage Scaling Benefits

- Complementary CMOS scales well over a wide voltage range
- Can be used widely over entire chip
- Can optimize power/performance (MIPS / W) over a 4X range

Voltage Scaling Challenges

- Custom Circuits, PLLs, Analog, and I/O drivers don't voltage scale easily
- Avoiding increase standby power in low active power circuits

  (the V_{TH} dilemma)



Operating at 1/2 normal Vdd increases delay 2.4-3.2X but reduces power by > 10X

PowerPC®

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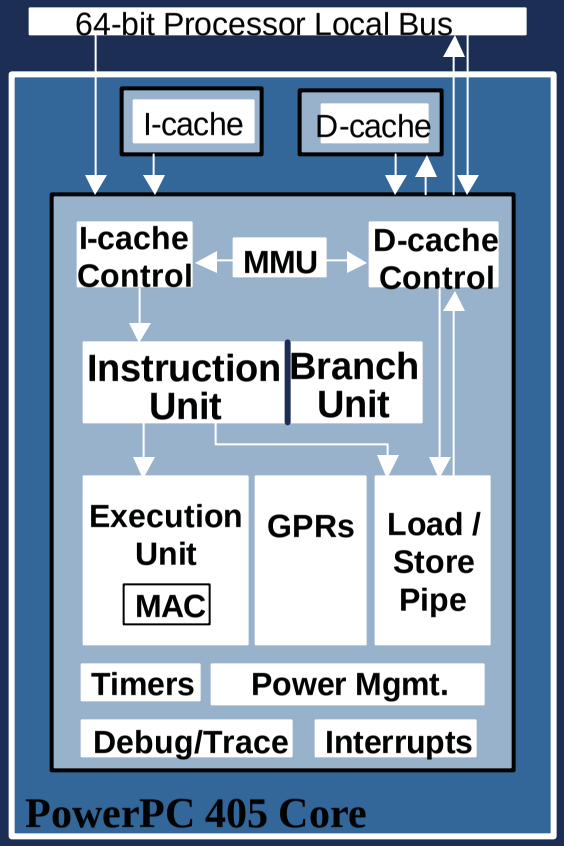
Scalable PowerPC 405 CPU Core

CPU Goals

- Expanded operating voltage range (0.9V to 1.95V)
- Maintain full software and tools with existing compatibility PowerPC 405
- Provide a high performance core capable of high efficiency low power operation

CPU Optimizations

- Redesigned custom circuits within CPU that were sensitive to low voltage operation
- Re-optimize design and timing for extended voltage range
- Verification of equivalence



PowerPC®

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Scalable Clock Generation Subsystem

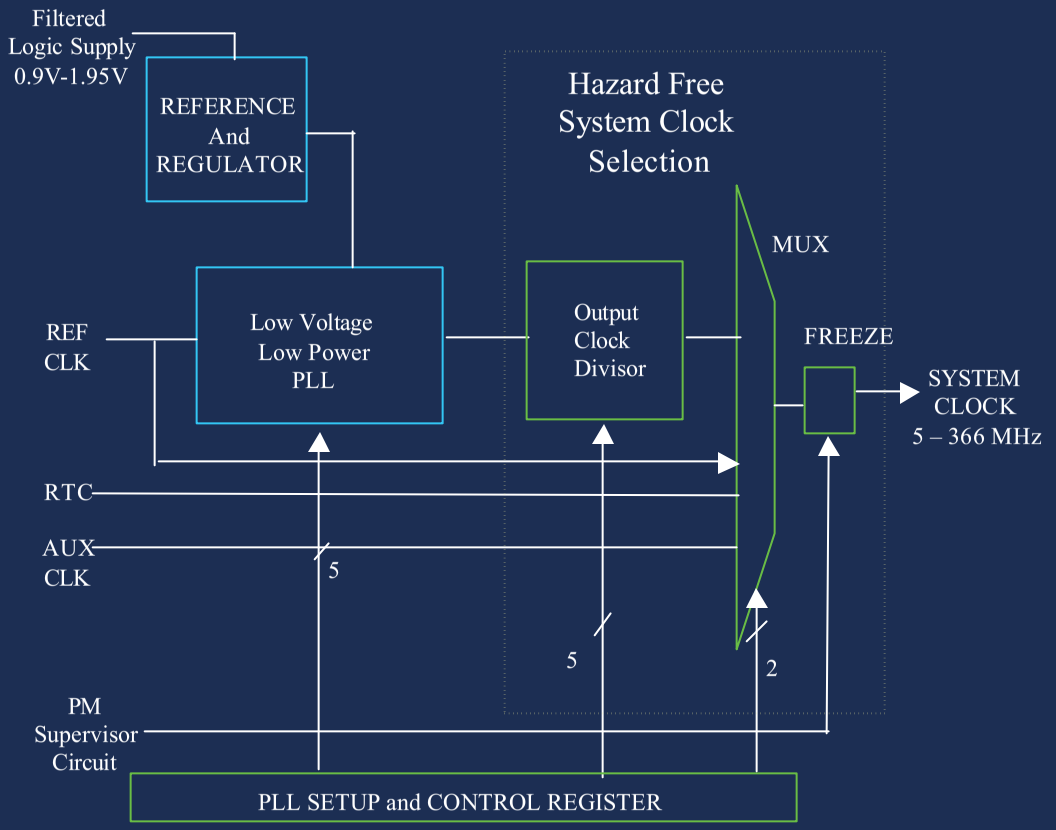
Clocking subsystem enables dynamic voltage and frequency scaling

Low Power Challenges

- Isolating PLL from effects of VDD scaling
- Enabling a wide range of input sources and output frequencies
- Level shifting and duty cycle correction

Clocking Subsystem Features

- Low voltage, low power PLL to generate a high frequency clock
- In-line self biasing regulator for dynamic VDD scaling
- Fast dynamic frequency scaling without losing PLL lock
- Hazard free system clock selection



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Clock Domains and Clock Gating

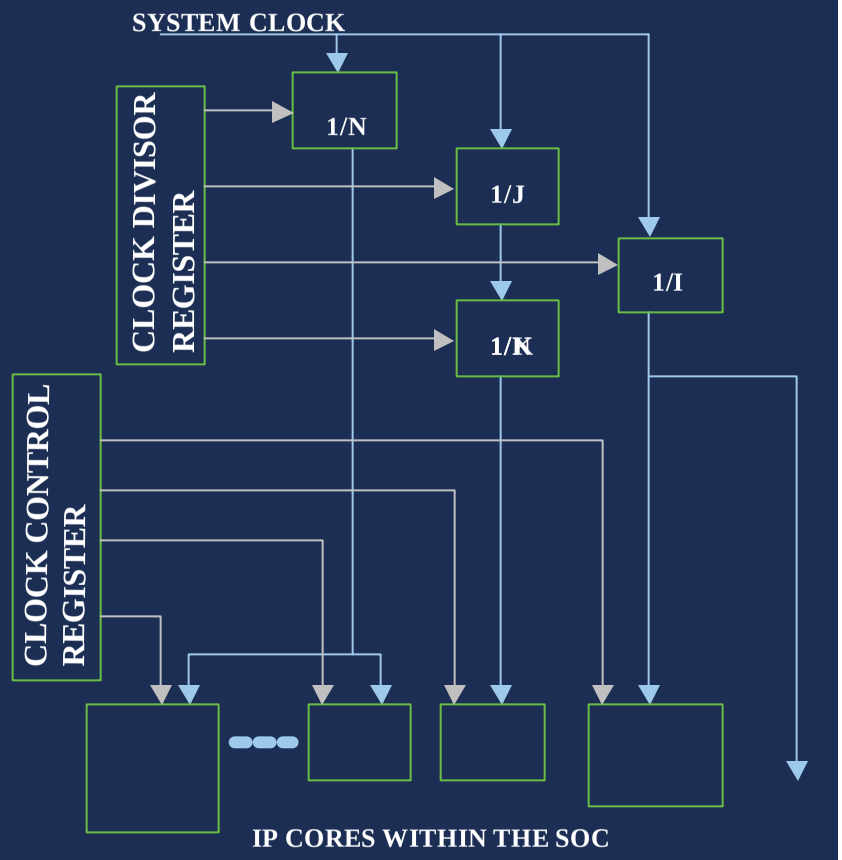
Clock distribution and clock gating used to reduce active power

Clock Domains

- On-chip clock distribution generates multiple synchronous phase aligned clock domains
- Support for dynamic frequency scaling via hazard free divisor selection

Clock Gating

- **IP core level** clock gating disables clocks to whole IP blocks that are not currently being used
- **Register level** clock gating disables clocks to unused portions of IP blocks during each operation or instruction cycle



PowerPC®

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Voltage Scalable Touch Panel Interface

New touch panel interface addresses unique low power challenges of analog sensor interfaces

Low Power Challenges

- Analog circuits do not benefit from CMOS voltage scaling
- Traditional A/D converters can be challenging to design at low VDD
- Protective voltage islands raise number of required supplies

Touch Panel Interface Features

- All digital CMOS solution based on an RC delay measurement
- Compatible with many standard resistive touch panels and other passive sensors
- Works over full logic voltage range
- Benefits of CMOS voltage scaling
- Provides up to 10-bits of resolution

PowerPC®

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Hardware Accelerators

Can increase performance or reduce overall active power

- Dedicated logic requires fewer cycles to execute algorithm than the main CPU
- Accelerators off load the CPU core allowing lower frequencies in both units
- Voltage scaling can be used in both hardware accelerator and CPU core

On-Chip Hardware Accelerators

Speech Language Accelerator

Targeted at embedded speech recognition software

Cryptography Accelerator

Supports DES and triple-DES encryption algorithms

CodePack™

Instruction compression to reduce system memory requirements

PowerPC®

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Active Power vs. Standby Power Tradeoffs

The V_{TH} Dilemma - Lowering the threshold voltage to reduce active power can increase standby/static power

Active Power

- Lower supply voltage significantly reduces active power (p = C Vdd^2 F)
- Threshold voltage limits the usable voltage range for complementary CMOS (Vdd / V_{TH})
- Lower threshold voltage (V_{TH}) allows a lower supply voltage and lower active power

Standby/Static Power

- Since devices are frequently idle, low standby power is important
- Higher threshold voltage (V_{TH}) reduces static leakage

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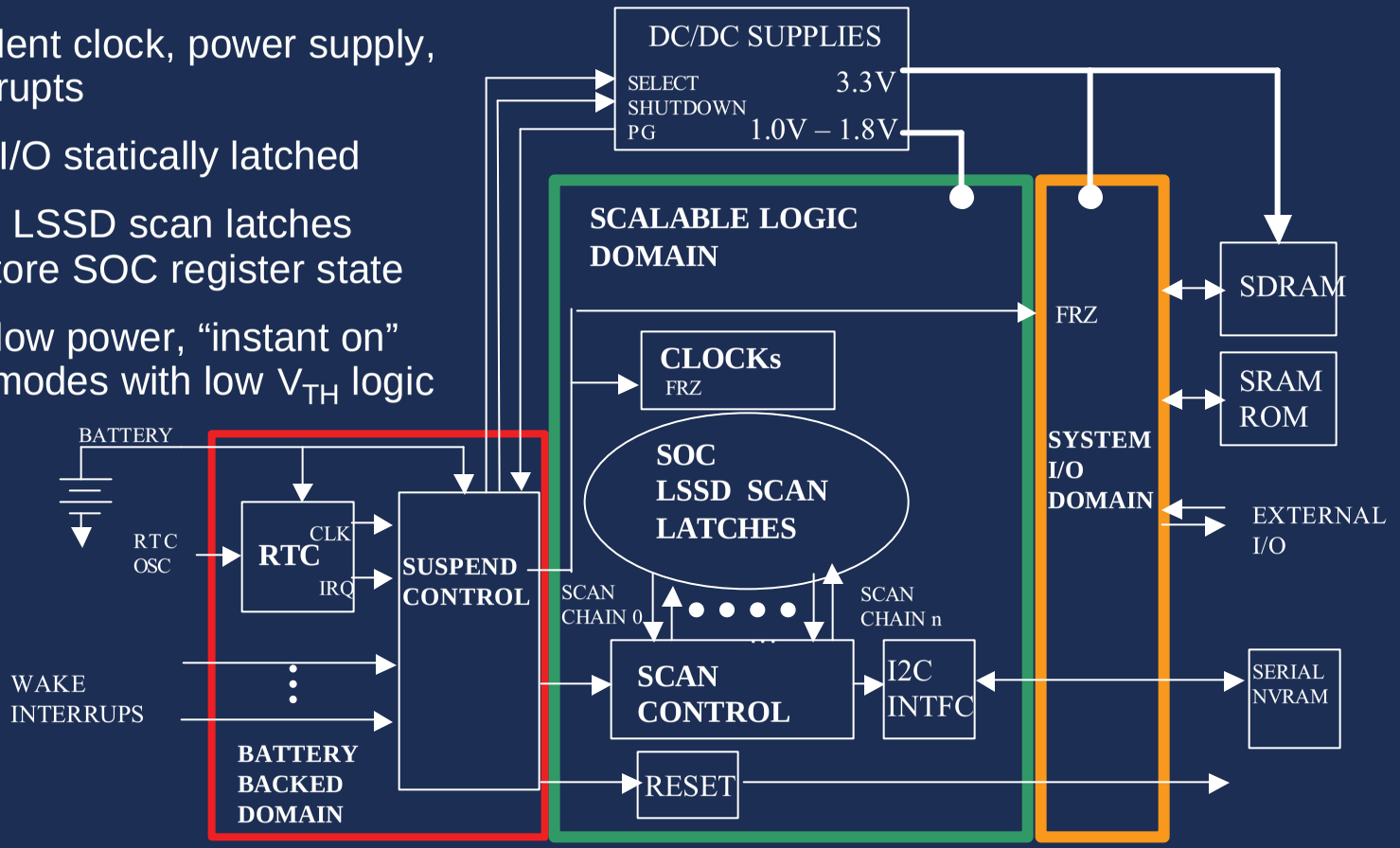
Standby Power Reduction

On-chip supervisory core manages standby/static power

Features

- Independent clock, power supply, and interrupts
- External I/O statically latched
- Standard LSSD scan latches save/restore SOC register state
- Enables low power, “instant on” standby modes with low V_{TH} logic



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Standby Power Modes

Standby power modes enable longer battery life and "instant on"

	System Clock	VDD Logic	State Saved	Restore Time	Power Logic
Freeze Mode	**0 Hz**	**1V**	**All**	**Write DCR Register (< 1uS)**	**CMOS Leakage at 1V**
Hibernation Mode	**0**	**0**	**Software State**	**OS Reboot (Seconds)**	**~0**
Cryo Mode	**0**	**0**	**Registers and Software State**	**"Instant On" – Scan Restore of State (100- 200 mS)**	**~0**

Cryo mode sequence

- Shutdown: Invalidate arrays ➔Clocks stopped ➔State scanned to IIC attached non-volatile storage ➔Power remove from logic
- Suspend: Monitor system for wake up condition or RTC timer
- Restore: On Wake indicator ➔Restore power to logic ➔State scanned in from non-volatile storage ➔Restore clocks

PowerPC®

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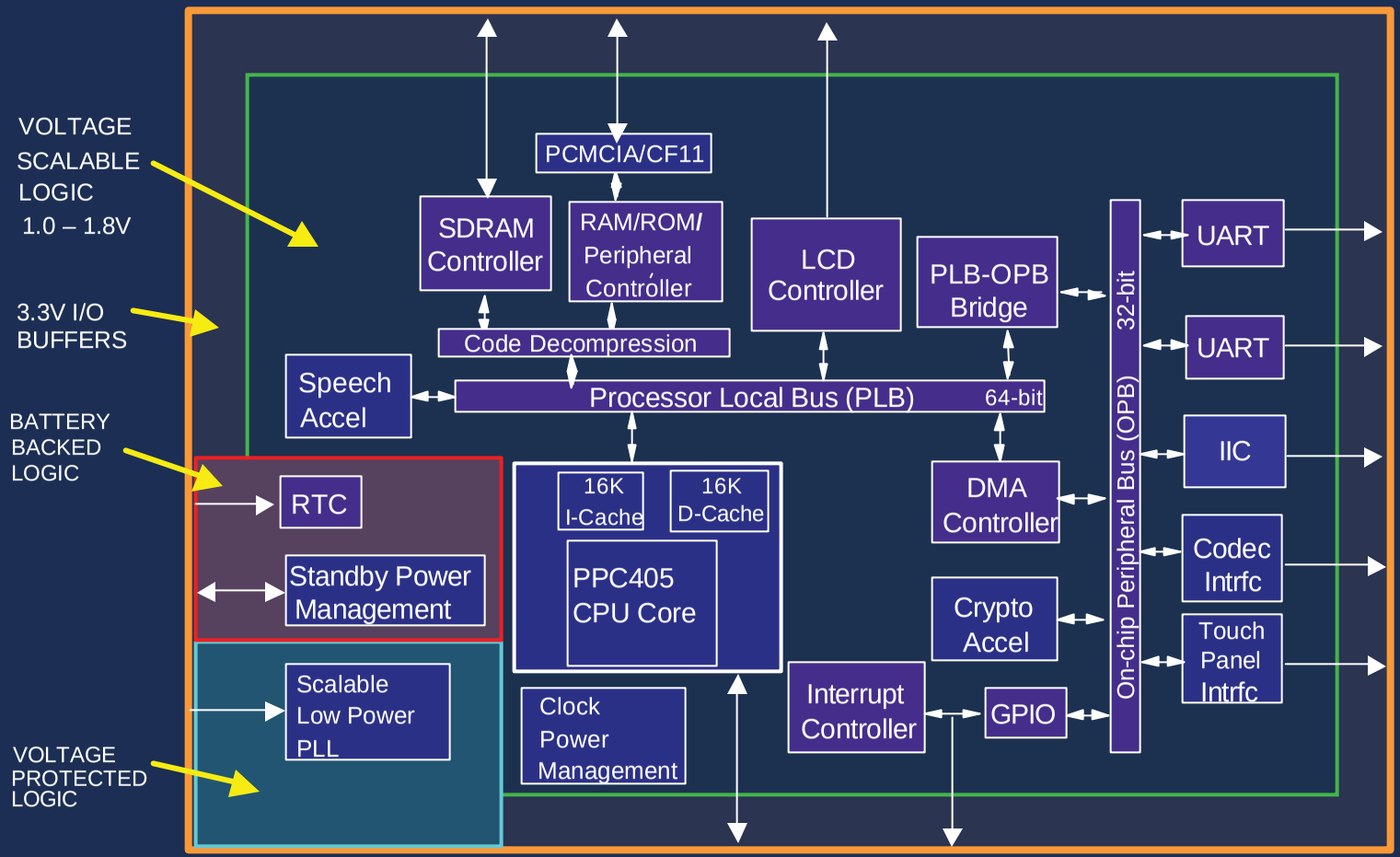
405LP Voltage Domains



PowerPC®

IBM®

CPU Core Specifications

Features

Architecture	32-bit PowerPC compliant, application code compatible with all IBM PowerPC processors
CPU/Caches	PPC405 16K I-Cache 16K D-Cache
Voltage	0.9V – 1.95V
Technology	0.18um, CMOS SA-27E

CPU Core/Caches Specifications

	TC1* (1.8V)	TC2* (1.0V)
Frequency	380 MHz	152 MHz
Performance (Dhrystone 2.1)	577 DMIPS	231 DMIPS
Typical Power (est.)	500 mW	53 mW
Performance/ Watt	1154 DMIPS/ W	4528 DMIPS/ W

* Notes: TC1 – Typical Conditions: 1.8V, 55C, Nominal Silicon
TC2 – Typical Conditions: 1.0V, 55C, Nominal Silicon

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What's Next?

- **Samples of 405LP SOC available to selected customers in 1Q '02**
- **Continuing innovation in low power techniques**
- **Developing highly integrated custom and standard SOCs based on these low power technologies**
- **For additional information:**
  - http://www.chips.ibm.com/products/powerpc/

The information above represents IBM's current business goals and objectives, but is subject to change or withdrawal at any time without advance notice.

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