IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

HSM PORTFOLIO LLC and TECHNOLOGY PROPERTIES LIMITED LLC, Plaintiffs; v. ELPIDA MEMORY INC., et al., Defendants.	Civil Action No. 11-770-RGA

MEMORANDUM OPINION

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February 11, 2016

Richard G. Andrews

ANDREWS, U.S. DISTRICT JUDGE:

Presently before the Court are Defendant Micron Technology, Inc.'s Motions for Summary Judgment of Noninfringement, Invalidity, and No Indirect Infringement (D.I. 1037, 1039, 1040) and Plaintiffs' Motion for Partial Summary Judgment that U.S. Patent No. 5,030,853 is Not Anticipated and is Not Indefinite (D.I. 1055). The issues have been fully briefed. (D.I. 1043, 1087, 1113, 1056, 1082, 1122). Oral argument was held on December 8, 2015. (D.I. 1163). For the reasons set forth herein, Micron's motion for summary judgment of non-infringement (D.I. 1037) is **GRANTED IN PART** and **DENIED IN PART**; Micron's motion for summary judgment of invalidity (D.I. 1039) is **DENIED**; Micron's motion for summary judgment of no indirect infringement (D.I. 1040) is **GRANTED IN PART** and **DENIED IN PART**; Plaintiffs' motion for partial summary judgment (D.I. 1055) is **GRANTED IN PART** and **DISMISSED AS MOOT IN PART**.

I. BACKGROUND

On September 1, 2011, HSM Portfolio and Technology Properties Limited LLC filed this patent infringement suit against Defendant Micron Technology, Inc. and other defendants. (D.I. 1). Micron is the only remaining defendant. (D.I. 1043 at 6). Plaintiffs allege that certain Micron DRAM and CMOS Image Sensor products infringe US Patent Nos. 5,001,367 (the "'367 patent"), 5,030,853 (the "'853 patent"), 5,247,212 (the "'212 patent"), and 5,391,949 (the "'949 patent") (collectively "patents-in-suit"). (D.I. 859 ¶¶ 77, 82, 105, 110, 127-28, 136-37). Plaintiffs further allege that Micron indirectly infringed the '853 and '949 patents by inducing and contributing to others' infringement. (*Id.* ¶¶ 77-81, 105-09; D.I. 1087 at 8).

On September 2, 2015, Micron filed its motions, requesting summary judgment of non-infringement with respect to all asserted claims of the patents-in-suit, anticipation with respect to

certain claims in the '853, '212, and '949 patents,[1] no indirect infringement,[2] and no damages with respect to certain products. (D.I. 1037, 1038, 1039, 1040). Also on September 2, 2015, Plaintiffs filed their motion, requesting summary judgment that the '853 patent is not anticipated with respect to certain prior art references and is not indefinite.[3] (D.I. 1055). On December 7, 2015, the Court denied Micron's motion for summary judgment of no damages. (D.I. 1038, 1161).

II. LEGAL STANDARDS

"The court shall grant summary judgment if the movant shows that there is no genuine dispute as to any material fact and the movant is entitled to judgment as a matter of law." Fed. R. Civ. P. 56(a). The moving party has the initial burden of proving the absence of a genuinely disputed material fact relative to the claims in question. *Celotex Corp. v. Catrett*, 477 U.S. 317, 330 (1986). Material facts are those "that could affect the outcome" of the proceeding, and "a dispute about a material fact is 'genuine' if the evidence is sufficient to permit a reasonable jury to return a verdict for the nonmoving party." *Lamont v. New Jersey*, 637 F.3d 177, 181 (3d Cir. 2011) (quoting *Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 248 (1986)). The burden on the moving party may be discharged by pointing out to the district court that there is an absence of evidence supporting the non-moving party's case. *Celotex*, 477 U.S. at 323.

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[1] While Micron originally sought summary judgment on anticipation of dependent claim 9 of the '853 patent (D.I. 1039, 1043), it has since withdrawn that position. (D.I. 1075).

[2] Plaintiffs originally opposed summary judgment of both contributory infringement and induced infringement. Plaintiffs informed the Court at oral argument, however, that after the Court's ruling with respect to Toshiba (D.I. 854), they would no longer contest summary judgment on the issue of contributory infringement. (D.I. 1163 at 112).

[3] Micron has informed the Court that it no longer intends to rely on the A35A Design ID as a prior art reference. (D.I. 1165). As a result, Plaintiffs' motion for partial summary judgment of non-anticipation is dismissed as moot with respect to the A35A Design ID. (*See* D.I. 1166).

The burden then shifts to the non-movant to demonstrate the existence of a genuine issue for trial. *Matsushita Elec. Indus. Co. v. Zenith Radio Corp.*, 475 U.S. 574, 586-87 (1986); *Williams v. Borough of West Chester, Pa.*, 891 F.2d 458, 460-61 (3d Cir. 1989). A non-moving party asserting that a fact is genuinely disputed must support such an assertion by: "(A) citing to particular parts of materials in the record, including depositions, documents, electronically stored information, affidavits or declarations, stipulations . . . , admissions, interrogatory answers, or other materials; or (B) showing that the materials cited [by the opposing party] do not establish the absence . . . of a genuine dispute . . . ." Fed. R. Civ. P. 56(c)(1).

When determining whether a genuine issue of material fact exists, the court must view the evidence in the light most favorable to the non-moving party and draw all reasonable inferences in that party's favor. *Scott v. Harris*, 550 U.S. 372, 380 (2007); *Wishkin v. Potter*, 476 F.3d 180, 184 (3d Cir. 2007). If the non-moving party fails to make a sufficient showing on an essential element of its case with respect to which it has the burden of proof, the moving party is entitled to judgment as a matter of law. *See Celotex*, 477 U.S. at 322.

A patent is infringed when a person "without authority makes, uses, offers to sell, or sells any patented invention, within the United States . . . during the term of the patent." 35 U.S.C. § 271(a). A two-step analysis is employed in making an infringement determination. *See Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 976 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996). First, the court must construe the asserted claims to ascertain their meaning and scope. *See id.* The trier of fact must then compare the properly construed claims with the accused infringing product. *See id.* at 976. This second step is a question of fact. *See Bai v. L & L Wings, Inc.*, 160 F.3d 1350, 1353 (Fed. Cir. 1998).

"Literal infringement of a claim exists when every limitation recited in the claim is found in the accused device." *Kahn v. Gen. Motors Corp.*, 135 F.3d 1472, 1477 (Fed. Cir. 1998). "If any claim limitation is absent from the accused device, there is no literal infringement as a matter of law." *Bayer AG v. Elan Pharm. Research Corp.*, 212 F.3d 1241, 1247 (Fed. Cir. 2000). If an accused product does not infringe an independent claim, it also does not infringe any claim depending thereon. *See Wahpeton Canvas Co. v. Frontier, Inc.*, 870 F.2d 1546, 1553 (Fed. Cir. 1989). However, "[o]ne may infringe an independent claim and not infringe a claim dependent on that claim." *Monsanto Co. v. Syngenta Seeds, Inc.*, 503 F.3d 1352, 1359 (Fed. Cir. 2007) (internal quotations omitted). A product that does not literally infringe a patent claim may still infringe under the doctrine of equivalents if the differences between an individual limitation of the claimed invention and an element of the accused product are insubstantial. *See Warner–Jenkinson Co. v. Hilton Davis Chem. Co.*, 520 U.S. 17, 24 (1997). The doctrine of equivalents must be applied to the "individual elements of the claim, not to the invention as a whole." *Id.* at 29. An accused element is equivalent if the differences between the element and the claim limitation are "insubstantial." *Zelinski v. Brunswick Corp.*, 185 F.3d 1311, 1316 (Fed. Cir. 1999). An accused element may be found to be equivalent if it performs substantially the same function in substantially the same way to obtain substantially the same result as the claim limitation. *See Graver Tank & Mfg. Co. v. Linde Air Prods. Co.*, 339 U.S. 605, 608 (1950). The patent owner has the burden of proving infringement and must meet its burden by a preponderance of the evidence. *See SmithKline Diagnostics, Inc. v. Helena Lab. Corp.*, 859 F.2d 878, 889 (Fed. Cir. 1988) (citations omitted).

When an accused infringer moves for summary judgment of non-infringement, such relief may be granted only if at least one limitation of the claim in question does not read on an

element of the accused product, either literally or under the doctrine of equivalents. *See Chimie v. PPG Indus., Inc.*, 402 F.3d 1371, 1376 (Fed. Cir. 2005); *see also TechSearch, L.L.C. v. Intel Corp.*, 286 F.3d 1360, 1369 (Fed. Cir. 2002) ("Summary judgment of noninfringement is . . . appropriate where the patent owner's proof is deficient in meeting an essential part of the legal standard for infringement, because such failure will render all other facts immaterial."). Thus, summary judgment of non-infringement can only be granted if, after viewing the facts in the light most favorable to the non-movant, there is no genuine issue as to whether the accused product is covered by the claims (as construed by the court). *See Pitney Bowes, Inc. v. Hewlett–Packard Co.*, 182 F.3d 1298, 1304 (Fed. Cir. 1999).

"The presumption of a patent's validity under 35 U.S.C. § 282 can be rebutted by clear and convincing evidence." *Allergan, Inc. v. Apotex Inc.*, 754 F.3d 952, 958 (Fed. Cir. 2014). A patent claim is invalid as anticipated under 35 U.S.C. § 102 if "within the four corners of a single, prior art document . . . every element of the claimed invention [is described], either expressly or inherently, such that a person of ordinary skill in the art could practice the invention without undue experimentation." *Callaway Golf Co. v. Acushnet Co.*, 576 F.3d 1331, 1346 (Fed. Cir. 2009) (alterations in original). As with infringement, the court construes the claims and compares them against the prior art. *See Enzo Biochem, Inc. v. Applera Corp.*, 599 F.3d 1325, 1332 (Fed. Cir. 2010). "While anticipation is a question of fact, it may be decided on summary judgment if the record reveals no genuine dispute of material fact." *Encyclopaedia Britannica, Inc. v. Alpine Elecs. of Am., Inc.*, 609 F.3d 1345, 1349 (Fed. Cir. 2010).

III. ANALYSIS

A. '853 Non-Infringement

The '853 patent relates to a buffer, a chain of inverters which allows smaller circuit elements to efficiently communicate with larger circuit elements. (D.I. 1047, Ex. 3 ¶ 101, Ex. 5 ¶ 15). The asserted claims[4] require that each inverter in this chain of inverters increase in size by "less than a predetermined factor times the width of the N-channel of the immediately preceding inverter stage." '853 patent at 27:65-28:2. In claim construction, the Court held that the "predetermined factor" (also known as "*K*") is to be "calculated using Equation (37) in the specification." (D.I. 729 at p. 1). The Court expressly found that "the patentee intended Equation 37, and only that equation, to define the 'predetermined factor.'" (D.I. 715 at p. 5). For purposes of proving infringement, however, it is irrelevant whether Equation (37) was actually used during the design process of an accused product. (*See id.*). The patent is directed at an apparatus, not a method or process.[5] (*See id.*). The patent requires only that the predetermined factor limitation is satisfied when one solves for *K* using Equation (37). Put another way, after determining *K* using Equation (37), the predetermined factor limitation of claim 1 is satisfied when the channel width of the N-channel field effect transistor is less than *K* times the channel width of the N-channel field effect transistor in the immediately preceding inverter stage. For purposes of the present motion, it is important to note that Equation (37)

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[4] Plaintiffs assert that Micron products embodying 26 Design IDs infringe claims 1-4 and 6-9. (D.I. 1047, Ex. 4; D.I. 1043 at 8). Claim 1 is the only asserted independent claim. '853 patent at 27:49-28:52.

[5] This is consistent with the Court's dicta from the claim construction opinion, which both parties frequently cite. There, the Court noted that "a statement of how to design the chip does not limit the claims to that design process" and "[t]he fact that the specification describes one method of ending up at the final product does not limit the claims to using only that method." (D.I. 715 at p. 5). Whether a party was even aware of Equation (37) is irrelevant to infringement. Without evidence of a desired rise time, however, it appears to be difficult to prove infringement, given the nature of Equation (37). But, as the Court noted at claim construction, "[t]here is no canon of claim construction that prefers an 'easy to prove infringement' construction." (D.I. 715 at p. 5); *see also White v. Dunbar*, 119 U.S. 47, 52 (1886) ("The claim is a statutory requirement, prescribed for the very purpose of making the patentee define precisely what his invention is; and it is unjust to the public . . . to construe it in a manner different from the plain import of its terms.").

includes the variable T_{rise}, which represents "desired rise time." '853 patent at 17:44-53. The parties agree that "desired rise time" represents the goal or target of the designer. (D.I. 677 at 74, D.I. 1088, Ex. B ¶ 129; D.I. 1163 at 34).

To prove infringement, Plaintiffs do not use Equation (37) as it appears in the patent in order to calculate *K*. Instead, Plaintiffs' infringement expert, Dr. Foty, uses a different equation: the "algebraically-reduced expression for *K*." (D.I. 1087 at 10; D.I. 1047, Ex. 1 ¶ 150). Dr. Foty arrives at this equation by "substituting other equations from the '853 patent, canceling certain variables, and making appropriate simplifications based on the particular characteristics of Micron's products." (D.I. 1087 at 10; *see* D.I. 1047, Ex. 31 at 5-8). In his report, Dr. Foty opines that his equation "is the same as, or mathematically equal to, Equation 37, but can be solved using different variables." (D.I. 1047, Ex. 1 ¶ 152).

Micron argues that Plaintiffs do not use Equation (37) to show literal infringement, and therefore Plaintiffs have failed to produce evidence from which a reasonable juror could conclude that Micron literally infringes. (D.I. 1043 at 9-10). Additionally, Micron contends that no reasonable jury could conclude that the "algebraically-reduced expression for *K*" is equivalent to Equation (37) under the doctrine of equivalents. (*Id.* at 10-13).

i. Literal Infringement

The '853 patent presents a peculiar problem. While the asserted claims are directed to an apparatus—rather than a method or process—the predetermined factor limitation implies a temporal limitation. That is, the prefix "pre-" in predetermined suggests that the factor must at least be capable of determination before some other event occurs. Were it capable of being determined at any time, the word "predetermined" would have no purpose at all. Since the predetermined factor sets the maximum N-channel transistor widths in each inverter stage,

Equation (37) must be capable of solution (to arrive at the predetermined factor *K*) before transistor channel widths are determined. It necessarily follows that the predetermined factor must be capable of determination during the design phase of the circuit. *See, e.g.*, *Pause Tech. LLC v. TiVo Inc.*, 419 F.3d 1326, 1335-36 (Fed. Cir. 2005) (finding that a "predetermined duration" of signals must be "determined prior to operation"). This temporal limitation is confirmed by the existence of the T_{rise} ("desired rise time") variable. The patent instructs a designer to use a desired rise time (a prefabrication goal or objective) in the equation to arrive at a factor, which then serves to set the maximum N-channel transistor widths in each inverter stage.

In arriving at the algebraically-reduced expression for *K*, Dr. Foty—in step 2 of his derivation—replaces desired rise time with the specification's Equation (15), which defines "rise time (Seconds)" or actual rise time. (D.I. 1047, Ex. 31 at 5; D.I. 1088, Ex. B ¶¶ 129-30); '853 patent at 11:64-12:26. In justifying this substitution, Dr. Foty states that "once a circuit is finished, the desired rise time becomes the actual rise time of the circuit" and that "[w]hether or not Micron conceived of a specific desired rise time before designing its circuits is irrelevant because all circuits have an actual rise time." (D.I. 1088, Ex. B ¶¶ 128-130). That parties agree that all circuits have an actual rise time. As Plaintiffs have before argued, however, that does not necessarily mean that desired rise time and actual rise time are interchangeable. As Plaintiffs' correctly argued during claim construction:

> Equation (37) involves a number of variables that would be readily available during the design process but that may not be available when analyzing a finished product. For example, the T_{rise} variable 'is the desired rise time.' . . . Obviously, the desired rise time could only be available to the designer of a finished product, whereas specific rise time (i.e., actual rise time) could be determined from a finished product.

(D.I. 677 at 74 (emphasis omitted)).[6] If actual rise time were always equal to desired rise time, this would be a distinction without difference. Further, Plaintiffs' invalidity expert—Mr. Salmon—conceded that a desired rise time may not exist at all for a particular node in a circuit. (D.I. 1047, Ex. 8 at 46). Indeed, Micron explains—and Plaintiffs apparently do not dispute—that it does not use a desired rise time at all in its process. (D.I. 1113 at 7; D.I. 1047, Ex. 5 ¶¶ 22-23, 31). Because Dr. Foty's conclusion that desired rise time and actual rise time are always identical fails to find any support in the record and contravenes previous representations made by Plaintiffs to this Court, "no reasonable jury could accord [it] evidentiary weight" and it is therefore disregarded. *See Jiminez v. All Am. Rathskeller, Inc.*, 503 F.3d 247, 253-55 (3d Cir. 2007); *see also St. Clair Intellectual Prop. Consultants, Inc. v. Matsushita Elec. Indus. Co.*, 2012 WL 1015993, at *12 (D. Del. Mar. 26, 2012), *aff'd,* 522 F. App'x 915 (Fed. Cir. 2013) (rejecting "expert affidavit" that conflicted with court's claim construction). In order for an accused product to meet the predetermined factor limitation, it must satisfy K when K is calculated using Equation (37). Because Plaintiffs' algebraically-reduced expression for K substitutes actual rise time for desired rise time, it is not the same mathematical equation. Plaintiffs' infringement theory is therefore inconsistent with the Court's claim construction order and fails to create a genuine dispute as to whether Micron literally infringes.

Even putting aside the substitution of actual rise time for desired rise time, Dr. Foty's algebraically-reduced expression for K fails to show literal infringement for another independent reason. Dr. Foty—in step 10 of his derivation—declares that "[b]ecause the length of the

[6] This does not mean that the desired rise time is only known to the designer. Dr. Foty concedes that there are "a wide [number] of ways that engineers define their design goals that they're going to then meet with their designs" and that the "desired rise time" may be recorded in "lab notebooks," "product spec[ifications]," or "an engineering meeting, transcript or result." (D.I. 1047, Ex. 6 at 133).

interconnect L_{cs} is negligible," the expression ($1+L_{cs}/\alpha_o L_{os}$) yields ($1+0/\alpha_o L_{os}$). (D.I. 1047, Ex. 31 at 8). Then, since zero over anything equals zero, the expression ultimately yields 1. (*Id.*). In reaching this "simplif[ication]," Dr. Foty opines that because the accused products have an "interconnect length [that] is so small as to be negligible," one can "simplify" Equation (37) by setting the interconnect length variable to zero. (D.I. 1088, Ex. C at 4). It is undisputed that Dr. Foty takes a number with a positive value—that may be "very small"—and treats it as zero. But the interconnect length is not zero, as Dr. Foty concedes, and therefore this "simplify[ing]" step cannot possibly be described as merely an algebraic substitution, the result of which would render the algebraically-reduced expression for *K* mathematically identical to Equation (37). Therefore, Plaintiffs' infringement theory is inconsistent with the Court's claim construction order for this additional reason.

The patent requires—as the Court has previously held—that for a product to infringe, it must satisfy the predetermined factor limitation, when the predetermined factor is calculated using Equation (37). As stated above, there are two independent reasons for concluding that the algebraically-reduced expression for *K* is not Equation (37). Plaintiffs' infringement theory thus fails to create a genuine dispute of fact. Micron is entitled to summary judgment of no literal infringement of the '853 patent.

ii. Doctrine of Equivalents

While Plaintiffs contend that the algebraically-reduced expression for *K* is mathematically identical to Equation (37), they argue in the alternative that the algebraically-reduced expression for *K* is equivalent to Equation (37). (D.I. 1087 at 14-15). Plaintiffs argue that a reasonable juror could conclude that the differences between calculating *K* with Equation (37) and with the algebraically-reduced expression for *K* are insubstantial, and therefore Micron

can be found to infringe under the doctrine of equivalents. (*Id.*). Micron argues that Equation (37) necessarily "require[s] the use of information that was generated before the circuit was made, including the 'desired rise time' of the buffer," and an equation that "depends on information that is available after the circuit was made" does not serve the same function, and is therefore "substantially different." (D.I. 1043 at 10-11 (emphasis omitted)).

In support of its argument, Micron relies on cases pertaining to the "doctrine of vitiation." (*Id.*). This doctrine, generally speaking, "'is nothing more than a conclusion that the evidence is such that no reasonable jury could conclude that an element of an accused device is equivalent to an element called for in the claim, or that the theory of equivalence to support the conclusion of infringement otherwise lacks legal sufficiency.'" *Cadence Pharms. Inc. v. Exela PharmSci Inc.*, 780 F.3d 1364, 1371 (Fed. Cir. 2015) (quoting *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1018-19 (Fed. Cir. 2006)). "Claim vitiation applies when there is a 'clear, substantial difference or a difference in kind' between the claim and the accused product." *See Trading Techs. Int'l, Inc. v. eSpeed, Inc.*, 595 F.3d 1340, 1355 (Fed. Cir. 2010) (quoting *Freedman Seating Co. v. Am. Seating Co.*, 420 F.3d 1350, 1360 (Fed. Cir. 2005)).

Micron argues an equation that determines a scaling factor after a circuit has been created cannot be equivalent to an equation which determines a scaling factor before a circuit has been created, as such a finding would vitiate the "predetermined" aspect of the predetermined factor limitation. Put another way, Micron argues the algebraically-reduced expression for K cannot be equivalent, because "after is opposite of before, not equivalent." *See Planet Bingo, LLC v. GameTech Int'l, Inc.*, 472 F.3d 1338, 1344 (Fed. Cir. 2006); *see also Lockheed Martin Corp. v. Space Sys./Loral, Inc.*, 324 F.3d 1308, 1321 (Fed. Cir. 2003). Micron is correct. Plaintiffs' algebraically-reduced expression for K purportedly determines K, but actually arrives at a factor

entirely different in kind. The patent goes to great lengths to describe how to arrive at Equation (37) and how its result—the predetermined factor—is used in the claimed invention. *See, e.g.*, '853 patent at 7:56-18:17, 27:65-28:2. "[W]here the patent document expressly identifies a role for a claim limitation, the doctrine of equivalents cannot be used to capture subject matter that does not substantially fill that role." *K-2 Corp v. Salomon S.A.*, 191 F.3d 1356, 1367 (Fed. Cir. 1999). An equation that arrives at a scaling factor based on information that is derived from a completed circuit—though ideal for proving infringement—is not, as a matter of law, equivalent to an equation which utilizes prefabrication information to arrive at a predetermined factor. This would read "predetermined" out of the claims. With an equation that is not equivalent to Equation (37), Plaintiffs reach a factor that is not equivalent to the predetermined factor described in the patent. Therefore, Plaintiffs have failed to present evidence sufficient to show that the accused products meet the predetermined factor limitation under the doctrine of equivalents. Micron is entitled to summary judgment of no doctrine of equivalents infringement of the '853 patent.

B. '853 Anticipation

Micron seeks summary judgment on anticipation of the '853 patent only "[i]f . . . the Court were to permit Plaintiffs to use Plaintiffs' Equation to prove infringement." (D.I. 1043 at 8). In other words, Micron contends there is no genuine dispute that the Proebsting reference anticipates Claims 1, 7, and 9 of the '853 patent "under Plaintiffs' infringement theories." (D.I. 1043 at 14). "It is axiomatic that claims are construed the same way for both invalidity and infringement." *Amgen Inc. v. Hoechst Marion Roussel, Inc.*, 314 F.3d 1313, 1330 (Fed. Cir. 2003); *see also Digital Reg of Tex., LLC v. Adobe Sys., Inc.*, 2014 WL 4090550, at *11 (N.D. Cal. Aug. 19, 2014) ("[T]he same claim scope must be applied to infringement and validity."

(citing *Tate Access Floors, Inc. v. Interface Architectural Res., Inc.*, 279 F.3d 1357, 1367 (Fed. Cir. 2002))). The Court has concluded that Plaintiffs infringement theory fails as a matter of law. Therefore, the basis for Micron's summary judgment on anticipation is a nullity. Accordingly, summary judgment is denied.

C. '212 Non-Infringement

The asserted claims[7] of the '212 patent are directed to a clocked latch. Generally, a semiconductor latch stores a logical value after being set to do so by an input. (D.I. 1047, Ex. 5 at 15-16). Independent claim 22 requires an arrangement of field effect transistors ("FETs") in which "the control electrodes of said third and fifth FETs [are] connected together for receiving a clock input signal." '212 patent at 17:11-13. At claim construction, the Court construed "clock input signal" as "a periodic signal with a constant frequency used for synchronization." (D.I. 729 at p. 3). Micron argues that its accused circuits do not include FETs capable of receiving a "clock input signal" and also do not include the claimed complementary "inverter." (D.I. 1043 at 17). Therefore, Micron argues, it does not literally infringe as a matter of law. Micron also contends that Plaintiffs have failed to show a dispute of material fact as to whether the accused "clock input signal" and the accused "inverter" are equivalent under the doctrine of equivalents. (D.I. 1043 at 21-22, 23-24).

i. Literal Infringement

a. Clock Input Signal

The parties first dispute the meaning of "for receiving a clock input signal." (D.I. 1087 at 21-25; D.I. 1043 at 19-20; D.I. 1113 at 10-11); *see* '212 patent at 17:12-13. Plaintiffs argue that

[7] Plaintiffs allege that products embodying twenty-seven Design IDs infringe claims 22 and 23 of the '212 patent. (D.I. 1047, Ex. 10; D.I. 1043 at 17). Claim 22 is the only asserted independent claim. '212 patent at 16:63-17:26.

"[e]ven if [the identified clock signals] are not, technically, clock input signals, all [they] needed to do is show capability." (D.I. 1087 at 24-25; D.I. 1163 at 68-69). Micron responds that "'capability' is not the standard" and even if it were, "[a]n argument that those circuits in the abstract could be used in products with a 'clock input signal' . . . is not sufficient to find infringement." (D.I. 1043 at 19-20)

Plaintiffs are correct that "apparatus claims cover what a device is, not what a device does." *Paragon Solutions, LLC v. Timex Corp.*, 566 F.3d 1075, 1090 (Fed. Cir. 2009). To prove infringement, Plaintiffs are not required to show that the accused circuits were actually used in any particular way, or that they were even used at all. To infringe an apparatus claim that recites capability, however, an accused device must be "capable of operating in the described mode." *Finjan, Inc. v. Secure Computing Corp.*, 626 F.3d 1197, 1204 (Fed. Cir. 2010) (internal quotations omitted). In other words, the device, as made or sold, must be "reasonably capable of satisfying the claim limitations." *Id.*; *see also Fantasy Sports Props., Inc. v. Sportsline.com, Inc.*, 287 F.3d 1108, 1117-18 (Fed. Cir. 2002). A "device does not infringe simply because it is possible to alter it in a way that would satisfy all the limitations of a patent claim." *High Tech Med. Instrumentation, Inc. v. New Image Indus., Inc.*, 49 F.3d 1551, 1555 (Fed. Cir. 1995); *see also Fantasy Sports*, 287 F.3d at 1118.

Here, the "for receiving a clock input signal" limitation describes the capability of the FETs. *See Ericsson, Inc. v. D-Link Sys., Inc.*, 773 F.3d 1201, 1216-17 (Fed. Cir. 2014) (discussing how "for preventing," "for arranging," and "for obtaining" are examples of claim limitations describing capabilities). That capability defines what the apparatus is, not merely what it does. *See Paragon Solutions*, 566 F.3d at 1090. For claims reciting capability, however, it is not enough to say that the third and fifth FETs could, in some abstract configuration, receive

a clock input signal. *See High Tech Med.*, 49 F.3d at 1555. An FET is not capable of receiving a clock input signal if there is no clock input signal to receive. Therefore, in order to satisfy the capability expressed in the claim, it must be that the case that a clock input signal exists in the accused products. Without a clock input signal, the accused products could not possibly be "reasonably capable of satisfying the claim limitations." *Finjan*, 626 F.3d at 1204.

Having established that, in order to infringe, the accused products must have a clock input signal, the Court must determine whether the signals identified by Plaintiffs are indeed clock input signals. Plaintiffs contend that "[a]ll of the signals connected to the third and fifth FETs will be active at least once" and that during that period, "the signals have a constant frequency and synchronize the output of the logic cell with the logic input signal and the clock input signal." (D.I. 1087 at 24; D.I. 1089 ¶¶ 27-29). Plaintiffs argue this is consistent with the Court's construction of clock input signals, as that construction did not require that the clock input signals "have multiple pulses." (D.I. 1087 at 24; D.I. 1089 ¶ 28). In support of this argument, Plaintiffs point to Figure 12B of the patent, which they posit is "the only embodiment describing the operation of the asserted claims" and "which shows a clock as a single pulse having a constant frequency over a single period." (D.I. 1087 at 24 (emphasis omitted)).

Plaintiffs' infringement theory is at odds with the Court's claim construction. The existence of the terms "periodic" and "frequency" within the Court's construction requires that there be more than one pulse. This was acknowledged by the parties during claim construction, as they disputed only whether the patent required that the frequency of the pulses be constant and whether they must be used for synchronization. (*See* D.I. 677 at 105-06, 108). If there is only one pulse, there is nothing "periodic" at all. Without more than one occurrence (of a pulse), there is no interval, and thus nothing to be constant or irregular. Even Dr. Foty concedes this in

his infringement report, stating that "[t]he word 'periodic' can be defined as 'occurring repeatedly from time to time.'" (D.I. 1088, Ex. E at 22 n.217 (citing http://www.merriam-webster.com/dictionary/periodic)). Plaintiffs' reference to Figure 12B is unavailing. *See* '212 patent fig.12B. Besides this being an attempt to reargue claim construction, it is clear that Figure 12B is a snapshot in time, of one pulse of the periodic clock signal. The patent itself notes Figure 12B shows that "any positive signal applied to the input of this circuit is latched at the output during the clock pulse *interval* regardless of whether the input signal drops during or after the clock pulse *interval*." *Id.* at 11:40-43 (emphasis added). An interval may be defined as "[t]he period of time between two events, actions, etc." or "[t]he space of time intervening between two points of time." *interval, n.*, Oxford English Dictionary (Dec. 2015), http://www.oed.com/view/Entry/98410. If the patentee considered 12B an embodiment with only one pulse, this reference to intervals would be nonsensical. With this understanding in mind, the Court held at claim construction that the interval of separation between pulses "must have a constant frequency." (D.I. 715 at p. 13).

Plaintiffs further argue that "each of [the targeted] signals will activate during at least one mode of operation of the accused products" and therefore "all of the signals . . . will activate at least once." (D.I. 1089 ¶¶ 27, 29). Dr. Foty then opines that for any "non-fixed" signal, "a time window can be defined as representing a time period for that signal; that window defines a mathematical period for the signal – and the signal will repeat for multiple repetitions of that window." (*Id.* ¶ 29). To put it modestly, this contorts the court's claim construction holding beyond what is permissible. By virtue of requiring a periodic signal, the Court held that the clock input signal must have multiple pulses with intervals between those pulses. (D.I. 715 at pp. 11-13). Resolving a dispute between the parties, the Court held that these intervals occur at a

"constant frequency."[8] (*Id.* at p. 12). Plaintiffs have not identified a signal that satisfies this construction and thus, necessarily, have not shown the capability of receiving it. Therefore, Plaintiffs have not advanced sufficient evidence to allow a reasonable juror to conclude that the accused products have third and fifth FETs capable of receiving a periodic signal with a constant frequency used for synchronization.

b. Complementary Inverters

For all but two[9] of the accused products, Micron moves for summary judgment on an independent ground of non-infringement. (D.I. 1043 at 22-23). Micron contends that the accused products do not contain the "complementary FET inverter" required by claims 22 and 23. (*Id.*).

For purposes of this issue, it is important to note that the "reasonably capable" standard discussed above applies "only to claim language that specifies that the claim is drawn to capability." *Ball Aerosol & Specialty Container, Inc. v. Limited Brands, Inc.*, 555 F.3d 984, 994 (Fed. Cir. 2009). In the absence of a claim describing capability, infringement requires "specific instances of direct infringement or that the accused device necessarily infringes the patent in suit." *ACCO Brands, Inc. v. ABA Locks Mfr. Co.*, 501 F.3d 1307, 1313 (Fed. Cir. 2007). When "it is clear" that the accused device "does not necessarily have to be placed in the infringing configuration," in order to prove infringement, there must be evidence that the device was actually "placed in the infringing configuration." *See Ball Aerosol*, 555 F.3d at 995.

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[8] The claim construction opinion states: "Plaintiffs argue that a 'clock input signal' refers to periodic signals sent by a clock circuit. Defendants agree. However, the parties dispute if the periodic signals must have a constant frequency." (D.I. 715 at p. 12; *see also* D.I. 677 at 108).

[9] Since Dr. Foty identifies an inverter within Design IDs F26A and F37Z, Micron does not pursue summary judgment for those IDs. (D.I. 1043 at 22; D.I. 1047, Ex. 5 at 21).

Here, Dr. Foty rests his opinion on the premise that an ordinary-skilled artisan "would understand 'complementary FET inverter' to mean a 'circuit that is capable of performing an inversion function' using CMOS (or an equivalently-'complementary') circuit technology." (D.I. 1089 ¶ 35). Dr. Foty then goes on to explain how, given certain circumstances, the NAND and NOR gates identified in the accused circuits would function as an inverter. (*Id.* ¶¶ 35-39; D.I. 1047, Ex. 1 ¶¶ 542-44). His analysis, however, is contrary to the law. The asserted claim comprises certain components, including an "inverter." Plaintiffs cannot make a showing of infringement by merely asserting that the accused device is capable of comprising one of the structural limitations. *See Cross Med. Prods. v. Medtronic Sofamor Danek, Inc.*, 424 F.3d 1293, 1311-12 (Fed. Cir. 2005) (holding that where a claim does not express capability, but instead a structural limitation, the plaintiff must show that the accused device "meet[s] all of the structural limitations"). Dr. Foty explains how the accused NOR and NAND gates could be configured to perform an inversion function, but advances no evidence that the accused products necessarily had this configuration. Since showing that the devices are capable of infringement is not enough, Plaintiffs' infringement theory fails as a matter of law. *See Ball Aerosol*, 555 F.3d at 994-95. Therefore, since Plaintiffs' evidence does not create a disputed material fact in regard to the "clock input signal" or the "complementary inverter" limitations, Micron is entitled to summary judgment as to no literal infringement of the '212 patent.

ii. Doctrine of Equivalents

Plaintiffs contend that, even if the accused products do not literally infringe the "clock input signal" or "complementary FET inverter" limitations, they infringe under the doctrine of equivalents. (D.I. 1087 at 25-28). Specifically, Plaintiffs argue that the signals identified by Plaintiffs are equivalent to "clock input signals" and that the identified NAND and NOR gates

are equivalent to "complementary inverters." (*Id.*). For both claim limitations, Micron argues that Plaintiffs are precluded from advancing their doctrine of equivalents theory because of the disclosure-dedication rule. (D.I. 1043 at 21-24).

The disclosure-dedication rule provides that "when a patent drafter discloses but declines to claim subject matter, . . . this action dedicates that unclaimed subject matter to the public." *Johnson & Johnston Assocs. Inc. v. R.E. Serv. Co.*, 285 F.3d 1046, 1054 (Fed. Cir. 2002) (en banc). "[T]he disclosure must be of such specificity that one of ordinary skill in the art could identify the subject matter that had been disclosed and not claimed." *PSC Computer Prods., Inc. v. Foxconn Int'l, Inc.*, 355 F.3d 1353, 1360 (Fed. Cir. 2004). Further, "before unclaimed subject matter is deemed to have been dedicated to the public, that unclaimed subject matter must have been identified by the patentee as an alternative to a claim limitation." *Pfizer, Inc. v. Teva Pharms. USA, Inc.*, 429 F.3d 1364, 1379 (Fed. Cir. 2005). The disclosure-dedication rule is a question of law to be decided by the Court. *See Toro Co. v. White Consol. Indus., Inc.*, 383 F.3d 1326, 1331 (Fed. Cir. 2004); *see also SanDisk Corp. v. Kingston Tech. Co.*, 695 F.3d 1348, 1364 (Fed. Cir. 2012). Therefore, whether the disclosure-dedication rule "legally foreclose[s] any scope of equivalency" is an issue appropriate for determination on summary judgment. *See Zircon Corp. v. The Stanley Works*, 713 F. Supp. 2d 881, 896 (N.D. Cal. 2010).

Micron argues that the patentee cannot assert that a "logic signal" is equivalent to a clock input signal "because the 212 Patent discloses, but does not claim, circuits for receiving non-clock signals." (D.I. 1043 at 21). In so arguing, Micron relies on Figures 3 and 8 of the patent, along with the patentee's statement that "[t]he clocked CLIP AND logic circuit 30 of FIG. 8 is identical to the unclocked AND circuit of FIG. 3 except one of the inputs 12 is a 'clock' input, for receiving a clock signal instead of a logic input signal." (*Id.*); '212 patent at 9:68-10:4.

According to the patent, Figure 3 shows "a schematic circuit diagram of a CLIP AND logic circuit," and Figure 8 shows "a schematic circuit diagram of a clocked CLIP AND gate." '212 patent at 4:36-37, 4:47-48. Claim 22, however, is directed at "[a] latching complementary logic input parallel (CLIP) field effect transistor (FET) output logic cell." *Id.* at 16:63-64. The only figure which embodies claim 22 appears to be Figure 12A, which the specification describes as "a schematic circuit diagram of a latching CLIP output logic cell." *Id.* at 4:59-61. The embodiments of Figures 3 and 8 seem to be claimed in claims 4 and 5, which are directed at a "CLIP AND circuit" and a "clocked CLIP circuit," respectively. *Id.* at 15:5-16. Thus, the "unclaimed alternative" embodiment may not be unclaimed at all. Even if this were not the case, however, the specification provides no indication whatsoever that some aspect of the unclocked "CLIP AND logic circuit" of Figure 3 serves as an alternative to the clock limitation of the CLIP output logic cell of claim 22. The disclosure-dedication rule does not provide "that any generic reference in a written specification necessarily dedicates all members of that particular genus to the public." *PSC Computer Prods.*, 355 F.3d at 1360. The '212 patent does not identify the unclocked circuit of Figure 3 as an unclaimed alternative to any limitation of claim 22. *See Pfizer*, 429 F.3d at 1379. Therefore, the disclosure-dedication rule does not apply.

Micron's disclosure-dedication argument pertaining to NAND and NOR gates fares no better. In this instance, Micron notes that the specification discusses AND, OR, NAND, and NOR gates, as well as inverters. (D.I. 1043 at 23); '212 patent at 2:41-46, 4:33-35, 4:43-46. Relying on that fact, Micron contends that "[b]ecause NAND and NOR gates and inverter gates are disclosed in the 212 specification, Plaintiffs cannot now seek to rewrite the claims to cover NAND and NOR gates when the patentee chose to claim only an inverter gate." (D.I. 1043 at 24).

The cited passages of the specification are nothing more than brief descriptions of the specification's figures. All they show is that the patentee was aware of NAND and NOR gates. Micron has not identified any part of the specification which shows that a NAND or NOR gate may be used as an alternative to the "complementary FET inverter" required by claim 22. This appears to be the paradigmatic example of "generic references in [the] written specification." *See PSC Computer Prods.*, 355 F.3d at 1360. Since the specification does not disclose NAND and NOR gates "as an alternative to the relevant claim limitation," the disclosure dedication rule does not apply. *See Pfizer*, 429 F.3d at 1378.

For the foregoing reasons, Micron's motion for summary judgment of non-infringement under the doctrine of equivalents is denied.

D. '212 Anticipation

Micron pursues summary judgment of anticipation "[t]o the extent that the Court permits Plaintiffs to assert that Micron's accused circuits include a "clock input signal." (D.I. 1043 at 24). In other words, as was the case with the '853 patent, Micron contends that if Plaintiffs are permitted to advance their literal infringement theory, the scope of the patent will be broadened so as to encompass certain prior art (in this case, the Masuda reference). (*Id.*). Since the Court has granted summary judgment on the issue non-infringement, there is no "extent that the Court permit[ted] Plaintiffs" to advance their infringement theory. Therefore, the Court recognizes that Micron has no basis for seeking summary judgment on anticipation of the '212 patent. Summary judgment is denied.

E. '949 Non-Infringement

The asserted claims[10] of the '949 patent relate to an FET Differential Latching Inverter ("DLI") circuit. The DLI circuit includes two "complementary inverters." '949 patent at 23:5-28. The claims provide that each inverter includes both "a first input" and a "second input." *Id.* The claims also provide that a first bit line is connected to the first input of the first inverter and a second bit line is connected to the first input of the second inverter. *Id.* At claim construction, the Court construed "bit lines" to mean "a pair of different conductive lines in a memory cell array that are connected to memory cells for transferring the stored value of a selected memory cell out of the memory array." (D.I. 729 at p. 2). Micron argues that the inverters in its accused circuits do not include first and second inputs. (D.I. 1043 at 28). Additionally, for the K15L Design ID, Micron argues that since the "lines" accused by Plaintiffs are connected to a multiplexer and not to memory cells, it does not infringe as a matter of law. (*Id.* at 29).

i. First and Second Inputs

The central issue is whether Plaintiffs have produced evidence sufficient to show that the accused products include a first and second input. Micron argues that the Plaintiffs cannot raise a dispute of fact because the two inputs which Dr. Foty targets are merely "two locations along the same input." (D.I. 1043 at 28; D.I. 1047, Ex. 5 ¶¶ 63-66). In other words, Micron argues that because "both points are on the same line, have the same voltage, and are input into the same transistors," they cannot constitute two separate inputs. (D.I. 1043 at 28; D.I. 1047, Ex. 5 ¶¶ 63-66). Dr. Foty contends that inputs may be specific points (or "nodes") along each line. (D.I. 1087 at 30; D.I. 1089 ¶¶ 44-45). To put it another way, "[e]ach 'line' can have multiple input

[10] Plaintiffs allege that products embodying three Design IDs infringe claims 1 and 2 of the '949 patent. (D.I. 1047, Ex. 16; D.I. 1043 at 26). Claim 1 is the only asserted independent claim. '949 patent at 23:5-41.

and output nodes, just as a highway can have multiple entrance and exit ramps." (D.I. 1087 at 30; D.I. 1089 ¶¶ 44-45).

The disagreement between Plaintiffs and Micron is best characterized as a factual dispute. Dr. Foty's opinion cannot be discarded merely because Micron disagrees with it. Whether or not the accused products have one or two inputs (or what constitutes an input) is not a question the Court can resolve. Plaintiffs have shown there is a genuine dispute as to whether the accused products have the first and second inputs required by the claims.

ii. Bit Lines Connected to Memory

The Court construed "first bit line" and "second bit line" to mean "a pair of different conductive lines in a memory cell array *that are connected to memory cells* for transferring the stored value of a selected memory cell *out of the memory array*." (D.I. 729 at p. 2 (emphasis added)). Micron argues that Plaintiffs cannot raise a genuine issue of infringement because the "lines" that Plaintiffs target in the K15L Design ID are connected to a multiplexer, rather than to memory cells. (D.I. 1043 at 29; D.I. 1047, Ex. 5 ¶¶ 70-72). Plaintiffs argue that the mere existence of the multiplexer as an intermediary does not preclude the conclusion that the bit lines are "connected to" memory cells for transferring the stored value of a selected memory cell out of the memory array. (D.I. 1087 at 31). In so arguing, Plaintiffs rely on Figures 4A and 4B of the '949 patent, which—according to Dr. Foty—demonstrate that bit lines need not be directly connected to the memory cells. (D.I. 1089 ¶ 50).

This is a factual dispute between the parties. The parties dispute whether "connected to" requires a direct connection. Whether the presence of an intermediary negates the existence of a "connection" is a factual question reserved for the jury. A reasonable juror could conclude that

the accused devices have bit lines connected to memory cells for transferring the stored value of a selected memory cell out of the memory array.

There is a genuine dispute as to whether the accused products infringe the '949 patent. Therefore, summary judgment is denied.

F. '949 Anticipation

Micron contends that "to the extent that Plaintiffs are permitted to advance" their infringement theory for the '949 patent, "the 949 Asserted Claims are anticipated by prior art 6T SRAM cells," such as the Annaratone reference. (D.I. 1043 at 30). Since Dr. Walker contends that the '949 patent is only anticipated under Plaintiffs' infringement theory, he—in his infringement analysis—compares Annaratone to the accused products. (D.I. 1047, Ex. 5 ¶¶ 75-79). Plaintiffs contend this is insufficient to show validity, as it constitutes "an improper practicing the prior art defense." (D.I. 1087 at 32 (citing *Zenith Elecs. Corp. v. PDI Commc'n Sys., Inc.*, 522 F.3d 1348, 1363-64 (Fed. Cir. 2008))). Additionally, Plaintiffs argue that Annaratone does not disclose complementary FET inverters "producing an inverter transfer function between said first input and said output which is skewed toward one of said first and second reference voltages." (D.I. 1087 at 32); '949 patent at 23:12-17. Plaintiffs also assert that the Annaratone reference fails to disclose the limitation that "the product of the square channel saturation current and the ratio of width to length of said at least one FET of said first conductivity type [is] greater than the product of the square channel saturation current and the ratio of width to length of said at least one FET of said second conductivity type." (D.I. 1087 at 32); '949 patent at 23:4-39.

The parties dispute whether it is proper to compare the accused products to the prior art. It is well-established that "the same test must be used for both infringement and anticipation."

Int'l Seaway Trading Corp. v. Walgreens Corp., 589 F.3d 1233, 1239 (Fed. Cir. 2009). To use the Supreme Court's century-old maxim, "'[t]hat which infringes, if later, would anticipate if earlier.'" *Id.* (quoting *Peters v. Active Mfg. Co.*, 129 U.S. 530, 537 (1889)). The holding in *PDI Communications* did not change that. In that case, the defendant "provided no evidence whatsoever" that the prior art reference "satisfie[d] the final two limitations" of the relevant claim, instead relying on the argument: "to the extent the [allegedly infringing] PDI P20LCD is considered to practice [the limitations], then so did the RCA J20525 television." *PDI Commc'ns Sys.*, 522 F.3d at 1363 (first alteration in original). The case is best understood as an affirmation that anticipation requires a strict limitation-by-limitation analysis. *See, e.g.*, *Advanced Display Sys., Inc. v. Kent State Univ.*, 212 F.3d 1272, 1282 (Fed. Cir. 2000). The case does not preclude parties from arguing that if a claim limitation must be interpreted in a certain fashion to read on the accused products, then—if interpreted that same way—the claim reads on the prior art. *See PDI Commc'ns Sys.*, 522 F.3d at 1363 ("[I]t is the presence of the prior art and its relationship to the claim language that matters for invalidity." (alteration in original) (quoting *Tate Access Floors, Inc. v. Interface Architectural Res., Inc.*, 279 F.3d 1357, 1367 (Fed. Cir. 2002))). Claims are "interpreted and . . . given the same meaning for purposes of both validity and infringement analyses." *Amazon.com, Inc. v. Barnesandnoble.com, Inc.*, 239 F.3d 1343, 1351 (Fed. Cir. 2001). "A patent may not, like a 'nose of wax,' be twisted one way to avoid anticipation and another to find infringement." *Id.* (quoting *Sterner Lighting, Inc. v. Allied Elec. Supply, Inc.*, 431 F.2d 539, 544 (5th Cir. 1970)).

Micron has made out a prima facie case of invalidity. Dr. Walker has performed a limitation-by-limitation anticipation analysis that merely relies on the claim interpretations that follow from Plaintiffs' infringement theory. (*See* D.I. 1047, Ex. 5 at 67-76). This amounts to

prima facie "showing that each element of the claim at issue . . . is found in a single prior art reference," rather than simply an argument that the prior art is "identical, in all material respects, to an allegedly infringing product." *PDI Commc'ns Sys.*, 522 F.3d at 1363. That is not the end of the analysis, however. Plaintiffs' validity expert, Mr. Salmon, disagrees with Dr. Walker's opinion. Specifically, Mr. Salmon contends that Annaratone "does not disclose anything about the inverter transfer function of the circuit identified by Dr. Walker, let alone that the inverter transfer function is 'skewed toward one of said first and second reference voltages.'" (D.I. 1090 ¶ 20). Further, as to inherent disclosure, Mr. Salmon states that because Annaratone "does not disclose sufficient information concerning the widths and lengths of the P-channel transistors relative to the N-channel resistors," the skewing limitation is not a "necessary result" of Annaratone. (*Id.* ¶ 21); *see In re Cruciferous Sprout Litig.*, 301 F.3d 1343, 1349 (Fed. Cir. 2002) (To establish inherency, the prior art must "necessarily function[] in accordance with . . . the claimed limitations."). Additionally, Mr. Salmon posits that Annaratone discloses no information about the "square channel saturation current of the transistors." (*Id.* ¶ 22). In short, Mr. Salmon states that Annaratone does not anticipate the '949 patent.

Anticipation is a question of fact upon which Micron bears the burden of proof by clear and convincing evidence. On summary judgment, the Court is not permitted to weigh the testimony of the competing experts and draw its own conclusion. Mr. Salmon's anticipation analysis cannot be disregarded. There are factual issues to be resolved. Therefore, Micron has not shown there is no dispute as to whether Annaratone discloses, expressly or inherently, all the limitations of the '949 patent. Summary judgment is denied.

G. '367 Non-Infringement

The asserted claims[11] of the '367 patent relate to a high speed "logic circuit." '367 patent at 1:8-10. Specifically, the asserted claims require a "field effect transistor (FET) logic circuit," which the Court construed to mean "an electronic circuit that is capable of operating on digital signals in accordance with a logic function." (D.I. 729 at p. 3); '367 patent at 9:1-2. Micron argues that the accused circuits are "delay circuits" which do not perform a "logic function." (D.I. 1043 at 32; D.I. 1047, Ex. 5 ¶¶ 82-83). Additionally, Micron argues that the U68A Design ID does not contain "a complementary FET inverter . . . serially connected between said first and second potential levels" because the accused inverter is not connected between the two potential levels identified by Plaintiffs. (D.I. 1047, Ex. 5 ¶¶ 85-88, Ex. 26); '367 patent at 9:11-15. Plaintiffs argue that the accused circuitry performs the "identity" logic function. (D.I. 1089 ¶ 59). Plaintiffs also contend that the accused inverter is not connected to vccp!, and even if it were, because vcc! and vccp! are both power supplies, the inverter is connected to a second potential level as required by the patent. (D.I. 1087 at 34; D.I. 1089 ¶¶ 60-61; D.I. 1188).

The dispute concerning whether the accused products perform a "logic function" is one of fact. Dr. Foty contends that the infringing circuitry is a "sub-section of the entire circuit" and further, that "any delay introduced into the . . . circuit will have no effect upon the digital operation of the infringing circuitry." (D.I. 1089 ¶ 55). Dr. Foty also opines that the "identity logic function"—a logical function which produces the same output as input—is "well-known in digital circuit design." (*Id.* ¶ 59). In response to an assertion by Micron that the identity logic function is not a logic function at all, Dr. Foty provides the example of a buffer gate (along with its truth table) and cites to an online digital circuits textbook. (*Id.* ¶ 59, n.13; *see* D.I. 1043 at 32-

[11] Plaintiffs allege that Micron products embodying four Design IDs infringe claims 1, 4, 5, 9, and 11 of the '367 patent. (D.I. 1047, Ex. 20; D.I. 1043 at 31). Claim 1 is the only asserted independent claim. '367 patent at 9:1-62.

33). From the opinion of Dr. Foty, a reasonable juror could conclude that the accused circuitry performs a logic function. Therefore, there is a genuine dispute as to a material fact.

The Court reaches the same conclusion with regard to the question of whether the accused complementary FET inverter is "serially connected between said first and second potential levels." In his infringement report, Dr. Foty identified gnd! and vcc! as the first and second potential levels. (D.I. 1047, Ex. 25 at 25-26). Micron contends that the accused complementary FET inverter is not in fact connected between those voltages, but is instead connected between gnd! and vccp!. (D.I. 1043 at 33; D.I. 1047, Ex. 5 ¶¶ 85-88, Ex. 25 at 4-6). With its summary judgment brief, Micron produced a declaration from Micron employee Jared Adams, wherein Mr. Adams declared that vcc! and vccp! had different voltages. (D.I. 1047, Ex. 26). Relying on this declaration, Micron argues that because vcc! and vccp! have different voltages, the load FET and complementary FET inverter are not connected to the same "second potential level," as the patent requires. (D.I. 1113 at 18). Plaintiffs dispute that the complementary FET inverter is connected to vccp!.[12] (D.I. 1188). Additionally, Dr. Foty states that "the different labels do not actually tell us that 'vcc!' and 'vccp!' are different voltages." (D.I. 1089 ¶ 61). Plaintiffs also argue that even if Mr. Adams is correct, a person having ordinary skill in the art "would understand that [vcc! and vccp!] are both power supplies and thus constitute the same potential level, since the difference in voltage would not materially affect the

[12] In response to the declaration from Mr. Adams, Plaintiffs sought access to the source code computer in order to investigate the assertions made by Mr. Adams. (D.I. 1163 at 117-19). The Court granted this request. (*Id.* at 148). After the inspection, Mr. Adams was deposed by Plaintiffs. At the deposition, Plaintiffs asked Mr. Adams about an entirely new inverter, claiming that it was the "actual inverter" they sought to accuse rather than the "represent[ative]" one depicted in Dr. Foty's infringement report. (D.I. 1185, Ex. A at 5; D.I. 1186, Exs. 2-3; D.I. 1188 at p. 3 (alteration in original)). Plaintiffs will not be permitted to rely on this entirely new theory of infringement. Dr. Foty's report indicates that MH00013489 "represents the transistor-level structure" of the accused inverter in MH00013254. (D.I. 1047, Ex. 25 at 6). Plaintiffs cannot now change course and claim MH000112334 was the accused inverter all along.

operation of the circuit." (D.I. 1087 at 34-35; D.I. 1089 ¶¶ 60-61). From this back and forth, a genuine factual dispute is apparent. Dr. Foty contends that, even if Mr. Adams is correct, the variance in voltage makes no difference, opining that "[b]ecause 'vcc!' and 'vccp!' are both power supplies, the complementary FET inverter is connected to the 'second potential level.'" (D.I. 1089 ¶ 60). In other words, Dr. Foty opines that the accused inverter is connected to the same "second potential level" as the load FET, as required by the claim 1. '367 patent at 9:8-15 ("a load FET . . . connected between a second potential level . . . and . . . a complementary FET inverter . . . serially connected between said first and second potential levels"). Micron disagrees with Dr. Foty. That disagreement must be resolved by the jury. I conclude that Plaintiffs have presented sufficient evidence to allow a reasonable juror to conclude that the accused inverter meets the claim limitation. Therefore, summary judgment is denied.

H. Indirect Infringement

"To prove induced infringement [under 35 U.S.C. § 271(b)], the patentee "must show direct infringement, and that the alleged [indirect] infringer 'knowingly induced infringement and possessed specific intent to encourage another's infringement.'" *Toshiba Corp. v. Imation Corp.*, 681 F.3d 1358, 1363 (Fed. Cir. 2012) (quoting *i4i Ltd. P'ship v. Microsoft Corp.*, 598 F.3d 831, 851 (Fed. Cir. 2010)). Thus, liability under an inducement theory requires affirmative acts inducing direct infringement and "proof the defendant knew the acts were infringing." *Commil USA, LLC v. Cisco Sys., Inc.*, 135 S. Ct. 1920, 1928 (2015); *Tegal Corp. v. Tokyo Electron Co.*, 248 F.3d 1376, 1378-79 (Fed. Cir. 2001).

Micron states that "Plaintiffs' claim of induced infringement appears to be based on the theory that Micron sells accused [products] to its customers abroad and encourages those customers to import into the United States and use end products . . . that incorporate Micron's

chips." (D.I. 1043 at 34). Micron argues that because "Plaintiffs have put forth no evidence that Micron has ever encouraged its customers to import the customers' products into the United States," Plaintiffs have failed to show the specific intent required for a finding of inducement. (D.I. 1043 at 34). Micron misunderstands Plaintiffs' argument. Plaintiffs indeed contend that Micron induced infringement through encouraging the importation of infringing products, but Plaintiffs also argue that Micron encourages the use of the infringing products which, though not sold in the United States, ultimately end up in the United States. (D.I. 1087 at 35). In other words, Plaintiffs contend that certain infringing products end up in the United States without ever being sold by Micron in the United States. For these "untaxed" products,[13] Micron indirectly infringes by encouraging its customers to use the infringing products. (D.I. 1163 at 123-26). Specifically, Plaintiffs argue that Micron induced direct infringement by assisting customers with "'qualification' and 'validation' of the products," by "provid[ing] customers with product samples, technical support and testing services in the United States," by providing "technical notes (in English) that encourage the infringing use," by providing "quality assurance services in the United States," by providing pre-production engineering samples, by providing customers with Field Application Engineers, and by providing "product repair and replacement services in the United States." (D.I. 1087 at 35; D.I. 1088, Ex. E ¶¶ 477-82, 523).

Micron has not established that there is no genuine factual dispute as to whether it actively induced infringement. "[W]hoever without authority . . . uses . . . any patented invention[] within the United States or imports into the United States any patented invention . . . infringes the patent." 35 U.S.C. § 271(a); *see also Aro Mfg. Co. v. Convertible Top Replacement Co.*, 377 U.S. 476, 484-85 (1964) ("[I]t has often and clearly been held that unauthorized use,

[13] The products are "untaxed" in the sense that because they were never sold by Micron in the United States, they are not accounted for in Plaintiffs' direct infringement theory.

without more, constitutes infringement."). Plaintiffs have presented sufficient evidence from which a reasonable juror could find that Micron's products infringe the '949 patent. (D.I. 1087 at 35). Micron does not dispute that it had pre-suit knowledge of the patents-in-suit. From this knowledge, a reasonable juror could conclude that Micron "knew it was inducing users of [the] accused products to infringe" the '949 patent. *Tarkus Imaging, Inc. v. Adobe Sys., Inc.*, 2012 WL 2175788, at *4 (D. Del. June 14, 2012) (citing *Fujitsu Ltd. v. Netgear Inc.*, 620 F.3d 1321, 1330 (Fed. Cir. 2010)). Further, Plaintiffs have evidence of specific actions undertaken by Micron within the United States. From these activities a reasonable juror could conclude that Micron actively induced acts of direct infringement. *See, e.g., Semiconductor Energy Lab. Co. v. Chi Mei Optoelectronics Corp.*, 531 F. Supp. 2d 1084, 1114 (N.D. Cal. 2007) (evidence of technical support and on-site technical presentations in United States, among other things, were found sufficient to deny summary judgment); *Trustees of Columbia Univ. v. Roche Diagnostics GMBH*, 150 F. Supp. 2d 191, 208 (D. Mass. 2001) ("[W]here use of a patented device constitutes an infringement under § 271(a), courts have found that the maintenance or repair of the device likewise constitutes an infringement." (collecting cases)); *Tarkus Imaging*, 2012 WL 2175788, at *4 (denying summary judgment where accused indirect infringer "advertised use of the accused features of its products and provided users with instructions detailing how to operate the accused products").

Plaintiffs have advanced evidence sufficient to allow a reasonable juror to conclude that Micron induced the infringement of the patents-in-suit. Summary judgment is therefore denied.

I. Plaintiffs' Motion on '853 Non-Anticipation and Indefiniteness

Plaintiffs seek summary judgment on two issues: (1) the '853 patent is not anticipated by certain prior art references, and (2) the '853 patent is not indefinite. (D.I. 1056 at 7-8). In

seeking summary judgment of non-anticipation, Plaintiffs argue the asserted prior art does not disclose—expressly or inherently—the predetermined factor limitation, the asserted prior art does not enable one of ordinary skill to make the claimed invention, and certain asserted prior art does not actually qualify as prior art under § 102. As for the issue of indefiniteness, Plaintiffs argue that a person having ordinary skill in the art "would understand the claims covered finished products that meet the Predetermined Factor Limitation." (*Id.* at 20).

i. Anticipation

Micron argues that if Plaintiffs are permitted to use the algebraically-reduced expression for K to prove infringement, claim 1 becomes "so broad that it captures additional prior art." (D.I. 1082 at 7). Micron specifically contends that under Plaintiffs' infringement theory, prior art references RCA, Hedenstierna, Proebsting, and products embodying the A10C design anticipate the asserted claims of the '853 patent. (D.I. 1082 at 10-11). Of the prior art references upon which Plaintiffs seek summary judgment of non-anticipation, Micron contends that only the Steele reference anticipates "[w]hen the Court's construction of the claims is correctly applied." (D.I. 1082 at 8). The Court has found that Plaintiffs' infringement theory fails to create a genuine dispute of fact as to infringement, as it is inconsistent with the Court's claim construction. Therefore, Micron lacks a basis to pursue its anticipation theory that relies on RCA, Hedenstierna, Proebsting, and the A10C design. Thus, there is no dispute as to whether these references anticipate the '853 patent.[14] Plaintiffs are therefore entitled to summary judgment of non-anticipation with respect to these prior art references.

[14] In the briefing, the parties dispute whether these references are enabling and whether they actually qualify as prior art. Since I understand that, following the Court's ruling as to infringement, Micron no longer argues that these references anticipate, I need not reach these issues.

The Steele reference presents a different question. Micron contends that the Steele thesis anticipates the '853 patent when *K* is properly calculated using Equation (37), rather than Plaintiffs' algebraically-reduced expression for *K*. Plaintiffs argue that the Steele reference is not prior art, that it is not enabling, and that the predetermined factor limitation is not anticipated.

Plaintiffs argue that the Steele reference does not qualify as prior art. (D.I. 1056 at 29-30). Micron has advanced considerable evidence from which a reasonable juror could conclude that the Steele reference is prior art printed publication under § 102(b). The Steele reference is a master's thesis. (D.I. 1083, Ex. 7 at 4). A declaration from the National Technical Information Service (NTIS) states that the reference was publicly accessible by at least December 1, 1988.[15] (D.I. 1083, Ex. 6 at 2). Specifically, the reference was published in the Government Reports Announcements and Index ("GRA&I") on December 1, 1988. (*Id.*). That issue "would have been distributed to subscribers no more than one week after the cover date." (*Id.*). NTIS would begin shipping any orders from its subscribers at that time. (*Id.*). The GRA&I itself confirms the thesis was indexed by subject matter. (*Id.* at 3-5). Therefore, the Steele reference qualifies as a printed publication under § 102(b). *See In re Klopfenstein*, 380 F.3d 1345, 1348 (Fed. Cir. 2004); *OKI Am. Inc. v. Advanced Micro Devices, Inc.*, 2006 WL 2711555, at *5-6 (N.D. Cal. Sept. 21, 2006).

Plaintiffs contend that the Steele reference does not contain enough information to calculate the predetermined factor *K*, and therefore Steele cannot anticipate the '853 patent under § 102. I agree. "Anticipation of a patent claim requires a finding that the claim at issue 'reads on' a prior art reference." *Atlas Powder Co. v. Ireco Inc.*, 190 F.3d 1342, 1346 (Fed. Cir. 1999); *see also Titanium Metals Corp. of Am. v. Banner*, 778 F.2d 775, 782 (Fed. Cir. 1985) (If "a claim

[15] The '853 patent has an application date of March 21, 1990. Further, Plaintiffs assume for purposes of this motion that March 21, 1990 also represents the date of invention. (D.I. 1056 at 8).

covers several compositions, the claim is 'anticipated' if one of them is in the prior art."). Here, in order to anticipate, a reference need not have used Equation (37) in the design process, but must disclose a buffer that has a scaling factor less than a predetermined factor, when that factor is calculated using Equation (37). Since Steele does not disclose the requisite variables to calculate *K*, it does not disclose the predetermined factor limitation.

When comparing Steele to the '853 patent, Dr. Walker's invalidity chart simply does not address the $(1+L_c/\alpha_o L_o)$ expression within Equation (37). (D.I. 1083, Ex. 4 at 214). Instead, Dr. Walker opines that because "Steele does not include the interconnect capacitance in the simulation net list, . . . Steele discloses that the interconnect capacitance is negligible." (*Id.*). Dr. Walker then concludes that $(L_c/\alpha_o L_o)$ is zero. (*Id.* ¶ 36). The absence of information about interconnect length is not a disclosure at all, much less a disclosure that the value is zero. Further, Micron is trying to have it both ways. For purposes of non-infringement, Micron argued it was improper to assume that because interconnect length was negligible in the accused products, it could be treated as zero.[16] Micron now takes the position that because the Steele reference does not discuss interconnect capacitance at all, the exact same expression can be treated as zero. The Court agreed with Micron before and maintains that position now. Absent some relevant disclosure in the prior art reference, Micron cannot, in calculating Equation (37) for purposes of determining *K*, simply disregard certain variables. In order for Steele to anticipate, the predetermined factor limitation must "read on" the Steele reference. *See Atlas Powder*, 190 F.3d at 1346. Having failed to show that a prior art reference meets the

[16] At oral argument, counsel for Micron stated that treating interconnect length as zero was "not a proper substitution, because it is ignoring something that has a positive value indisputably, and then simply treating it as zero. . . . [T]hat then is a . . . non-use of Equation (37)." (D.I. 1163 at 18).

predetermined factor limitation, a reasonable juror could not conclude that the Steele thesis anticipates.

For an additional independent reason, Micron fails to survive summary judgment on non-anticipation with respect to the Steele reference. Dr. Walker makes certain assumptions about the η value that appears in the following limitation, as construed:

> the P-channel field effect transistor in each inverter stage having a channel which is wider than the channel of the corresponding N-channel field effect transistor of each inverter stage by a factor of η, the ratio of electron mobility in the N-channel field effect transistors to hole mobility in the P-channel field effect transistors, such that the voltage transfer function of each inverter stage is symmetrical.

(D.I. 729 at p. 2). Specifically, Dr. Walker concludes that η is "approximately" 2.5. (D.I. 1083, Ex. 4 ¶ 38). Dr. Walker justifies his arrival at this number in several ways. First, Dr. Walker notes that the P/N ratio in the inverters is 2.59. (*Id.*). From this, Dr. Walker concludes that since Steele "discloses that the rise time is approximately equal to the fall time for a given load," "the inverters have a symmetric voltage transfer function," and therefore η is approximately 2.5. (*Id.*). Second, Dr. Walker notes that the typical η range at that time (1988) would have ranged from 2 to 2.5. (*Id.*). Third, Dr. Walker states that he corroborated this with Mr. Steele himself. (*Id.* ¶ 40). For purposes of anticipation, the typical η range and the testimony of Mr. Steele are irrelevant. *See Calloway Golf Co. v. Acushnet Co.*, 576 F.3d 1331, 1346 (Fed. Cir. 2009) (holding that "every element of the claimed invention" must be described "express or inherently" within "the four corners of a single, prior art document"); *Finisar Corp. v. DirecTV Grp., Inc.*, 523 F.3d 1323, 1334-35 (Fed. Cir. 2008). Since the reference contains no information about η, it is not disclosed expressly. Inherent anticipation can be established when "prior art necessarily functions in accordance with, or includes, the claimed limitations." *In re Cruciferous Sprout Litig.*, 301 F.3d 1343, 1349 (Fed. Cir. 2002). Micron's inherency theory similarly fails. Dr.

Walker's conclusion about η is not a necessary result of Steele; it is an assumption, and further, is one subject to dispute.[17] Since Steele does not disclose a value for η—and one cannot merely be hypothesized for purposes of proving anticipation—Equation (37) cannot be calculated. Therefore, Micron has not shown that Steele meets the predetermined factor limitation.

Micron has failed to carry its burden of producing clear and convincing evidence from which a reasonable juror could conclude that the '853 patent was anticipated by the Steele reference. Having concluded that the Steele reference does not contain every element of the claimed invention, the Court need not address the argument that the Steele reference is not enabling. Plaintiffs' motion for summary judgment of non-anticipation, with respect to the Steele reference, is granted.

ii. Indefiniteness

Indefiniteness under 35 U.S.C. § 112 ¶ 2 is a question of law to be determined by the Court. *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1365 (Fed. Cir. 2011). "[A] patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 134 S. Ct. 2120, 2124 (2014).

Micron contends that "the asserted claims of the 853 Patent are indefinite to the extent that they are interpreted to encompass calculating K with equations other than Equation (37)." (D.I. 1082 at 26). Specifically, Micron argues that if Plaintiffs are permitted to advance an

[17] Mr. Salmon, in his reply declaration, states that "[e]quality of rise/fall time is not the same as symmetry of an inverter transfer function," since the former is an AC characteristic, while the latter is a DC characteristic. (D.I. 1124 ¶ 10). Further, Mr. Salmon states that since "Dr. Walker has failed to show that Steele discloses proper capacitive loading conditions and equal propagation delay times, . . . it is improper to assume that Steele discloses a symmetrical inverter transfer function based on the disclosure of equal rise and fall times." (*Id.*).

infringement theory using an equation "determined using only information about the finished products," which excludes the desired rise time variable, the asserted claims are indefinite. (*Id.*).

The Court has concluded that Plaintiffs' infringement theory cannot be sustained. Since the Court has rejected Plaintiffs' infringement theory, Micron no longer has a basis for pursuing a claim of indefiniteness. Indeed, Micron explicitly argued during claim construction that if their proposed construction of "predetermined factor" were not adopted, the claim would be indefinite. (D.I. 677 at 80-81). The Court adopted Micron's construction, finding that K is calculating using Equation (37). (D.I. 715 at pp. 3-5). The Court does not understand Micron to now argue that the '853 patent is invalid when K is properly calculated using Equation (37), nor likely could it. *See Detz v. Greiner Indus., Inc.*, 346 F.3d 109, 117-18 (3d Cir. 2003) (discussing judicial estoppel). Therefore, there is no genuine dispute that the '853 patent is not indefinite. Plaintiffs are entitled to summary judgment.

IV. CONCLUSION

For the reasons set forth above, Micron's motion for summary judgment of non-infringement (D.I. 1037) is **GRANTED IN PART** and **DENIED IN PART**; Micron's motion for summary judgment of invalidity (D.I. 1039) is **DENIED**; Micron's motion for summary judgment of no indirect infringement (D.I. 1040) is **GRANTED IN PART** and **DENIED IN PART**; Plaintiffs' motion for partial summary judgment (D.I. 1055) is **GRANTED IN PART** and **DISMISSED AS MOOT IN PART**. An appropriate order will be entered.