IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF DELAWARE

CRADLE IP, LLC,	)	
	)	
Plaintiff,	)	
	)	
v.	)	Civ. No. 11-1254-SLR
	)	
TEXAS INSTRUMENTS, INC.	)	
	)	
Defendant	)	
	)	

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MEMORANDUM OPINION

Dated: November 20, 2013
Wilmington, Delaware

ROBINSON, District Judge

I. INTRODUCTION

On December 16, 2011, plaintiff Cradle IP, LLC ("Cradle") filed suit in this district against defendant Texas Instruments, Inc. ("TI") alleging infringement of three of its patents: U.S. Patent Nos. 6,874,049 ("the '049 patent"), 6,708,259 (the "259 patent"), and 6,647,450 (the "450 patent"). (D.I. 1) TI answered the complaint and asserted a counterclaim for declaratory judgment of non-infringement and invalidity of the '049, '259, and '450 patents on February 6, 2012. (D.I. 10) Cradle answered TI's counterclaims on March 1, 2012. (D.I. 15)

Presently before the court are TI's motions for summary judgment of non-infringement and invalidity of the patents-in-suit. (D.I. 217; D.I. 218) TI also filed motions to exclude testimony by Cradle's experts, Dr. James Olivier and Dr. David Albonesi. (D.I. 224; D.I. 227) Additionally, Cradle filed motions to strike the declaration and testimony of Michael Shay, as well as new expert opinions. (D.I. 271; D.I. 309) TI also filed motions to strike inadmissible evidence and untimely expert opinions. (D.I. 295; D.I. 315) The court has jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

Cradle is a limited liability corporation organized and existing under the laws of the State of Delaware, with its principal place of business in Mountain View, California. (D.I. 1 at ¶ 6) Cradle is a privately-held, majority-owned subsidiary of Cradle Technologies. (*Id.* at ¶ 8) Cradle Technologies recently assigned the patents-in-suit to Cradle. (*Id.*) TI is a corporation organized and existing under the laws of the State of Delaware, with its principal place of business in Dallas, Texas. (*Id.* at ¶ 7) It makes,

manufactures, and sells the accused products. (*Id.* at ¶¶ 13, 16, 19)

II. STANDARDS OF REVIEW

A. Summary Judgment

"The court shall grant summary judgment if the movant shows that there is no genuine dispute as to any material fact and the movant is entitled to judgment as a matter of law." Fed. R. Civ. P. 56(a). The moving party bears the burden of demonstrating the absence of a genuine issue of material fact. *Matsushita Elec. Indus. Co. v. Zenith Radio Corp.*, 415 U.S. 574, 586 n.10 (1986). A party asserting that a fact cannot be—or, alternatively, is—genuinely disputed must support the assertion either by citing to "particular parts of materials in the record, including depositions, documents, electronically stored information, affidavits or declarations, stipulations (including those made for the purposes of the motions only), admissions, interrogatory answers, or other materials," or by "showing that the materials cited do not establish the absence or presence of a genuine dispute, or that an adverse party cannot produce admissible evidence to support the fact." Fed. R. Civ. P. 56(c)(1)(A) & (B). If the moving party has carried its burden, the nonmovant must then "come forward with specific facts showing that there is a genuine issue for trial." *Matsushita*, 415 U.S. at 587 (internal quotation marks omitted). The court will "draw all reasonable inferences in favor of the nonmoving party, and it may not make credibility determinations or weigh the evidence." *Reeves v. Sanderson Plumbing Prods., Inc.*, 530 U.S. 133, 150 (2000).

To defeat a motion for summary judgment, the non-moving party must "do more than simply show that there is some metaphysical doubt as to the material facts."

Matsushita, 475 U.S. at 586-87; *see also Podohnik v. U.S. Postal Service*, 409 F.3d 584, 594 (3d Cir. 2005) (stating party opposing summary judgment "must present more than just bare assertions, conclusory allegations or suspicions to show the existence of a genuine issue") (internal quotation marks omitted). Although the "mere existence of some alleged factual dispute between the parties will not defeat an otherwise properly supported motion for summary judgment," a factual dispute is genuine where "the evidence is such that a reasonable jury could return a verdict for the nonmoving party." *Anderson v. Liberty Lobby, Inc.*, 411 U.S. 242, 247-48 (1986). "If the evidence is merely colorable, or is not significantly probative, summary judgment may be granted." *Id.* at 249-50 (internal citations omitted); *see also Celotex Corp. v. Catrett*, 411 U.S. 317, 322 (1986) (stating entry of summary judgment is mandated "against a party who fails to make a showing sufficient to establish the existence of an element essential to that party's case, and on which that party will bear the burden of proof at trial").

B. Claim Construction

Claim construction is a matter of law. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1330 (Fed. Cir. 2005) (en banc). Claim construction focuses on intrinsic evidence - the claims, specification and prosecution history - because intrinsic evidence is "the most significant source of the legally operative meaning of disputed claim language." *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996); *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996). Claims must be interpreted from the perspective of one of ordinary skill in the relevant art at the time of the invention. *Phillips*, 415 F.3d at 1313.

Claim construction starts with the claims, *id.* at 1312, and remains centered on the words of the claims throughout. *Interactive Gift Express, Inc. v. Compuserve, Inc.*, 256 F.3d 1323, 1331 (Fed. Cir. 2001). In the absence of an express intent to impart different meaning to claim terms, the terms are presumed to have their ordinary meaning. *Id.* Claims, however, must be read in view of the specification and prosecution history. Indeed, the specification is often "the single best guide to the meaning of a disputed term." *Phillips*, 415 F.3d at 1315.

C. Infringement

A patent is infringed when a person "without authority makes, uses or sells any patented invention, within the United States . . . during the term of the patent." 35 U.S.C. § 271(a). A two-step analysis is employed in making an infringement determination. *See Markman*, 52 F.3d at 976. First, the court must construe the asserted claims to ascertain their meaning and scope. *See id.* Construction of the claims is a question of law subject to de novo review. *See Cybor Corp. v. FAS Techs.*, 138 F.3d 1448, 1454 (Fed. Cir. 1998). The trier of fact must then compare the properly construed claims with the accused infringing product. *See Markman*, 52 F.3d at 976. This second step is a question of fact. *See Bai v. L & L Wings, Inc.*, 160 F.3d 1350, 1353 (Fed. Cir. 1998).

"Direct infringement requires a party to perform each and every step or element of a claimed method or product." *BMC Res., Inc. v. Paymentech, L.P.*, 498 F.3d 1373, 1378 (Fed. Cir. 2007), *overruled on other grounds by* 692 F.3d 1301 (Fed. Cir. 2012). "If any claim limitation is absent from the accused device, there is no literal infringement

as a matter of law." *Bayer AG v. Elan Pharm. Research Corp.*, 212 F.3d 1241, 1247 (Fed. Cir. 2000). If an accused product does not infringe an independent claim, it also does not infringe any claim depending thereon. *See Wahpeton Canvas Co. v. Frontier, Inc.*, 870 F.2d 1546, 1553 (Fed. Cir. 1989). However, "[o]ne may infringe an independent claim and not infringe a claim dependent on that claim." *Monsanto Co. v. Syngenta Seeds, Inc.*, 503 F.3d 1352, 1359 (Fed. Cir. 2007) (quoting *Wahpeton Canvas*, 870 F.2d at 1552) (internal quotations omitted). A product that does not literally infringe a patent claim may still infringe under the doctrine of equivalents if the differences between an individual limitation of the claimed invention and an element of the accused product are insubstantial. *See Warner-Jenkinson Co. v. Hilton Davis Chem. Co.*, 520 U.S. 17, 24 (1997). The patent owner has the burden of proving infringement and must meet its burden by a preponderance of the evidence. *See SmithKline Diagnostics, Inc. v. Helena Lab. Corp.*, 859 F.2d 878, 889 (Fed. Cir. 1988) (citations omitted).

When an accused infringer moves for summary judgment of non-infringement, such relief may be granted only if one or more limitations of the claim in question does not read on an element of the accused product, either literally or under the doctrine of equivalents. *See Chimie v. PPG Indus., Inc.*, 402 F.3d 1371, 1376 (Fed. Cir. 2005); *see also TechSearch, L.L.C. v. Intel Corp.*, 286 F.3d 1360, 1369 (Fed. Cir. 2002) ("Summary judgment of noninfringement is . . . appropriate where the patent owner's proof is deficient in meeting an essential part of the legal standard for infringement, because such failure will render all other facts immaterial."). Thus, summary judgment

of non-infringement can only be granted if, after viewing the facts in the light most favorable to the non-movant, there is no genuine issue as to whether the accused product is covered by the claims (as construed by the court). *See Pitney Bowes, Inc. v. Hewlett–Packard Co.*, 182 F.3d 1298, 1304 (Fed. Cir. 1999).

"[A] method claim is not directly infringed by the sale of an apparatus even though it is capable of performing only the patented method. The sale of the apparatus is not a sale of the method. A method claim is directly infringed only by one practicing the patented method." *Joy Technologies, Inc. v. Flakt, Inc.*, 6 F.3d 770, 775 (Fed. Cir. 1993). Therefore, "an accused infringer must perform all the steps of the claimed method, either personally or through another acting under his direction or control." *Akamai Technologies, Inc. v. Limelight Networks, Inc.*, 692 F.3d 1301, 1307 (Fed. Cir. 2012).

With respect to apparatus claims, "to infringe a claim that recites capability and not actual operation, an accused device 'need only be capable of operating in the described mode.'" *Finjan, Inc. v. Secure Computing Corp.*, 626 F.3d 1197, 1204 (Fed. Cir. 2010) (citing *Intel Corp. v. U.S. Int'l Trade Comm'n*, 946 F.2d 821, 832 (Fed. Cir. 1991). However, if an apparatus claim requires "software [to] be configured in a particular way to infringe," infringement does not occur merely because the apparatus could be used in an infringing fashion. *Finjan*, 626 F.3d at 1204-05.

For there to be infringement under the doctrine of equivalents, the accused product or process must embody every limitation of a claim, either literally or by an equivalent. *Warner-Jenkinson*, 520 U.S. at 41. An element is equivalent if the

differences between the element and the claim limitation are "insubstantial." *Zelinski v. Brunswick Corp.*, 185 F.3d 1311, 1316 (Fed. Cir. 1999). One test used to determine "insubstantiality" is whether the element performs substantially the same function in substantially the same way to obtain substantially the same result as the claim limitation. *See Graver Tank & Mfg. Co. v. Linde Air Products Co.*, 339 U.S. 605, 608 (1950). This test is commonly referred to as the "function-way-result" test. The mere showing that an accused device is equivalent overall to the claimed invention is insufficient to establish infringement under the doctrine of equivalents. The patent owner has the burden of proving infringement under the doctrine of equivalents and must meet its burden by a preponderance of the evidence. *See SmithKline Diagnostics, Inc. v. Helena Lab. Corp.*, 859 F.2d 878, 889 (Fed. Cir. 1988) (citations omitted).

D. Invalidity

1. Anticipation

Under 35 U.S.C. § 102(b), "[a] person shall be entitled to a patent unless the invention was patented or described in a printed publication in this or a foreign country . . . more than one year prior to the date of the application for patent in the United States." The Federal Circuit has stated that "[t]here must be no difference between the claimed invention and the referenced disclosure, as viewed by a person of ordinary skill in the field of the invention." *Scripps Clinic & Research Found. v. Genentech, Inc.*, 927 F.2d 1565, 1576 (Fed. Cir. 1991). In determining whether a patented invention is explicitly anticipated, the claims are read in the context of the patent specification in

which they arise and in which the invention is described. *Glaverbel Societe Anonyme v. Northlake Mktg. & Supply, Inc.*, 45 F.3d 1550, 1554 (Fed. Cir. 1995). The prosecution history and the prior art may be consulted if needed to impart clarity or to avoid ambiguity in ascertaining whether the invention is novel or was previously known in the art. *Id.* The prior art need not be *ipsissimis verbis* (i.e., use identical words as those recited in the claims) to be anticipating. *Structural Rubber Prods. Co. v. Park Rubber Co.*, 749 F.2d 707, 716 (Fed. Cir. 1984).

A prior art reference also may anticipate without explicitly disclosing a feature of the claimed invention if that missing characteristic is inherently present in the single anticipating reference. *Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1268 (Fed. Cir. 1991). The Federal Circuit has explained that an inherent limitation is one that is necessarily present and not one that may be established by probabilities or possibilities. *Id.* That is, "[t]he mere fact that a certain thing may result from a given set of circumstances is not sufficient." *Id.* The Federal Circuit also has observed that "[i]nherency operates to anticipate entire inventions as well as single limitations within an invention." *Schering Corp. v. Geneva Pharms. Inc.,* 339 F.3d 1373, 1380 (Fed. Cir. 2003). Moreover, recognition of an inherent limitation by a person of ordinary skill in the art before the critical date is not required to establish inherent anticipation. *Id.* at 1377.

An anticipation inquiry involves two steps. First, the court must construe the claims of the patent in suit as a matter of law. *Key Pharms. v. Hercon Labs Corp.,* 161 F.3d 709, 714 (Fed. Cir. 1998). Second, the finder of fact must compare the construed claims against the prior art. *Id.* A finding of anticipation will invalidate the patent.

Applied Med. Res. Corp. v. U.S. Surgical Corp., 147 F.3d 1374, 1378 (Fed. Cir. 1998).

2. Obviousness

"A patent may not be obtained . . . if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art." 35 U.S.C. § 103(a). Obviousness is a question of law, which depends on underlying factual inquiries.

Under § 103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background the obviousness or non-obviousness of the subject matter is determined.

"[A] patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." *KSR*, 550 U.S. at 418. Likewise, a defendant asserting obviousness in view of a combination of references has the burden to show that a person of ordinary skill in the relevant field had a reason to combine the elements in the manner claimed. *Id.* at 418-19. The Supreme Court has emphasized the need for courts to value "common sense" over "rigid preventative rules" in determining whether a motivation to combine existed. *Id.* at 419-20. "[A]ny need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed." *Id.* at 420. In addition to showing that a person of ordinary skill in the art would have had reason to attempt to make the composition or

device, or carry out the claimed process, a defendant must also demonstrate that "such a person would have had a reasonable expectation of success in doing so." *PharmaStem Therapeutics, Inc. v. ViaCell, Inc.*, 491 F.3d 1342, 1360 (Fed. Cir. 2007).

A combination of prior art elements may have been "obvious to try" where there existed "a design need or market pressure to solve a problem and there [were] a finite number of identified, predictable solutions" to it, and the pursuit of the "known options within [a person of ordinary skill in the art's] technical grasp" leads to the anticipated success. *Id.* at 421. In this circumstance, "the fact that a combination was obvious to try might show that it was obvious under § 103." *Id.* Federal Circuit precedent has also established that "[s]tructural relationships may provide the requisite motivation or suggestion to modify known compounds to obtain new compounds," and that particular types of structural similarity can give rise to a case of prima facie obviousness. *Genetics Institute, LLC v. Novartis Vaccines and Diagnostics, Inc.*, 655 F.3d 1291, 1312 (Fed. Cir. 2011) (citing *In re Deuel*, 51 F.3d 1552, 1558 (Fed. Cir. 1995)).

A court is required to consider secondary considerations, or objective indicia of non-obviousness, before reaching an obviousness determination, as a "check against hindsight bias." *See In re Cyclobenzaprine Hydrochloride Extended-Release Capsule Patent Litig.*, 676 F.3d 1063 (Fed. Cir. 2012). "Such secondary considerations as commercial success, long felt but unsolved needs, failure of others, etc., might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented." *Graham v. John Deere Co. of Kansas City*, 383 U.S. 1, 17–18 (1966).

"Because patents are presumed to be valid, *see* 35 U.S.C. § 282, an alleged infringer seeking to invalidate a patent on obviousness grounds must establish its obviousness by facts supported by clear and convincing evidence." *Kao Corp. v. Unilever U.S., Inc.*, 441 F.3d 963, 968 (Fed. Cir. 2006) (citation omitted). In conjunction with this burden, the Federal Circuit has explained that,

> [w]hen no prior art other than that which was considered by the PTO examiner is relied on by the attacker, he has the added burden of overcoming the deference that is due to a qualified government agency presumed to have properly done its job, which includes one or more examiners who are assumed to have some expertise in interpreting the references and to be familiar from their work with the level of skill in the art and whose duty it is to issue only valid patents.

PowerOasis, Inc. v. T-Mobile USA, Inc., 522 F.3d 1299, 1304 (Fed. Cir. 2008) (quoting *Am. Hoist & Derrick Co. v. Sowa & Sons*, 725 F.2d 1350, 1359 (Fed. Cir. 1984)).

III. RECORD

As explained above, the purpose of the summary judgment exercise is to determine whether there are genuine issues of material fact that require resolution by a jury. Issues of fact are raised by conflicting evidence, not by attorney argument or conclusory expert opinions. Evidence appropriate for review on summary judgment is that which has been vetted through discovery.[1] In order to make its determinations on summary judgment, the court actually peruses the record to confirm that: (1) the parties have cited to evidence in support of their arguments; and (2) the evidence

[1] I.e., there should be no surprises in the summary judgment record.

demonstrates the proposition for which it was cited.[2] With the above in mind, the court addresses the summary judgment record compiled by the parties at bar, in order to address the various motions to strike and to exclude filed by the parties in connection with said record.

With respect to the record in general, the parties could not have been less helpful to the court. In connection with their eight motions and 24 briefs, the parties filed something like 42 declarations and volumes of appendices referencing or containing exhibits. Often the parties (and their experts) cited to documents by their Bates-stamp numbers, with no indicia of their location in the record. Even when the parties were kind enough to locate the document in question by an exhibit number, it was often difficult to discern which of the volumes containing identical exhibit numbers was actually referenced. To add insult to injury, the parties organized the appendices so that the exhibits were not necessarily included in numerical order because, e.g., one exhibit had to be sealed. In sum, it was a rare occurrence that a brief cited evidence by an exhibit number that was clearly identified by the appendix in which it resided.

Which takes us to the various pending motions. Although not the first-filed motions, the court would be remiss if it did not recount the tremendous waste of time spent by the parties (and the court) in connection with the expert reports relating to infringement. As reflected in the docket, Cradle's expert (Dr. Albonesi) filed his initial report on infringement, followed by TI's rebuttal report on non-infringement filed by its expert (Dr. Hassoun). Cradle argues that TI revealed for the first time its

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[2]This is especially important to do in cases such as this, where so much of the briefing is attorney argument, rather than evidence-based.

non-infringement theories through the rebuttal report, causing Dr. Albonesi to file a supplemental report. Because Dr. Albonesi arguably expanded his response beyond that which was vetted through discovery, Dr. Hassoun also filed a supplemental expert report in response to Dr. Albonesi's supplemental report. Bad enough. Not content to rely on this series of reports, both parties submitted expert declarations (complete with appendices) in support of their respective infringement positions on summary judgment. All of these efforts to presumably identify and corroborate their arguments ultimately led to the counter-motions to strike certain portions of the supplemental reports and/or declarations as containing "new" opinions.[3]

The court grants TI's motion to strike certain paragraphs of the Albonesi declaration. (D.I. 295, 315) As far as the court can tell, the declaration (D.I. 285) is longer than his two expert reports combined (D.I. 245, exs. 4 and 23), and primarily cites to itself as authority.[4] Because Dr. Albonesi's initial and supplemental reports are part of the record,[5] there should be no prejudice to plaintiff, to wit, only new theories will truly be stricken. The court also grants TI's motion as it relates to the "Declaration of Third-Party Motorola Solutions, Inc." as said "evidence" was not vetted through discovery. (D.I. 295)

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[3]To the extent TI has moved to strike the initial and supplemental expert reports of Dr. Albonesi as failing the reliability test set forth in *Daubert* and its progeny, said motion (D.I. 227) is denied as moot, as the sufficiency of Dr. Albonesi's opinions will be addressed in connection with the court's discussion on infringement *infra*.

[4]To the extent it refers to his reports, the court has reviewed his reports and the evidence cited therein.

[5]Unlike complete versions of Dr. Hassoun's two reports, which are dissected and scattered throughout multiple volumes. Again, not helpful.

The court, however, denies the remaining motions that relate to the supplemental expert reports, including the motion related to Dr. Hassoun's declaration that relies on his supplemental report. (D.I. 309, 315) In this regard, the court has neither the time nor the resources - nor even the record - to recreate the parties' tortuous litigation strategies insofar as determining whether plaintiff had cause to file a supplemental report in the first instance and whether it ventured into new theories which demanded a response by defendant in the second instance. Because the court relies on the remaining reports only to identify the evidence relied upon by the experts, which evidence has been vetted through discovery, the prejudice to the parties, if any, is minimal and can be addressed through focused evidentiary disputes.

The final motions to be addressed are those related to the parties' invalidity experts. Defendant has filed a motion to exclude the testimony of Dr. Olivier on secondary considerations of non-obviousness based on his alleged failure to establish a nexus between the secondary considerations and any of the claimed inventions. (D.I. 224) The court denies this motion, finding that Dr. Olivier's opinion rests upon a reliable foundation and that defendant's challenge goes to the weight of the evidence.

Plaintiff has filed a motion to strike the declaration and testimony of Michael Shay as containing disclosures that were never vetted through discovery. (D.I. 271) The court grants this motion. If, indeed, Mr. Shay's declaration is consistent with the patent, the NS486SXF Data Sheet, and the NS486SXF chip, then his declaration is redundant, as Dr. Hassoun has described and relied on all three prior art references. To the extent Mr. Shay had anything to add, defendant had the obligation to supplement its discovery responses before the close of fact discovery.

IV. DISCUSSION

For each of the three patents-in-suit, the court will discuss the background technology, any necessary claim construction on summary judgment, and any infringement and invalidity issues on summary judgment.

A. The '049 patent

The '049 patent, entitled "Semaphores With Interrupt Mechanism," was filed on February 1, 2002 and issued on March 29, 2005. It claims priority from provisional application No. 60/266,002 which was filed on February 2, 2001. The '049 patent is assigned to Cradle. (D.I. 1 at ¶ 8)

A multiprocessor system of the prior art included a system bus coupled to each of a plurality of processors, a main memory, and a shared resource. ('049 patent, 1:16-19) The main memory included a semaphore which was used to monitor access to a shared resource by the processors. (*Id.* at 1:21-23) The processors each include a register. (*Id.* at 1:23-24) The processors examined the content of the semaphore to determine the availability of a shared resource. (*Id.* at 1:26-28) When the shared resource was available for access, the content of the semaphore read a "0." (*Id.* at 1:28-33)

To access the shared resource, the processor would read the content of the semaphore into its register and write a "1" into the semaphore. (*Id.* at 1:33-36) The reading of the semaphore constituted one bus transaction. (*Id.* at 1:37-40) In the event that a processor examined the content of the semaphore and it read that the shared resource was not available for access, the processor executed a program loop that

included: (a) reading the content of the semaphore into its register; (b) writing a "1" into the semaphore; and (c) examining the copy of the content of the semaphore which it received in its register. (*Id.* at 1:59-67) "The processor execute[d] the program loop until the copy of the content of the semaphore which the processor receive[d] in its register [was] a '0'." (*Id.* at 1:65, 2:1-2) "This require[d] repeated use of the system bus." (*Id.* at 2:11-12)

The '049 patent eliminates the required repeated reading and writing and aims to increase the system throughput by introducing a digital system comprising a semaphore cell, an interrupt generation circuit coupled to the semaphore cell, and a processor coupled to the interrupt generation circuit. (*Id.* at 2:19-28) "The semaphore cell is configured to have a first state and a second state, the first state of the semaphore cell indicating that a shared resource is available for access, and the second state of the semaphore cell indicating that the shared resource is unavailable for access." (*Id.* at 2:28-32) "The interrupt generation circuit is configured to generate a semaphore interrupt signal to the processor if the semaphore cell changes from the second state to the first state and if the processor needs to access the shared resource." (*Id.* at 2:32-35)

Cradle alleges that TI's digital signal processor ("DSP") chips infringe apparatus claims 1-3 and method claim 6 of the '049 patent. (D.I. 278 at 11) Claims 1 and 6 teach a system and method, respectively, for monitoring access by a processor to a shared resource. The claims are reproduced below:

> 1. In a digital system of the type having at least first and second processors and at least one shared resource

accessible to the processors via a system bus, the bus allowing only one bus transaction in any one clock cycle, a hardware semaphore circuit coupled to said system bus and configured to monitor shared resource accesses by said processors, the hardware semaphore circuit comprising:

a semaphore cell coupled to the first and second processors via the system bus and configured to have a first state and a second state, the first state indicating that the shared resource is available for access and the second state indicating that the shared source is unavailable for access, and configured to be in the second state after being read by any processor and to change back to the first state after the shared resource is again made available for access; and

an interrupt generation circuit coupled to the first and second processors via the system bus and coupled to an output of the semaphore cell, and configured to generate a semaphore interrupt signal to any processor requesting access to the shared resource Whenever the semaphore cell changes from the second state back to the first state, the interrupt generation circuit comprising:

(i) a semaphore interrupt cell coupled to the output of the semaphore cell and configured to have a third state and a fourth state, the fourth state indicating that the semaphore cell has changed from the second state back to the first state and thus that the shared resource has just been made available for access;

(ii) first and second semaphore interrupt enable cells respectively coupled to the first and second processors via the system bus, each semaphore interrupt enable cell configured to have a fifth state and a sixth state, the fifth state indicating that the corresponding processor does not need to access the shared resource and the sixth state indicating that the corresponding processor has read the semaphore cell and found that the semaphore is in the second state; and

(iii) first and second logic gate circuits coupled to the semaphore interrupt cell, to respective first and

second semaphore interrupt enable cells, and via the system bus to respective first and second processors, each logic gate circuit configured to generate a semaphore interrupt signal to its corresponding processor if the semaphore interrupt cell is in the fourth state and the corresponding semaphore interrupt enable cell is in the sixth state, the semaphore interrupt cell and a corresponding semaphore interrupt enable cell further configured to change back to their respective third and fifth states after the semaphore interrupt signal is sent to its corresponding processor.

(*Id.* at 6:50-67, 7:1-33)

2. The hardware semaphore circuit in a digital system as in claim 1, wherein the system has multiple shared resources, and the semaphore cell, the semaphore interrupt cell and the first and second semaphore interrupt enable cells are cells of corresponding registers with one cell of each register dedicated to semaphore operations for a particular shared resource.

3. The hardware semaphore circuit in a digital system as in claim 1, wherein more than two processors can access the at least one shared resource via the system bus, and the interrupt generation circuit comprises additional semaphore interrupt enable cells and logic gate circuits corresponding each additional processor.

6. A method of using a hardware semaphore circuit to monitor shared resource accesses over a system bus that allows only one bus transaction in any one clock cycle, there being at least first and second processors and at least one shared resource coupled to said system bus together with said hardware semaphore circuit, the method comprising: reading a state of a semaphore cell of the hardware semaphore circuit by a first processor and if the state read from the semaphore cell is a first state, indicating that the shared resource is available for access, then accessing the shared resource by the first processor, but if the state read from the semaphore cell is a second state, indicating that the shared resource is unavailable for access, then setting a

first semaphore interrupt enable cell to a state indicating that the first processor needs to access the shared resource and the first processor waiting for a semaphore interrupt signal from the hardware semaphore circuit before again reading the state of the semaphore cell, any reading of the state of the semaphore cell by any processor setting the state of the semaphore cell to its second state, the semaphore cell changing back to its first state after the shared resource is again made available for access;

continually monitoring the state of the semaphore cell by a semaphore interrupt cell of the hardware semaphore, the semaphore interrupt cell having third and fourth states with the fourth state indicating that the shared resource has just been made available for access, the semaphore interrupt cell changing to the fourth state whenever the semaphore cell being monitored has just changed from the second state back to the first state;

reading the state of the semaphore cell by a second processor and if the state read from the semaphore cell is a first state then accessing the shared resource by the second processor, but if the state read from the semaphore cell is second state then setting a second semaphore interrupt enable cell to a state indicating that the second processor reads to access the share resource and the second processor waiting for a semaphore interrupt signal from the hardware semaphore circuit before again reading the state of the semaphore cell; and

whenever the semaphore interrupt cell changes to the fourth state and either the first or second semaphore interrupt enable cell is in a state indicating that the respective first or second processor needs to access the shared resource, generating a semaphore interrupt signal for the respective first and second processor and transmitting said interrupt signal thereto over said system bus.

(*Id.* at 8:19-8:65)

1. Claim Limitations

a. "A system bus that allows only one bus transaction in any

one clock cycle"[6]

The court construes "a system bus that allows only one bus transaction in any one clock cycle" as "a signal path shared by all devices that are connected to the path and used for transactions among them, in which only one device has use of the path for the entire duration of the transaction." "One bus transaction" is construed as "a transaction in which only one device has use of the system bus for the entire duration of the transaction."

That the system bus is a shared path between the processors, the shared resource, and the semaphore circuit is supported by the specification. ('049 patent, 2:66-3:6) Although the only description of "one bus transaction" appears in the background section of the patent and limits it to "the reading of the semaphore and writing a '1' into the semaphore by the processor," the patent provides no further support for the notion that the patentee wished to limit this term to this type of transaction. (*See id.* at 1:35-40; 1:55-58)[7]

In distinguishing the present invention from the Wenniger reference cited by the PTO, applicant noted that

> the hardware semaphore is accessed via a system bus in which only one bus transaction can take place in any one clock cycle. (The bus system in the present invention

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[6] The parties identified the terms "one bus transaction" and "system bus, the bus allowing only one bus transaction in any one clock cycle" in their joint claim construction statement. (D.I. 191) The court will discuss these terms together.

[7]The background further explains that "the processor seizes the system bus continuously for both the reading and writing of the semaphore," and that without this guarantee, a race condition — when at least two processors have access to a shared resource at the same time — may occur. (*Id.* at 1:40-45)

> effectively serializes access to the semaphore from multiple contenders). There is no need for arbitrated access to the semaphore in applicant's invention.

(D.I. 201 at CIP 131) Notably, applicant cancelled the original claims, which did not specify how the interrupt signals were transmitted to the processor, and included the limitation to method claim 6 that the interrupt signal is transmitted over the system bus. (*Id.* at CIP 126-130)[8]

b. "Any processor requesting access to the shared resource"

The court adopts TI's construction "all processors requesting access to the shared resource." There is no evidence to indicate that the patentee wished to limit his invention to only a number of processors requesting access to the shared resource as Cradle argues. (D.I. 206 at 12-13) Instead the specification explains that "[t]he interrupt generation circuit is configured to generate a semaphore interrupt signal to the processor if the semaphore cell changes from the second state to the first sate and if the processor needs to access the shared resources." ('049 patent, 2:33-36)

c. "The shared resource is available/unavailable for access"

The court construes the term "the shared resource is available for access" to mean "the shared resource is not in use by a processor and corresponds to a semaphore content of '0.'" The court construes "the shared resource is unavailable for access" as "a shared resource is in use by a processor and corresponds to a semaphore content of '1.'"

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[8]The inventor of the patent testified that "[t]he bus itself is a collection of wires that allow only one speaker at a time." (D.I. 223, ex. Y at 69:14-18)

The specification provides an illustration of the operation of the digital system. (*Id.* at 3:57-4:3) When a processor needs to access a shared resource, it reads a hardware semaphore cell into its register to determine whether the shared resource is available. A hardware semaphore content of "0" indicates that the resource is available for access. (*Id.*) Conversely a hardware semaphore content of "1" indicates that another processor is currently using the shared resource. (*Id.* at 5:38-41)[9] Assuming that the first processor then accesses the shared resource, "[w]hen the [first] processor finishes using the shared resource, the processor writes a '0' into the semaphore." (*Id.* at 2:3-5; 5:47-49; *see also* 4:22-24) A second processor, which had been waiting to access the shared resource, receives an interrupt signal. It can then determine that the release of the corresponding shared resource caused the interrupt. (*Id.* at 4:40-47; 6:11-13)

d. "The shared resource has just been made available for access"

The court construes this term as "the shared resource is no longer in use and has been released when a processor changes the content of the hardware semaphore cell to a '0.'" This construction is supported by the specification. "When the processor no longer needs access to the shared resource, the processor writes a '0' into the hardware semaphore cell." (*Id.* at 4:22-24) The second processor then receives an interrupt and it can determine that the release of the corresponding shared resource caused the interrupt. (*Id.* at 4:40-47; 6:11-13)

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[9]The background section of the '049 patent explains that a shared resource is available for access when both processors are not using the shared resource and the content of the semaphore is a "0." (*Id.* at 1:28-33)

e. "Cell"

The court adopts TI's construction "a portion of one register capable of storing a value." Figure 2 and the specification explain that the hardware semaphore cells, the semaphore interrupt cells, and the semaphore interrupt enable cells are each portions of the hardware semaphore register, the semaphore interrupt register, and the semaphore interrupt enable register, respectively. (*Id.* at 3:7-45)

2. Infringement

Cradle has accused TI's DSP chips of infringing apparatus claims 1-3 and method claim 6 of the '049 patent. (D.I. 278 at 11) TI's customers program the DSP chips by installing software that runs on the processing cores that comprise the chips. (*Id.* at 11-12) Each of the '049 accused products also includes a semaphore peripheral. (*Id.* at 12) To use the semaphore peripheral, a customer must install software on the chip. (*Id.*) The software must be programmed to acquire a semaphore in the semaphore peripheral by invoking one of three access modes: (1) the direct mode; (2) the indirect mode; or (3) the combined mode. (*Id.*)

Cradle alleges that the '049 products, without any additional software, infringe apparatus claims 1-3; and that method claim 6 is infringed when software running on an accused product acquires a semaphore using either (1) direct mode followed by indirect mode, or (2) combined mode. (*Id.*)

a. Apparatus claims 1-3

TI alleges that Cradle has not shown that TI has made, used, sold, or offered to sell the "entire patented invention" or that any of its customers have employed the

"entire patented invention in the required configuration set forth in the apparatus claims." (*Id.* at 13) The asserted apparatus claims require the claimed semaphore circuit to be **configured** so that each semaphore is mapped to or corresponds to a particular shared resource, such that reading a semaphore cell indicates whether a particular shared resource is available for access. (*See* '049 patent, 6:54-65) Without additional software, reading a semaphore would not indicate whether a particular shared resource is available for access and, thus, the products by themselves are not configured to monitor shared resource accesses by said processors. (D.I. 278 at 14) Cradle responds that there is no requirement that TI's customers add the software in order for the product to infringe the apparatus claim – that because the accused products include a hardware semaphore circuit, they are capable of performing the functions recited in the apparatus claim. (D.I. 284 at 16-17)

The law does not support Cradle's view. Because the apparatus claims require the "software [to] be configured in a particular way to infringe," infringement does not occur merely because the apparatus was capable of operating in an infringing fashion. *See Finjan*, 626 F.3d at 1204-05. Instead, Cradle must provide evidence of the software installed on the chip (apparatus) used in combined mode. As discussed below regarding the method claim, Cradle has not done so. There is no evidence to show that TI or its customers used the apparatus in combined mode. To the contrary, the only evidence provided shows that the software needed for the apparatus to operate in combined mode was not even developed. Based on the record, the court concludes

that Cradle has failed to identify evidence sufficient to raise a genuine issue of material fact as to infringement of the apparatus claims.

b. Method claim 6

TI further contends that Cradle has failed to provide evidence to show that either TI or its customers have actually performed "all of the steps of the claimed method." (D.I. 278 at 15; *see Akamai*, 692 F.3d at 1307) In support of its contentions, TI cites to subpoenas issued to its customers by Cradle confirming the lack of evidence of the programming or use of hardware semaphores in the '049 accused products. Alcatel-Lucent informed Cradle that it "found no evidence of use of hardware semaphores in TI's [DSP chips] incorporated in [Alcatel's] products." (D.I. 230, ex. 7) Ericsson provided a declaration stating that "the hardware semaphore peripheral in . . . [TI's] chip is not used." (*Id.*, ex. 10 at ¶ 4) Nokia Siemens Networks ("NSN"), following a motion to compel partially granted by this court, responded that "no employees in NSN US's Bedminster office . . . are knowledgeable about . . . whether hardware semaphores are employed in such devices." (*Id.*, ex. 9) Motorola Solutions, Inc. also submitted a declaration after the close of discovery, which has been stricken from the record.[10] (*Id.*, ex. 17)

In opposing TI's motion, Cradle attempts to identify a genuine issue of material fact by citing to circumstantial evidence relied on by Dr. Albonesi in reaching his conclusion that "the only rational conclusion is that the use of the hardware semaphore

[10]Even if not stricken, the declaration did no more than suggest that it had software capable of infringing; there is no averment (despite the clear opportunity to offer one) that such capability was ever utilized by Motorola Solutions, Inc.

peripheral module must be substantial." (D.I. 284 at 20; D.I. 230, ex. 1 ¶ 204) Notably, the only exhibits that suggest direct infringement are TI's e-mail communications with customer, Motorola, contemplating the development of a product using the combined mode, and one slide of a PowerPoint that TI presented to Motorola on the use of the combined mode. (D.I. 245, ex. 8-9) Cradle also points to the deposition of a TI field application engineer discussing his communications with a Motorola engineer who informed him that he was attempting to write code for a combo mode relying heavily on examples from the presentation. (*Id.* at ex. 11) The field application engineer did not know, however, whether Motorola was ever able to make the combo mode work. (*Id.* at 32) Dr. Albonesi did not review any customer software, or inspect or test any product incorporating the '049 accused products to determine whether the semaphore peripheral was used. (D.I. 230, ex. 2 at 135:20-136:2; ex. 8 at 60:15-61:3)

Accordingly, the court finds that Cradle has failed to identify evidence sufficient to raise a genuine issue of material fact as to infringement of the method claim. TI's motion for summary judgment of non-infringement with respect to the '049 patent is granted.

3. Invalidity

TI alleges that the asserted claims of the '049 patent are invalid because they fail to comply with the written description requirement, specifically, that the '049 patent does not describe a system that selects a subset of processors to receive the interrupts. (D.I. 234 at 37) Because the court has adopted TI's construction for "any processor requesting access to the shared resource" to mean "all processors

requesting access to the shared resource," TI's motion for summary judgment of invalidity for failure to comply with the written description requirement is moot.

B. The '259 patent

The '259 patent, "Programmable Wake Up of Memory Transfer Controllers in a Memory Transfer Engine," was filed February 1, 2002 and issued March 16, 2004. It claims priority from provisional application No. 60/266,002 which was filed on February 2, 2001. The '259 patent is assigned to Cradle. (D.I. 1 at ¶ 8)

The '259 patent relates to "[m]ethods for waking up an idle memory transfer controller (MTC) in response to an event from an external source." ('259 patent, Abstract) Independent claim 1 recites:

> 1. In a semiconductor chip, a method of waking up an idle memory transfer controller in response to an event from an external source, said method comprising:
>
> a) Writing to at least one hardware register of a memory transfer engine including a plurality of memory transfer controllers, said writing performed by an external agent; and
>
> b) activating an idle memory transfer controller so that it can execute instructions, said activation enabled by the writing step.

(*Id.* at 6:8-17)

1. Limitations of the '259 patent

a. "Idle Memory Transfer Controller"

Cradle and TI both propose constructions that could also define the inactive state of a MTC. These two states can be distinguished by the fact that, in the idle state, either the wake-up bit or the External WakeUp bit is set enabling the MTC to automatically wake up in response to a wake-up event. Accordingly, the court

construes this term as "a memory transfer controller that is not ready to execute instructions because its clock is stopped, i.e., the run bit is set to '0', and either the wake-up bit or the External WakeUp (XW) bit is set to '1.'"

The '259 patent refers to two wake-up mechanisms available to make an idle MTC ready to execute in response to a wake-up event. (*Id.* at 1:55-57; 2:56-59; 4:58-60) The first mechanism "activates the MTC's run bit, placing the MTC in a state where it can execute instructions." (*Id.* at 1:59-62) The specification explains that

> [t]he run bit helps control the MTC clock. When the run bit is one, the MTC clock runs and the MTC executes instructions. When the run bit is zero, the MTC clock is stopped and the MTC is stalled.

(*Id.* at 4:1-4) Figure 4 and the specification define what it means for a MTC to be idle. This occurs when "the wake-up bit is set to '1' and the run bit is '0' . . . ." (*Id.* at 4:47-52; *see also* 5:47-55) It further explains that "it will become ready if a wake-up event occurs." (*Id.* at 48-49) In contrast, when either the wake-up bit or the XW bit is '0,' the MTC is inactive. (*Id.* at 5:45-46; *see also* 4:50-52) The MTC's run bit is set to 0 in this state as well. (*Id.* at 4:50-52)

Figure 5 describes an external wake-up event during which time the run bit is set to "1." "When the run bit is set, the MTC is ready and eligible to be made executing in the next arbitration round." (*Id.* at 5:9-11; 5:55-57)

2. Infringement

Cradle has accused TI's OMAP 3, OMAP 4, OMAP 5, Centaurus and Netra chips of infringing method claims 1-3, 6, and 10-11 of the '259 patent. (D.I. 284 at 5, 32) These products include a Power Clock Reset Management ("PRCM") module that

controls the clocks to various initiator and target modules. (D.I. 228 at 8) When an initiator or target module is not needed, the PRCM – either automatically or if instructed by software to do so – can stop the clocks to that module, thereby placing the module in an "idle" state. (*Id.*) When a module is needed, the PRCM can similarly activate the module by turning on its clocks. (*Id.*)

The OMAP 3 products contain a static dependency feature. (D.I. 228 at 9) This feature is a relationship between an initiator module and a target module where the PRCM ensures that the target module is activated whenever the initiator module is also activated. (*Id.*) The static dependency feature can be enabled or disabled by TI's customers, but is enabled by default. (*Id.*; D.I. 278 at 29)

The OMAP 4 and OMAP 5 products further contain a dynamic dependency feature.[11] (*Id.*) This feature is a relationship between an initiator module and a target module where, if the PRCM senses a command being sent from the initiator module to the target module and, if the target module is idle, the PRCM will turn on the clocks of the target module. (*Id.*) Where a product has both features and the static dependency feature has been enabled, the static dependency feature controls and the dynamic dependency feature will never be exercised. (*Id.*)

Cradle alleges that: (1) the PRCM activates the accused memory controllers by turning on their clocks in the OMAP 4 and OMAP 5 products; and (2) the accused controllers activate themselves by turning on their own internal clocks in all accused

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[11]The Centaurus and Netra products contain neither feature. (D.I. 228 at 9)

products. (D.I. 278 at 28-30) The default setting in the accused products is that the PRCM-based clock gating strategy is off and the static dependency feature is on. (D.I. 278 at 31) Therefore, to prove infringement, Cradle must show that the PRCM-based clock gating strategy is turned on and the static dependency has been disabled.

Under the internal clock theory, Cradle must show that: (1) the accused "memory transfer controllers" implement the internal clock gating strategy; and (2) the internal clock gating strategy is on. (*Id.* at 32) Cradle has accused the dynamic memory manager (DMM), general purpose memory controller (GPMC), and external memory interface (EMIF) modules of being the accused memory controllers in OMAP4+.[12] (*Id.*)

a. Evidence of direct infringement by the OMAP 4+ products

TI contends that Cradle has provided no evidence to prove infringement by OMAP 4 and OMAP 5 under the PRCM-based theory or to prove infringement by OMAP 4+ under the internal clock theory. (D.I. 290 at 15) With respect to the PRCM-based theory, Cradle has failed to proffer evidence showing that any user of TI's products has changed the default setting to disable the static dependency feature. (D.I. 278 at 31) Cradle issued subpoenas to Motorola Solutions and Motorola Mobility, seeking documents relating to "the programming or use of the PRCM module to wake up" the target modules in end-products that incorporate the '259 Accused products. (D.I. 228 at 11) Cradle points to three pages of source code provided by Motorola Mobility as providing evidence that Motorola changes the default values of the accused

[12]Omap4+ refers to the OMAP4, OMAP5, Centaurus, and Netra products. (D.I. 278 at 28)

devices to allow sleep transitions to realize the power savings available by the PRCM automatic clock gating features. (*See* D.I. 245, exs. 20-22) However, at best the source code shows capability, but not use thereof.[13] TI's recommendation in its domain architecture document that certain memory modules, within the OMAP 3 products, be reconfigured to take advantage of the PRCM-based clock gating feature also does not provide evidence of use of the infringing mode by OMAP 4 and OMAP 5 products. (D.I. 287, ex. 79 at TI-CRAD-0096741)

Under the clock gating strategy, Cradle attempts to identify a genuine issue of material fact by again pointing to TI documentation to show evidence of direct infringement. (D.I. 284 at 32-34) That TI strongly recommends the use of autoidle mode for OMAP 3 products (not presently at issue) does not provide evidence of use of the allegedly infringing mode under the internal clock gating strategy. (*See* D.I. 287, ex. 79 at TI-CRAD-0096741) Neither does TI's technical reference manual stating that "[t]he EMIF can gate off the EMIF_FCLK. There is an internal mechanism which can stop the EMIF_FCLK automatically." (*Id*, ex. 23 at TI-CRAD-0124269)

Under either theory, the evidence shows that the products are, at best, capable of operating in an infringing manner. Infringement of a method claim, however, requires evidence of use. The court finds, therefore, that Cradle has failed to identify evidence sufficient to raise a genuine issue of material fact as to infringement by the OMAP 4+

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[13]Contrary to Dr. Albonesi's conclusion that a "large number of users of the OMAP 4 and OMAP 5 chips will disable the default static dependencies to reduce power consumption via the dynamic dependency mechanism," the Motorola Solutions declaration (stricken from the record) merely suggests capability, but not use. (D.I. 228, ex. 11 at App. B ¶ 16; D.I. 230, ex. 17)

products. Summary judgment of non-infringement is proper with respect to the OMAP 4+ products.

b. Infringement by the OMAP 3 products

TI has not carried its burden of persuasion with respect to the OMAP 3 products under the internal clock theory. The evidence cited by Dr. Hassoun (one sentence within the description of the features in the design specification for the clock tree generator), without further explanation or evidence, is not sufficient to support his conclusion that the OMAP 3 products "always keep one of their internal clock branches . . . on." (*See* D.I. 279 ¶ 10; ex. 27 at TI-CRAD-0875906) Further the parties present issues and arguments regarding the constructions of "execute instructions" and "writing."[14] Because there are genuine issues of material fact, summary judgment is denied as to the OMAP 3 products.

3. Invalidity

1. Anticipation

TI alleges that U.S. Patent No. 5,805,923 (the "923 patent") and the NS486SXF chip anticipate the asserted claims of the '259 patent under 35 U.S.C. 102(b). (D.I. 234 at 19-20) The '923 patent "discloses a configurable power management system that can be used in a controller for embedded systems." (*Id.* at 19) The NS486SXF chip embodies the invention disclosed in the '923 patent. (*Id.* at 20) Cradle responds that

[14]For example, in opposing TI's motion for summary judgment of invalidity, Cradle argued that the prior art memory transfer controllers do not "execute instructions" because they merely respond to the CPU's "address, data and control signals," which are not "instructions" within the meaning of the '259 patent. (D.I. 250 at 30-31)

there exist several factual disputes including whether the '923 patent and the NS486SXF chip disclose: (1) a "writing" to a hardware register; (2) "activating an idle MTC so that it can execute instructions;" and (3) that the activating is "enabled by the writing step." (D.I. 250 at 25-26)

The parties' experts disagree on whether the '923 patent and the NS486SXF chip disclose a "writing" to a hardware register. Cradle's expert contends that "setting a bit in a register as a result of a reset signal is not a writing because a reset is an individual signal line and does not involve a command or decoding any portion of a command." (D.I. 251, ex. 2 at Appx. B ¶ 36) TI's expert disagrees and contends that the "plain and ordinary meaning of writing is setting or resetting a register or changing the value of a register," and under this the '923 patent and the NS486SXF chip disclose "writing to at least one hardware register of a memory transfer engine." (D.I. 236 at ¶ 74; D.I. 264 at 15)

That the parties' experts do not agree on the plain and ordinary meaning of the term presents a genuine issue of material fact not properly resolved on summary judgment.[15] For this reason, the court does not address anticipation of dependent claims 2-3, 6, and 10-11, all of which depend on independent claim 1.[16] TI's motion for summary judgment is denied.

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[15]The parties make similar arguments related to the plain and ordinary meaning of the terms for the remaining disputed issues. (D.I. 250 at 26-33; D.I. 264 at 12-16)

[16]As the court finds a genuine issue of material fact with respect to anticipation, it does not reach TI's motion with respect to obviousness, as this argument is premised on a finding that the step of "writing to at least one hardware register of a memory transfer engine" is not disclosed in the '923 patent and the NS486SXF chip. (*See* D.I. 234 at 33)

C. The '450 patent

The '450 patent, "Multiprocessor Computer Systems With Command FIFO Buffer At Each Target Device," was filed October 6, 2000 and issued November 11, 2003. It claims priority from provisional application No. 60/158,184 filed on October 6, 1999. The '450 patent is assigned to Cradle. (D.I. 1 at ¶ 8)

Conventionally, a single transaction bus required that an entire transaction between two devices through the bus be complete before another transaction began. ('450 patent, 1:52-54) This led to the reduction of the data throughput of the computer system because, if the target device was slow in retrieving requested data, the bus was blocked and unused for a very long time. (*Id.* at 1:54-56)

To solve this problem and increase the efficiency of the system, a split transaction bus was devised. (*Id.* at 1:57-58) In a split transaction bus, "the transaction between the master and target devices is split in time into two transactions so that during the time in between the bus is free for use by other devices." (*Id.* at 1:62-2:2) Problems associated with split transaction buses occurred when a second master device sent a command to the same target device while it was busy retrieving data for the first. (*Id.* at 2:8-16) Such problems included the amount of bus time it cost to (1) send busy signals from the target device to the second master device and to (2) resend the transfer command from the second master device to the target device. (*Id.* at 2:14-21) Additionally, "the order of execution of transfer commands [was] not optimal, i.e. not first come first served." (*Id.* at 2:24-25)

To decrease the inefficiencies associated with the system bus of the prior art, the '450 patent provides "[a] multiprocessor computer system in which each processor being used as a target device has a FIFO (first in first out) buffer for receiving and storing transfer commands for a split transactional global bus for later execution." (*Id.* at Abstract) Independent claim 22 recites:

> A method of preventing a bus in a multiprocessor computer system from being blocked comprising:
>
> a) sending a command from a master device to a split transaction global bus;
>
> b) placing the command in a command FIFO of a target device;
>
> c) sending the master device an acknowledgement of command receipt;
>
> d) releasing the split transaction global bus for use by other bus devices, where such use includes another master device issuing a command accepted by the target device while the target device is executing a previously-issued transaction; and
>
> e) repeating steps a)—d) as necessary.

(*Id.* at 6:28-41) Dependent claim 26 includes the limitation "executing commands stored in a command FIFO on a first come first served basis. (*Id.* at 6:49-51)

1. Claim limitations

a. "Command FIFO"

Cradle argues that, although the preferred embodiment includes commands released in a first in, first out basis, the patentee did not intend to so limit the invention. (D.I. 206 at 22) TI responds that "command FIFO" is the centerpiece of the alleged invention. (D.I. 207 at 4) Because the specification includes ample evidence that the

command FIFO buffer executes its commands in a "first come first serve order," the court construes the term "command FIFO" as "a buffer of the target device in which commands are stored in the order of their arrival and taken out in that same order (First in, First out)."

The abstract of the '450 patent explains that transfer commands are "put in the FIFO of the target device in the order of their arrival and are taken out of the FIFO and executed by the target device in the same order." ('450 Patent, Abstract) The specification further highlights a problem associated with the split transaction global bus of the prior art – that "the order of execution of transfer commands [was] not optimal, i.e. not first come first served." (*Id.* at 2:24-25) Importantly, an object of the invention was "to provide a multiprocessor computer system in which the transfer commands from master devices to a target device are executed by the target device in a first come first serve order." (*Id.* at 2:34-37) The specification indicates that "[t]he transfer command will be taken out of the FIFO [buffer] and be executed by the target device in the same order [it was put in]." (*Id.* at 2:44-46)

Figure 5 and the specification in columns 4:31-54 illustrate how the command FIFO functions. Importantly, after a second command is sent to the target device, "[t]he second transfer command is put in command FIFO to be executed by target device after the execution of the first read command." (*Id.* at 4:43-45) Following the execution of the first read command, the "target device executes the second transfer command in a similar manner." (*Id.* at 4:52-54) Finally, the specification spells out that "commands in command FIFO will be executed in first come first served order." (*Id.* at 5:10-11)

With respect to Cradle's claim differentiation argument (D.I. 206 at 22-23), claim 26 further explains the execution of the command function on a first come first served basis. (*Id.* at 6:32-33) Claim 22, however, merely describes the action of "placing a command in a command FIFO of a target device." (*Id.* at 6:49-51)

b. "Split transaction global bus"

The court adopts TI's construction "a signal path shared by master and target devices in which one device has sole use of the path until it releases the path, wherein read transactions are split in time into two transactions." The specification defines a bus as "the means by which the electrical signals are communicated back and forth between a central processor, memory, and other devices . . . ." (*Id.* at 1:18-20) In a single transaction bus, "the entire transaction between two devices through the bus must complete before another transaction starts through the bus." (*Id.* at 1:51-54) To increase the efficiency of a system, the split transaction bus splits the transactions between the master and target devices in time into two transactions "so that during the time in between the bus is free for use by other devices." (*Id.* at 1:65-2:2) "Write transactions are still single transactions . . . ." (*Id.* at 2:2-3)

Figure 5 and the specification (in columns 4:30-54) describe how transactions are executed through the use of the global bus. The transaction begins when a first master device gets a bus use permit from a bus arbiter and sends a first read command through the global bus to the target device. After the first read command is put in command FIFO, the target device sends back to master device an acknowledgment of command receipt. "Upon receiving this acknowledgment, master device releases global

bus for use by other bus devices." (*Id.* at 4:37-39; 4:46-48) Although, as Cradle avers, the patent does not include the words "sole use" (D.I. 206 at 25-26), the description in the specification indicates that during the use of the bus by one device, it is unavailable for use by another.

c. "Acknowledgment of command receipt"

The court construes this term as "a signal generated by the target device to the master device, in response to receipt of the command, leading to release of the split transaction global bus by the master device for use by other devices." Cradle contends that the patent does not indicate what sends the acknowledgment to the master device. (D.I. 206 at 26) In illustrating how command FIFO operates, however, the specification does include the requirement that the target device sends the acknowledgment to the master device. (*See* '450 Patent at 4:31-54) This illustration explains that the "[t]arget device sends back to master device an acknowledgment of command receipt." (*Id.* at 4:35-37; 4:45-46) Further, "[u]pon receiving this acknowledgment, master device releases global bus for use by other bus devices." (*Id.* at 4:37-39; 4:47-49) The file history of the '450 patent provides additional support for this construction. To distinguish prior art in response to a rejection by the PTO, applicant argued that the invention teaches releasing a split transaction global bus for use by other devices "upon receipt of an acknowledgment of command receipt from the target device." (D.I. 201 at CIP 341-42)

d. "Releasing the split transaction global bus"

The court construes this term as "after receiving the acknowledgment, the master device releases the split transaction global bus for use by other bus devices." This construction finds support in several places in the specification. First, the claim itself recites "releasing the split transaction global bus for use by other bus devices . . . ." ('450 Patent at 6:36-37) Figure 5 and the specification illustrate that, "[u]pon receiving this acknowledgment, master device releases global bus for use by other bus devices." (*Id.* at 4:37-39; 4:46-48) Finally, during prosecution the applicant stated that the master device releases the split transaction global bus for use by other devices. (D.I. 201 at CIP 341-42)

e. Limiting preamble

The court agrees with TI that the preamble of claim 22 which recites, "[a] method of preventing a bus in a multiprocessor computer system from being blocked," is not limiting because it merely recites an intended use of the invention.

2. Infringement

Cradle has accused TI's OMAP 3, OMAP 4, OMAP 5, Netra, and Centaurus chips of infringing claims 22 and 24-30 of the '450 patent. (D.I. 284 at 5) "[T]hese chips contain initiator modules and target modules, which are connected to each other through an L3 interconnect." (D.I. 228 at 13) Cradle alleges that the accused "split transaction global bus" is the L3 interconnect and the OCP interfaces connected to it. (D.I. 278 at 6)[17]

[17]Cradle also alleged that the accused "split transaction global bus" may be an OCP interface between the L3 interconnect and the target device. This theory was

TI contends that no device has sole use of the "split transaction global bus," which includes the L3 interconnect, as "[m]ultiple devices can use the L3 interconnect simultaneously because it has: (1) crossbar switches and (2) independent request and response networks." (D.I. 278 at 3; D.I. 279 at Pt. A ¶ 11) A review of the evidence[18] cited by TI indicates that multiple crossbar switches in both the OMAP 3 and OMAP4 + products are used to allow multiple connections between multiple master and target devices. (*See* D.I. 279 at Part A, ¶¶ 13-16; ex. 37; ex. 51-52; D.I. 280, ex. 13) TI's products, therefore, do not require that only one device has sole use of the path until it releases it for use by other devices.

Cradle fails to identify evidence to support a finding of a genuine issue of material fact, instead pointing only to a conclusory opinion, unsupported by evidence, in Dr. Albonesi's declaration. According to Cradle's expert, "even though multiple devices may have commands pending on the L3 interconnect at any given time, only a single command from a single master device can be issued at a time through the target OCP interface and only one command can traverse the target OCP interface at a time." (D.I. 285 at ¶¶ 155, 220-21 (citing generic timing diagrams)) Because TI provides evidence to show that its products do not meet the "split transaction global bus" limitation, and Cradle has failed to rebut this with actual evidence to show otherwise, the accused products do not infringe the '450 patent.

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subject to TI's motion to strike untimely expert opinions cited in Dr. Albonesi's declaration. (D.I. 295) As the motion was granted, this theory will not be addressed.

[18]Including a white paper describing the Arteris chip, a description of the components and performance of SonicsMX interconnect, and specification of the L3 interconnect.

Similarly, the court finds no genuine issue of material fact as to whether the accused structures are equivalent under the doctrine of equivalents. Cradle asserts that the structures are equivalent to the claimed split transaction global bus because they perform the same function (transmitting split read transactions) in substantially the same way (from master to target, where no other master can send a command to the same target) and achieve substantially the same results (the command is sent to the target and then the split transaction global bus is released for use by the other master devices to send a command to the same target). (D.I. 284 at 7; D.I. 285 at ¶ 156) However, as described above, the crossbars are more complex and provide a higher throughput, as they allow multiple devices to send commands and data simultaneously. As such, the differences between the "split transaction global bus" limitation and the accused structures are not insubstantial.[19] The court finds that Cradle has failed to identify evidence sufficient to raise a genuine issue of material fact as to infringement of the '450 patent. TI's motion is granted.

3. Invalidity

a. Anticipation

TI alleges that U.S. Patent No. 5,546,546 (the "546 patent") anticipates the asserted claims of the '450 patent under 35 U.S.C. 102(b). (D.I. 234 at 3) The only disputed issues are: (1) whether the In-Order Queue is a "command FIFO;" and (2) whether the response sent by the target device after it receives a command, and before

[19]Because the court finds summary judgment is appropriate, it does not address the "infringement by proxy" theory that Cradle uses in support of its infringement arguments for the limitation "acknowledgment of command receipt" (D.I. 284 at 11) and discussed in TI's motion to exclude Dr. Albonesi's testimony (D.I. 227).

it supplies the requested data or completion signals, is an "acknowledgment of command receipt." (*Id.* at 7)

The parties' dispute centers on whether the entries in the In-Order Queue are "commands" within the meaning of claim 22. (*Id.* at 9; D.I. 236 at ¶¶ 35-36, 40; D.I. 251, ex. 2 at App. A ¶¶ 24-30) In particular, the parties' arguments rely on their experts' differing interpretations of Figure 3 in the '546 patent. (*See* D.I. 236 at ¶¶ 35-36, 40; D.I. 251, ex. 2 at App. A ¶¶ 24-30) With respect to the second issue, the parties again differ in their reading of Figure 3. Although TI's expert explains that the '546 patent discloses this limitation, Cradle's expert argues that the response will be generated when the responding agent is ready to complete a deferred bus transaction, not when a command is received. (D.I. 236 at ¶37; D.I. 251, ex. 2 at App. A ¶¶ 31-35)

Because the court finds a genuine issue of material fact regarding whether the '546 patent anticipates independent claim 22 of the '450 patent, it does not consider anticipation of dependent claims 24-30. TI's motion is denied.

b. Obviousness

TI further asserts that the '546 patent renders the asserted claims of the '450 patent obvious, alleging that it would have been obvious to one of skill in the art at the time of the invention to modify the In-Order Queue to store commands. (D.I. 234 at 16-17; D.I. 236 at ¶¶ 50-51) Cradle asserts that TI did not consider the secondary considerations of non-obviousness, as discussed by Dr. Olivier. (D.I. 226, ex. 1 ¶¶ 52-53) A court is required to consider secondary considerations, or objective indicia of non-obviousness, before reaching an obviousness determination, as a "check against

hindsight bias." *See In re Cyclobenzaprine Hydrochloride Extended-Release Capsule Patent Litig.*, 676 F.3d 1063 (Fed. Cir. 2012). TI is correct that Cradle did not present these considerations in its briefing. (D.I. 264 at 9-10)

As TI's burden of proof is one of clear and convincing evidence and the existence of secondary considerations of non-obviousness represent factual inquiries to be determined by a fact-finder, summary judgment of invalidity is denied.

VI. Conclusion

For the foregoing reasons, the court grants in part and denies in part TI's motion for summary judgment of non-infringement and denies its motion for summary judgment of invalidity of the patents-in-suit. (D.I. 217; D.I. 218) The court denies TI's motion to exclude the testimony of Dr. Olivier. (D.I. 224) The court denies as moot TI's motion to strike the testimony of Dr. Albonesi. (D.I. 227) The court grants Cradle's motion to strike the declaration and testimony of Michael Shay. (D.I. 271) The court grants TI's motion to strike inadmissible evidence and untimely expert opinions. (D.I. 295) The court denies Cradle's motion to strike new expert opinions. (D.I. 309) The court grants in part and denies in part TI's motion to strike untimely expert opinions. (D.I. 315) An appropriate order shall issue.