IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF DELAWARE

ROUND ROCK RESEARCH, LLC,	)	
	)	
Plaintiff,	)	
	)	
v.	)	Civ. No. 12-569-SLR
	)	
SANDISK CORPORATION,	)	
	)	
Defendant.	)	

MEMORANDUM ORDER

At Wilmington this 21st day of July, 2014, having heard argument on, and having reviewed the papers submitted in connection with, the parties' proposed claim construction;

IT IS ORDERED that the disputed claim language of U.S. Patent Nos. 5,615,159 ("the '159 patent"), 6,728,798 ("the '798 patent"), 6,948,041 ("the '041 patent"), and 8,060,719 ("the '719 patent") shall be construed consistent with the tenets of claim construction set forth by the United States Court of Appeals for the Federal Circuit in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005), as follows:

1. **"Control means for generating control signals for controlling operations of the system:"**[1] The parties do not dispute that the corresponding function is: "Generating control signals for controlling operations of the system, said operations including programming the memory cells and reading the memory cells." The corresponding structure is: "Command execution logic unit and state machine, and equivalents thereof." This structure is consistent with the specification, which links the

[1]Claim 1 of the '159 patent.

state machine and command execution logic components of the control unit to the claimed function. (*See* '159 patent, cols. 7:52-8:3; 8:20-23; fig. 2)

2. **"Default parameter means coupled to the data storage unit for outputting default parameter data rather than the control parameter data in response to a first control signal from the control means:"**[2] The parties do not dispute that the corresponding function is: "Outputting default parameter data rather than the control parameter data in response to a first control signal from the control means." The corresponding structure is: "A control signal wire electrically coupled to an inverter, where the output of the inverter is electrically coupled to the first input of an AND gate, and where the second input of the AND gate is electrically coupled to the data storage unit; or control signal wire coupled to the data storage unit; and equivalents thereof." The specification links the above function with the structure of figures 8 and 9. (*See* cols. 22:66-23:17 and fig. 8; cols. 23:55-24:7 and fig. 9) The specification further teaches that the default parameter means operates in several modes including a "test mode." (*See* cols. 3:18-55 (describing other non-test mode applications); 23:45-55 (describing multiple modes))

3. **"Control data word:"**[3] "A group of bits representing data." This construction is consistent with the language of the claims and the specification. (*See* '041 patent, cols. 2:59-62; 3:1-7 ("The control data word is comprised of eight control bits."); fig 2. *See also* col. 8:8-9 ("the control data word comprises a "plurality of bits")) The claim

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[2]Claim 1 of the '159 patent.

[3]Claims 1, 18, and 27 of the '041 patent.

language expressly identifies the "control" aspect of the data word – it "indicates which memory blocks to protect." (*See id.* at cols. 6:8-12; 7:45-48; 8:37-40)

4. **"[M]emory block:"**[4] "A division of the flash memory that is designed to be erased in response to an erase operation." This construction is supported by the specification, which indicates that blocks of memory are selectively erased. (*See id.* at col. 1:25-28)

5. **"[A]n unused control address:"**[5] "An address that is not being used by other functions of the memory device." This is consistent with the specification, which provides that "[t]he control data word that indicates which memory blocks to secure is then written to an address that is not being used by other functions of the memory device." (*Id.* at col. 4:17-19)

6. **"[Y]-cycles" / "y-clock cycles:"**[6] "0-7 clock cycles." This construction is supported by the specification, which indicates that "[t]he memory can also provide the register data in accordance to a defined clock latency value." ('798 patent, Abstract; col. 28:24-26. *See also* col. 2:34-35 "Outputting the register data is delayed for a predefined clock latency period after receiving the register read command.") The specification expressly provides that "[t]he latency can be set to one, two, or three clock[] cycles." (*Id.* at col. 8:28-34) Figures 3, 7, 8, and 10 show examples of latencies of 1, 2, and 3. Figure 2B shows a "reserved" range allowing for latencies of 0 to 7.

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[4]Claims 1, 18, and 27 of the '041 patent.

[5]Claims 18 and 27 of the '041 patent.

[6]Claims 2 and 6 of the '798 patent.

Absent such boundaries supported by the specification, this limitation would be rendered indefinite for failure to "inform those skilled in the art about the scope of the invention with reasonable certainty." *Nautilus, Inc. v. Biosig Instruments, Inc.*, 134 S. Ct. 2120, 2129 (2014).

7. **"[D]etermining usage associated with a logical address" / "to determine usage data of a logical address:"**[7] "Determining [to determine] the number of actual or predicted operations performed on, or the time at which the operations are performed on, a logical address." Generally, the specification provides that data is allocated to the appropriate storage (SLC or MLC) as a result of the actual prior usage or predicted usage. (*See, e.g., id.* at cols. 4:14-20; 5:58-62; 6:3-5) More specifically, however, the specification provides examples corresponding to storing usage data according to the operations performed or the frequency at which data is sent to a particular type of storage. (*See id.* at cols. 4:6-14; 4:62-5:5; 5:10-19; 9:24-33; 12:1-11, 20-23)

The court has provided a construction in quotes for the claim limitations at issue. The parties are expected to present the claim construction to the jury consistently with any explanation or clarification herein provided by the court, even if such language is not included within the quotes.

United States District Judge

[7]Claims 1 and 28 of the '719 patent.