Intellectual Ventures I LLC et al v. Toshiba Corporation et al Doc. 277

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

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| INTELLECTUAL VENTURES I LLC and INTELLECTUAL VENTURES II LLC, | ) | |
| Plaintiffs/Counterclaim Defendants, | ) | |
| v. | ) | Civ. No. 13-453-SLR |
| TOSHIBA CORPORATION, TOSHIBA AMERICA, INC., TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC., and TOSHIBA AMERICA INFORMATION SYSTEMS, INC., | ) | |
| Defendants/Counterclaim Plaintiffs. | ) | |

**MEMORANDUM ORDER**

At Wilmington this 17th day of December, 2015, having heard argument on, and having reviewed the papers submitted in connection with, the parties' proposed claim construction;

IT IS ORDERED that the disputed claim language of U.S. Patent Nos. 5,701,270 ("the '270 patent"); 5,568,431 ("the '431 patent"); 5,600,606 ("the '606 patent"); 5,829,016 ("the '016 patent"); 5,500,819 ("the '819 patent"); 7,836,371 ("the '371 patent"); 5,938,742 ("the '742 patent"); 6,618,788 ("the '788 patent") shall be construed consistent with the tenets of claim construction set forth by the United States Court of Appeals for the Federal Circuit in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005), as follows:

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## The '270 Patent

1. **"First and second banks of memory:"**[1] "First and second arrays of memory." **"Plurality of memory banks:"**[2] "Two or more arrays of memory." The specification explains that:

> [F]rame buffer 104 is partitioned into a selected number of memory blocks 200. In the illustrated embodiment, four memory blocks 200a-200d are provided each of which contains an array of memory cells arranged as X number of rows and Y number of columns and configured, output at n-bit words per address. Each memory block is associated with an address decoder 201.

(7:17-24) The patent refers to "multi-bank systems" and describes "inter-bank row/column replacements," i.e., replacing defective row/columns with redundant row/columns from another bank. (13:58-62) The specification and claim language[3] explain that each array is made up of "a predetermined number of primary memory cells and a predetermined number of redundant memory cells." This language further illustrates that the memory banks are delineated from one another in a "predetermined" fashion.

2. **"Redundant memory cells:"**[4] "Additional memory cells that are designed only for use in replacing defective primary memory cells." The invention's "principles allow for the replacement of a defective row or column of a given bank with a row or column of any other bank or array in the memory subsystem. This feature

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[1] Found in claim 1.
[2] Found in claim 20.
[3] Claim 1 recites in part "first and second banks of memory, each said bank including a predetermined number of primary memory cells and a predetermined number of redundant memory cells," and claim 20 recites "a plurality of memory banks each comprising an array of memory cells, each said array including a preselected number of primary cells and a preselected number of redundant memory cells."
[4] Found in claims 1-2 and 20.

advantageously allows for the optimal use of the **available redundant cells** thereby allowing for increased chip yield." (5:21-26; *see also* 4:22-27) (emphasis added) In one embodiment, "each memory bank includ[es] a predetermined number of primary memory cells and a predetermined number of redundant memory cells." (4:33-36) In another embodiment, "each array includ[es] a preselected number of primary rows and columns and a preselected number of redundant rows and columns. . . . Second address logic is included for addressing the redundant rows and columns in response to bits presented by the processing circuitry on a redundancy bus." (4:44-52) The specification also states that "each memory block includes a number of redundant cells . . . for repairing defective cells by substitution." (7:29-33)

3. **"Allowing said processing circuitry to address at least one of said primary [redundant] memory cells:"**[5] "Allowing said processing circuitry to access at least one of said primary [redundant] memory cells." The specification explains that processing circuitry is used to address the memory cells. (4:37-40, 47-52) For example,

> a defective set of memory cells is identified in a first one of the banks, the defective memory cells associated with a bank select bit and a location address bit and addressable by the controller by a primary address bus. A redundant set of memory cells is programmed in a second one of the banks, the redundant set of cells addressable with a bank select bit, a primary location address bit, and a redundancy address bit by the controller via a redundancy address bus. Access is then steered from the defective set of cells to the corresponding redundant cells by addressing the redundant set of cells via the redundancy bus.

[5] Found in claim 1. The parties presented the shortened limitation "to address at least one of said primary [redundant] memory cells" for construction.

(5:7-18) During prosecution, the applicant distinguished the Park reference[6] on several grounds, including that "[c]laim 1 . . . calls out for accesses on a **cell** basis, a feature which is clearly not possible with Park." (D.I. 207, ex. 9 at A262) The court disagrees with Toshiba that such a statement warrants the additional proposed language "on a single cell basis." Indeed, the portion of the specification quoted above teaches addressing a set of cells.

4. **"Redundancy bus:"**[7] "Address bus that allows for the addressing of the redundant memory cells independent of the addressing of the primary memory cells through the primary address bus." The specification explains that "[a]n address bus is included for allowing a processing circuitry to address at least one of the primary memory cells. A redundancy bus is provided for allowing the processing circuitry to address at least one of the redundancy cells." (4:36-40) The description of figure 2 makes no reference to a "redundancy bus" or a "redundancy address bus." Figure "3 is a high level functional block diagram of a second integrated controller – memory device 300 according to the principles of the present invention. Integrated device 300 **further** includes a k-bit wide redundancy address bus 301." (9:53-54) (emphasis added)

> Redundancy bus 301 and the additional redundancy bits presented thereon, advantageously allow for the steering of an access directed to a defective row or column in one bank 200 to good row in another bank 200. Specifically, redundancy bus 301 allows for addressing of the redundant rows/columns 205 independent of the addressing of the primary rows and columns through address bus 202.

(12:33-40)

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[6] U.S. Patent No. 5,469,388.
[7] Found in claims 1, 3, and 20.

5. **"Redundancy cell memory space separate from said primary cell memory space:"**[8] "Address set for redundant memory cells separate from the address set for primary memory cells." The specification explains that the invention "allow[s] for the replacement of a defective row or column of a given bank with a row or column of any other bank or array in the memory subsystem." (5:20-24)

> Specifically, redundancy bus 301 allows for addressing of the redundant rows/columns 205 independent of the addressing of the primary rows and columns through address bus 202. The redundancy address bits increase the size to the address set (space) to each bank to accommodate unique addressing of redundant rows/columns. Hence, even if the lower order address bits are identical for a good primary row/column and a programmed redundant row in the same bank, the redundancy address bits Rz insure that an access is not steered to multiple rows/columns during replacement.

(12:37-47)

> Specifically, in multi-bank systems, inter-bank row/column replacements can be implemented, thereby allowing the available redundancy resources to be put to their best use. For example, if all the redundant rows/columns of one bank have been used for repairs, yet redundant rows or columns remain in another bank, the first bank can still be repaired and the full capability of the overall device maintained as a result.

(13:60-67) As previously discussed, the prosecution history distinguishes the Park reference on several grounds, including that the Park reference "does not disclose or suggest [the] partitioning of the primary and redundant cells into separate memory spaces." Moreover, "block to block replacements are not even possible" in the Park reference, instead, "replacements can only be made within single blocks." (D.I. 207, ex. 9 at A261-262)

[8] Found in claim 1.

**The '431 Patent**

6. **"A plurality of arrays of memory cells:"**[9] "Two or more arrays of memory cells." The specification describes a memory array as "an array of rows and columns of memory cells." (2:53-58) More specifically, the memory array "includes an array 202 of storage cells 203 arranged in M number of rows and N number of columns. (5:61-63)

7. **"A plurality of registers:"**[10] "Two or more registers, each register exclusively associated with an array of memory cells." The entire limitation at issue recites "a plurality of registers, each of said registers for exchanging parallel bits of data with a corresponding one of said arrays." **"Data transfer circuitry for transferring parallel bits of data from any selected one of said arrays through the corresponding said register to any other selected one of said arrays through the corresponding said register."**[11] The court adopts Toshiba's proposal and constrains this limitation in that "the first 'said register' is not the same register as the second 'said register' recited in the claim."

8. The parties dispute whether two memory arrays may share the same register. IV relies on *Hill-Rom Servs., Inc. v. Stryker Corp.*, 755 F.3d 1367 (Fed. Cir. 2014), to argue that while the specification does not provide an embodiment with shared registers, the claim language does not support the restriction of claim scope to the described embodiment, wherein each memory bank has its own shift register. A court should "depart from the plain and ordinary meaning of claim terms based on the specification in only two instances: lexicography and disavowal." *Id.* at 1371.

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[9] Found in claim 1.
[10] Found in claim 1.
[11] Found in claim 1.

"Disavowal requires that 'the specification [or prosecution history] make[ ] clear that the invention does not include a particular feature,' or is clearly limited to a particular form of the invention." *Id.* at 1372 (internal citations omitted).

> [A]bsent some language in the specification or prosecution history suggesting that the [limiting language] is important, essential, necessary, [f]or the 'present invention,' there is no basis to narrow the plain and ordinary meaning of the term . . . . There are no magic words that must be used, but to deviate from the plain and ordinary meaning of a claim term to one of skill in the art, the patentee must, with some language, indicate a clear intent to do so in the patent.

*Id.* at 1373. The patent at bar seeks to improve the speed of block data transfers between address spaces. (2:11-19) The specification explains that

> [e]ach memory unit is coupled to one parallel port of a corresponding shift register. A second parallel port of each shift register is coupled to interconnection circuitry, such as a bus. Under the control of associated control circuitry, data may be exchanged between a given memory unit and one or more other such memory units via the corresponding shift registers and the interconnection circuitry.

(2:30-36) The embodiments describe using a register "coupled to the selected memory unit" and "a plurality of shift registers each for controlling the exchange of data with a respective subsystem." (2:47-50; 58-60) Figure 2, "a functional block diagram of a memory according to the principles of the present invention," illustrates a separate shift register coupled to each memory array. The court concludes that the claim language read in light of the specification suggests that each memory array is coupled to its own register. *Fenner Investments, Ltd. v. Cellco P'ship*, 778 F.3d 1320, 1322-23 (Fed. Cir. 2015) ("The terms used in patent claims are not construed in the abstract, but in the context in which the term was presented and used by the patentee, as it would have been understood by a person of ordinary skill in the field of the invention on reading the patent documents.").

9. **Extrinsic evidence.** IV's expert, Dr. Huber, concludes that the claim language indicates to a person of ordinary skill in that art that the registers may be the same register. He further opines that "using a shared register for the transfer would further the goals of the patent regarding speed and efficiency because that would require fewer steps than using multiple registers." (D.I. 233 at ¶ 19) Toshiba's expert, Dr. Subramanian, opines that the claim language indicates to a person of ordinary skill in the art that "the source address space and the destination address space reside within different memory arrays," each array is coupled to a different register, and the "data transfer circuitry is used to transfer the data between the register coupled to the source array and the (different) register coupled to the destination array." (D.I. 202 at ¶ 19) Moreover, "[o]ne of ordinary skill in the art would have understood that if the source array and the destination array were associated with a common register, then data could be transferred from the source array to the destination array through the common register, bypassing the data transfer circuitry." (*Id.* at ¶ 21) In the context of the '431 patent, this would render the data transfer circuitry (and the invention) unnecessary. "Therefore, each register recited in claim 1 must be exclusively associated with an array of memory cells." (*Id.*) Evaluating the claim language in the context of the specification's description of the prior art and invention, the court finds Toshiba's expert more persuasive in this instance.

**The '606 Patent**

10. **"Substantially simultaneously inputting said row address bit and column address bit:"**[12] "Inputting said row address bit and column address bit at

[12] Found in claim 1.

substantially the same point in time." The specification describes a method of operating a memory device, where "[a]t least one row address bit and at least one column address bit are substantially simultaneously input during an address cycle." (Abstract; 2:32-34, 41-42, 49-51) The specification describes "serial" addressing – "row and column addresses received at pins 220 and 230 may be word serially received (i.e., row address bits received as a word and column address bits received subsequently as a separate word) from a conventional multiplexed address bus" (6:20-24) – and uses the language "substantially simultaneously" to distinguish it.

> Memory system 600 is substantially similar to memory system 200, with the primary difference being that a non-multiplexed addressing scheme is used. In other words, during each random access, instead of receiving and latching-in the row address with $\overline{RAS}$ and subsequently receiving and latching in the column address with $\overline{CAS}$, all row and column address bits are received from the associated data bus and latched-in substantially simultaneously.

(8:22-31) The specification describes using both "address dedicated pins 220 and the multiplexed address/data pins 230" to input row and column address bits for the operation of the memory devices. (6:64-7:1; *see also* 8:66-9:5)

11. **"Column address:"**[13] "the address of a column in the array." The specification describes pins receiving "row and column addresses" (6:19-28); the memory device waiting "for a new set of row and column addresses" (7:22-24); and inputting "row and column addresses" (7:25-26).

[13] Found in claim 1.

## The '016 Patent

12. **"Command and control cycle:"**[14] "Command and control mode." The specification explains that "a memory is provided which includes a plurality of input/output terminals for exchanging data bits during a data access cycle and receiving command and control bits during a command and control cycle." (2:49-52) The "input/output port (pins) 220, labelled IO(0:31), input or output data during a data access mode (cycle) and receive command, control and address bits during a command and control mode (cycle)." (6:42-46; *see also* 7:9-11) The specification describes the timing scheme:

> In some operations, such as setting the burst and page latencies or setting the mask, the command and control cycle may not be immediately followed by a data access cycle. In such cases, memory 200 idles or resumes its previous data stream as appropriate until another command opcode is received and decoded, either during a new command/control cycle initiated by [a command bit] or during the same command/control cycle.

(9:49-56) During prosecution, the applicant distinguished the Farmwald reference[15] (which required serial transmission of the addresses on the bus to the identified device), arguing that it

> does not disclose a system whose addressees, opcodes and control signals are input during one cycle and data are accessed in another. . . . [The Farmwald reference] defeats the advantages of the present invention, which include the ability to load information for control addressing, and operations, and then simply performing data accesses through the same pins. No serial address pipelining is required with the present invention as in [the Farmwald reference].

(D.I. 208, ex. 12 at JA625)

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[14] Found in claims 1, 26, and 27.
[15] U.S. Patent No. 5,408,129.

13. **Extrinsic evidence.** Toshiba's proposed construction limits the "command and control cycle" to "a single clock cycle." Toshiba's expert, Dr. Baker, opines that figures 3A and 3B "show that the command opcodes, addresses and control bits of claim 1, and the command opcodes and pointer bits of claim 26, are input to the memory through the multiplexed input/output terminals . . . **during a single clock cycle**." (D.I. 203 at ¶ 18) As to the prosecution history discussed above, Dr. Baker explained that

> [s]erial pipelining entails inputting (or outputting) information over multiple clock cycles. . . .
> . . . In contrast, if a piece of information is input in parallel, it is not divided into words, but rather input all at once in a single clock cycle. A person of skill in the art . . . would . . . conclude that the '016 patent does not include serial address pipelining over multiple clock cycles.

(*Id.* at ¶¶ 29-30)

14. Dr. Huber disagreed and opined that the "patent equates the terms 'cycle' and 'mode' in the specification" and "a single clock cycle is referred to as CLK." (D.I. 233 at ¶ 26) Moreover, claim 1

> requires that addresses, command opcodes, and control bits are received during a command and control cycle. One of ordinary skill in the art at the time this patent was filed would understand that a "command and control cycle" could take more than a single clock cycle (CLK), and would not understand the "cycle" aspect of this term to refer to a single clock cycle. Instead, "cycle" indicates an operating mode.

(*Id.*) Dr. Huber explained that the specification's description of a preferred embodiment ("a command bit (CMD) which is received through a selected input (pin) controls and times the address/control and data access modes" (6:50-53)) means that

> the durations of the various modes are controlled by a command bit and are not limited to a single clock cycle (CLK). For example, 9:49-56 provides an example where a command opcode is received, followed by an idle period, and then, "another command opcode is received and

> decoded, either during a new command/control cycle initiated by CMD or during the same command/control cycle."

(*Id.*) Dr. Huber additionally opines that the disputed prosecution history "does not support the notion that a command and control cycle is a single clock cycle, and does not mention 'CLK' or 'clock cycle.' The distinction . . . was not directed to one clock cycle vs. multiple clock cycles, but instead on the presence or absence of multiplexed pins." (*Id.* at ¶ 27) The court finds Dr. Huber's explanations more consistent with the specification's disclosures and the prosecution history and, therefore, more persuasive.

15. **"Addresses:"**[16] "Bits that identify locations in an array of memory cells." The specification states that "[t]he page pointer bits select one row in array 201 and the burst pointer bits select at least one initial w-bit wide location along that row for access." (10:6-8) Moreover, "[a]fter a delay of a pre-determined number of master clock cycles, to allow for sense amplifiers 203 to set-up, 32-bit words of data can be read or written to/from locations of the selected page (row) . . . ." (10:24-27)

16. **"Receiving addresses."**[17] The parties disagree on whether the limitation should exclude "serial address pipelining." For the reasons discussed above in paragraphs 12 and 13, the court concludes that the applicant did not disclaim "serial address pipelining" in distinguishing the Farmwald reference.

**The '819 Patent**

17. **"Sensing the bitlines of the array to read data stored in the cells of the selected row with a bank of master sense amplifiers:"**[18] "Detecting and amplifying a

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[16] Found in claim 1.
[17] Found in claim 1.
[18] Found in claim 17. The parties submitted "sensing the bitlines of the array to read data stored in the cells" for construction.

voltage level on each of the bitlines of the cells for reading data using sense amplifiers." The memory system of the invention uses "master sense amplifier circuitry for reading and writing data into . . . selected cells." (2:55-57) The "bank of master sense amplifiers is coupled to the bitlines." (3:18-19) "Mode control circuitry 214 receives mode control signals from input circuitry 206 and provides in response wordline timing and control signals to row decoder 205 and sense timing and control signals to master sense amplifiers 208." (6:15-18) "A first row to be read is selected by activating the associated wordline. The bitlines are then sensed with a bank of master sense amplifiers to read the data stored in the cells of the first row." (3:55-58) The specification also describes an example wherein, "[i]n a random access (read or write) to the cells" of a memory array, "the master sense amplifier bank 208 sets the selected bitlines 204 to the proper voltages." (6:24-25, 33-35)

18. **Extrinsic evidence.** The parties' experts offer competing opinions regarding whether the limitation's construction should require "amplifying a voltage level on each of the bitlines." Dr. Huber opines that bitlines are sensed. Moreover, he disagrees that "sensing" must include amplifying the voltage, concluding that this would be a separate step not recited in the claim and not discussed by the patent. Dr. Huber opines that "there are multiple types of sense amplifiers, including notably differential voltage sense amplifiers, current mirror sense amplifiers, and inverters," and that Toshiba's construction would exclude "the entire class of sense amplifiers that detect the differential voltage on a pair of bitlines." (D.I. 233 at ¶¶ 31-32; D.I. 253 at ¶ 10)

19. Mr. Murphy, Toshiba's expert, explains that "[a] sense amplifier senses the bitline by detecting the slightly changed bitline voltage level and amplifying that voltage

level to a proper, full voltage representing the 'high' or 'low' logic value stored in the cell." (D.I. 204 at ¶ 12) To a person of ordinary skill in the art, "the term 'sensing' means detecting **voltages** set on the bitlines by memory cells . . . ." (*Id.* at ¶ 13) More specifically, Mr. Murphy describes:

> When the data in a particular memory cell is read, that memory cell alone is coupled to the bitline, inducing a change in the bitline voltage, the direction of the change corresponding to the data value stored in the cell. Because memory cells are so small, and the bitlines relatively large, the memory cell is only capable of inducing a very small change in the bitline voltage. Before other circuits can recognize what data this small change represents, the small change must be amplified to a full "low" or a full "high" voltage level. Detection alone is insufficient to sense the data stored in the cells by master sense amplifiers. Sensing the bitlines of the array to read data stored in the cells requires both **detecting** and **amplifying** a voltage level on each bitline, to read the data stored in the cells.

(D.I. 244 at ¶ 6) As to the different types of sense amplifiers, Mr. Murphy explains that "[w]hile the different types of sense amplifiers operate differently, they all sense a small sense voltage and output a full 'low' or a full 'high' voltage level. Therefore, Toshiba's construction is inclusive of all types of sense amplifiers." (*Id.* at ¶ 8)

20. The parties additionally provide a textbook reference[19] which explains that read circuitry "involves the use of a sense amplifier to read the low level of signal from the cell. A simple invertor can be used as a sense amplifier, however, a pair of single-ended differential sense amplifiers are used in the case shown in Figure 5.8 since they can sense and amplify a very small difference between the level on the bit and $\overline{\text{bit}}$ lines." (D.I. 201, ex. G at TOSH-IV213008; *see also* D.I. 232, ex. D) The court finds Mr.

[19] Betty Prince, *Semiconcuctor Memories: A Handbook of Design, Manufacture, and Application* (2nd ed. 1991).

Murphy's explanations more persuasive in the context of the patent and extrinsic evidence.

21. **"Writing the data:"**[20] "Transferring said amplified voltage level to the bitlines for writing data." The specification states that to write data, "[f]irst data is latched in a first bank of slave sense amplifiers. This first data is then written into first selected cells in the array." (4:3-5) To write entire rows, data inputs and writes to the array are alternated "until a desired block of data has been written. Preferably, each slave sense amplifier bank 210 and 211 includes write driver (buffer) circuitry which provides sufficient write voltage drive to cause master sense amplifiers 208 to latch the proper write voltages and transfer these voltages to the bitlines 204."[21] (7:32-38)

**The '371 Patent**

22. **"System operation signals during normal system operation:"**[22] "Signals internal to the integrated circuit when the integrated circuit is operating normally."

**"System operation signals on said system bus during normal system operation:"**[23] "Signals internal to the integrated circuit on said system bus when the integrated circuit is operating normally." The abstract provides that "[t]est and debug circuits may be designed to observe states in user-definable circuits during the normal system operation of said user-definable circuits." (Abstract) According to the invention, "a Service Processor Unit (SPU) is incorporated within an integrated circuit" (IC) and used to address "the problems of testing and debugging the IC," thus simplifying "the

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[20] Found in claims 17 and 19.
[21] The court also relies on the intrinsic and extrinsic evidence discussed in paragraphs 16-18.
[22] Found in claim 1.
[23] Found in claim 7.

problem of resetting the IC and observing its current state." (4:33-38) The specification describes a mode of operation where

> the diagnostics console 103 invoke[s] the IC 100 to execute its normal system operations. If and when the selected trigger event is detected and the analysis engine 215 has captured the required data, the diagnostics console 103 instructs the SPU 101 to transfer the captured data values out of the IC 100 and into the diagnostics console 103 where the data may be formatted and presented for analysis and interpretation.

(14:20-27) The specification also describes "normal mode" and "test mode" in the context of input and output signals, which terms do not define "normal system operations:"[24]

> The control signal on the line 300 selects whether the functional signal at data-in terminal 302 or the signal held in the scan flip-flop 301 is passed onto the data-out terminal 307. When the control signal of the line 300 signal is not-asserted, i.e., normal mode, there is normal operational signal flow between the data-in terminal 302 and the data-out terminal 307. On the other hand, when the control signal on the line 300 is in asserted state, i.e., test mode, the current state of the scan flip-flop 301 is passed onto the data-out terminal 307; the data-in terminal 302 and the data-out terminal 307 are isolated from one another.

(8:4-15)[25]

23. **"System bus:"** [26] "A communication path within a system that can be shared." The specification describes various embodiments wherein the system bus connects various components: a host processor connected by a system bus to various circuit blocks (6:15-17); a peripheral bus which is connected to the system bus by a bridge (6:19-20); "a system bus interface 214, a test bus interface 213 and a built-in

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[24] This section of the specification contains the singular use of each term – "test mode" and "normal mode."

[25] **Extrinsic evidence.** IV's expert, Dr. Oklobzija, opines that this passage shows that "normal mode and test mode are used to refer to how data signals are passed out from the device." (D.I. 235 at ¶ 16)

[26] Found in claim 7.

self-test (BIST) engine 212, which are all interconnected by a processor bus 219" (6:37-40); and the system bus connected to the SPU 101 (10:20-21; 12:30-31).

**The '742 Patent**

24. **"Bus interrupt line:"**[27] "A line dedicated to carrying bus interrupt signals." The specification describes "an intelligent daisy-chainable serial (IDCS) bus structure [that] is used to connect one or more peripheral devices to a base station such as a palm-top computer." (2:13-17) "The ICDS bus of this invention is fully interrupt driven. Peripheral devices send interrupts over a bus interrupt line to get the attention of the bus dispatch unit."[28] (4:25-27) "Base station 100 is connected to bus connector 401 by a first bi-directional signal line MBDATA, a second bi-directional signal line MBCLK, and unidirectional interrupt line MBINT." (12:65-13:1) "If a peripheral device needs to transfer data to bus dispatch 305, peripheral device 410, 420 or 430 must first interrupt bus dispatch 305 via a unidirectional interrupt on its respective line MBINT . . . ." (14:50-53) "Interrupt signals flow only from peripheral devices . . . to bus dispatch 305, i.e., upstream only, and so buffers on line MBINT pass a signal upstream to bus dispatch 305." (17:1-4)

25. **"Data transfer speed of the peripheral device:"**[29] "Speed at which the peripheral device can transfer data." Claims 62 and 63 recite in part "wherein information including the data transfer speed of the peripheral device is sent to a bus

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[27] Found in claim 57.

[28] **Extrinsic evidence.** Toshiba's expert, Dr. Stevenson, opines that "if a line is denoted as carrying a certain type of signal, a person of ordinary skill in the art would understand that it only carries that type of signal." (D.I. 205 at ¶ 19) IV did not provide expert testimony regarding this claim limitation.

[29] Found in claims 62 and 63.

dispatch." The specification explains that a peripheral configuration sequence is performed, wherein

> bus dispatch 305 requests identification and peripheral information . . . for each newly addressed peripheral device on IDCS bus 150. Bus dispatch 305 also locates and attaches a peripheral client for each of the newly addressed peripheral devices. The information procured tells bus dispatch 305 how to refer to the peripheral device and the speeds at which bus dispatch 305 can send commands and data to the peripheral device as well as important peripheral device requirements like the frequency of interrupt servicing required during isochronous data transfers.

(50:43-53) Command sequencer 2614, has a "set bus speed step 2901" in which "bus dispatch 305 sets the speed of IDCS bus 150 based on the type of command or data being sent and the capabilities of the addressed peripheral device." (59:30-33)

26. **"Locate peripheral client sequence:"**[30] "Steps used to find the client (software driver) that can service the peripheral device." The specification explains that in the "locate client sequence 2103, . . . bus dispatch 305 uses the peripheral ID information to find the client that can service the peripheral device." (54:18-21) The "client" is the "software driver" for the peripheral device. (2:33-39)

**The '788 Patent**

27. **"Packet-to-ATA bridge"**[31] **and "packet-to-ATA bridging device:"**[32] "Hardware or software that enables packet-to-ATA or ATA-to-packet transfer." The specifications explains that "[t]he portions of the [patented] method . . . that are performed by the bridge form another aspect of the invention. The methods can be

[30] Found in claim 62.
[31] Found in claim 10.
[32] Found in claim 24.

performed by hardware, software, or a combination of the two." (4:24-27) More specifically,

> [a]lthough the [patent's] description focuses on a hardware bridge implementation, the described methods are also appropriate for software implementation. As such, the scope of the present invention extends to an apparatus comprising a computer-readable medium containing computer instructions that, when executed, cause a processor or multiple communicating processors to perform one of the described methods.

(13:30-38)

28. **"Parsing the command block into a sequence of ATA register operations:"**[33] "Retrieving a sequence of ATA register operations from the command block." The specification explains that a command block in packet format is transmitted to the packet-to-ATA bridge. "The bridge parses the command block into a sequence of ATA operations necessary to execute the given ATA register-delivered transaction." (4:9-23) For example, "an ATA command protocol adapter is included [in an apparatus comprising a packet-to-ATA bridge] to parse a command packet into a sequence of ATA register operations and cause that sequence of operations to be performed by the ATA register protocol adapter." (4:41-44) Or, "[w]hen controller 166 receives an ATA command block, it recognizes the command block as such, checks it for inconsistencies, and parses it into a sequence of ATA register accesses." (6:11-14)

29. **"ATA interface:"**[34] "Component used to transmit ATA host signals to an ATA device and receive ATA device signals from the device." The specification describes the "ATA interface 98 [as] provid[ing] the low-level timing, handshaking, and signal-driving necessary to communicate with ATAPI device 100 over ATA PHY 101."

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[33] Found in claims 10 and 24.
[34] Found in claims 10 and 24.

(3:34-37) In another aspect of the invention, "[t]he bridge also comprises an ATA interface to transmit ATA bus host signals to an ATA device and receive ATA device signals from the device." (4:34-36)

30. The court has provided a construction in quotes for the claim limitations at issue. The parties are expected to present the claim construction consistently with any explanation or clarification herein provided by the court, even if such language is not included within the quotes.

United States District Judge