IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF DELAWARE

INTELLECTUAL VENTURES II LLC, Plaintiff, v. TOSHIBA CORPORATION, TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC., and TOSHIBA AMERICA INFORMATION SYSTEMS, INC., Defendants.	)	Civ. No. 13-453-SLR

MEMORANDUM ORDER

At Wilmington this 24th day of January, 2017, having reviewed the papers (D.I. 582, 586) filed in connection with the issues raised at trial;

IT IS ORDERED that the disputed claim language of U.S. Patent No. 5,701,270 ("the '270 patent") shall be construed consistent with the tenets of claim construction set forth by the United States Court of Appeals for the Federal Circuit in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005), as follows:

1. **"Redundancy bus:"**[1] "Address bus that allows for addressing of the redundant rows/columns independent of the addressing of the primary rows and columns through the primary address bus.[2] For the addressing to be independent, the

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[1] Found in claim 1, 3, and 20 of the '270 patent.

[2] *See* '270 patent, 12:37-40 ("redundancy bus 301 allows for addressing of the redundant rows/columns 205 independent of the addressing of the primary rows and columns through address bus 202.")

addresses must be unique to the redundant rows/columns.[3] The primary and redundancy buses may be multiplexed[4] and may transmit primary and redundancy addresses at different times.[5]"

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[3] "The redundancy address bits increase the size to the address set (space) to each bank to accommodate unique addressing of redundant rows/columns. Hence, even if the lower order address bits are identical for a good primary row/column and a programmed redundant row in the same bank, the redundancy address bits R_z insure that an access is not steered to multiple rows/columns during replacement." ('270 patent, 12:40-47)

[4] (D.I. 559 at 29)

[5] There are no temporal requirements in the specification; there is no record evidence that "independent addressing" has a temporal meaning in the art.